



# PSMN013-100XS

N-channel 100V 13 mΩ standard level MOSFET in TO220F (SOT186A)

Rev. 2 — 6 March 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel MOSFET in TO220F (SOT186A) package qualified to 175°C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Isolated package
- Suitable for standard level gate drive

### 1.3 Applications

- AC-to-DC power supply equipment
- Server power supplies
- Motor control
- Synchronous rectification

### 1.4 Quick reference data

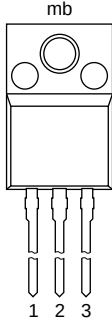
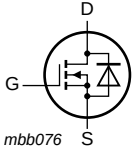
Table 1. Quick reference data

| Symbol                         | Parameter                                    | Conditions                                                                                                                                                                     | Min | Typ  | Max  | Unit |
|--------------------------------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|------|------|
| $V_{DS}$                       | drain-source voltage                         | $T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$                                                                                                                             | -   | -    | 100  | V    |
| $I_D$                          | drain current                                | $T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a>                                                                                                | -   | -    | 35.2 | A    |
| $P_{tot}$                      | total power dissipation                      | $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>                                                                                                                         | -   | -    | 48.4 | W    |
| <b>Static characteristics</b>  |                                              |                                                                                                                                                                                |     |      |      |      |
| $R_{DS(on)}$                   | drain-source on-state resistance             | $V_{GS} = 10\text{ V}$ ; $I_D = 10\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>                                            | -   | 10.8 | 13.9 | mΩ   |
| <b>Dynamic characteristics</b> |                                              |                                                                                                                                                                                |     |      |      |      |
| $Q_{GD}$                       | gate-drain charge                            | $V_{GS} = 10\text{ V}$ ; $I_D = 10\text{ A}$ ; $V_{DS} = 50\text{ V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>                                          | -   | 17.5 | -    | nC   |
| $Q_{G(tot)}$                   | total gate charge                            |                                                                                                                                                                                | -   | 57.5 | -    | nC   |
| <b>Avalanche ruggedness</b>    |                                              |                                                                                                                                                                                |     |      |      |      |
| $E_{DS(AL)S}$                  | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $I_D = 35.2\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; unclamped; $R_{GS} = 50\text{ Ω}$ ; see <a href="#">Figure 3</a> | -   | -    | 180  | mJ   |



## 2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description             | Simplified outline                                                                | Graphic symbol                                                                      |
|-----|--------|-------------------------|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| 1   | G      | gate                    |  |  |
| 2   | D      | drain                   |                                                                                   |                                                                                     |
| 3   | S      | source                  |                                                                                   |                                                                                     |
| mb  |        | mounting base; isolated |                                                                                   |                                                                                     |

SOT186A (TO-220F)

## 3. Ordering information

Table 3. Ordering information

| Type number   | Package |                                                                                                     |         |
|---------------|---------|-----------------------------------------------------------------------------------------------------|---------|
|               | Name    | Description                                                                                         | Version |
| PSMN013-100XS | TO-220F | plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" | SOT186A |

## 4. Limiting values

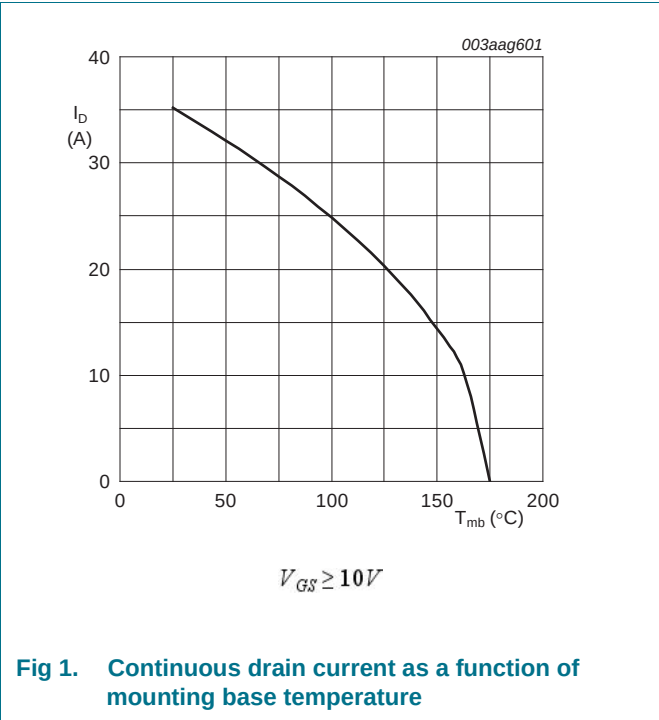
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

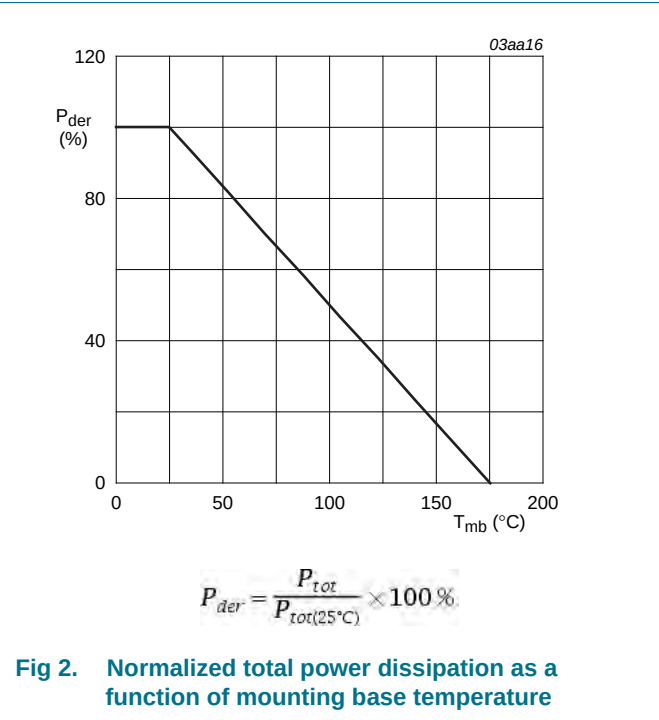
| Symbol       | Parameter                  | Conditions                                                                                        | Min | Max  | Unit |
|--------------|----------------------------|---------------------------------------------------------------------------------------------------|-----|------|------|
| $V_{DS}$     | drain-source voltage       | $T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$                                                | -   | 100  | V    |
| $V_{DGR}$    | drain-gate voltage         | $T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$                 | -   | 100  | V    |
| $V_{GS}$     | gate-source voltage        |                                                                                                   | -20 | 20   | V    |
| $I_D$        | drain current              | $V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>                   | -   | 35.2 | A    |
|              |                            | $V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>                  | -   | 24.9 | A    |
| $I_{DM}$     | peak drain current         | pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 4</a> | -   | 141  | A    |
| $P_{tot}$    | total power dissipation    | $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>                                            | -   | 48.4 | W    |
| $T_{stg}$    | storage temperature        |                                                                                                   | -55 | 175  | °C   |
| $T_j$        | junction temperature       |                                                                                                   | -55 | 175  | °C   |
| $T_{sld(M)}$ | peak soldering temperature |                                                                                                   | -   | 260  | °C   |

**Table 4. Limiting values ...continued**  
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                      | Parameter                                    | Conditions                                                                                                                                                               | Min | Max  | Unit |
|-----------------------------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|------|
| <b>Source-drain diode</b>   |                                              |                                                                                                                                                                          |     |      |      |
| I <sub>S</sub>              | source current                               | T <sub>mb</sub> = 25 °C                                                                                                                                                  | -   | 40.3 | A    |
| I <sub>SM</sub>             | peak source current                          | pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C                                                                                                                  | -   | 141  | A    |
| <b>Avalanche ruggedness</b> |                                              |                                                                                                                                                                          |     |      |      |
| E <sub>DS(AL)S</sub>        | non-repetitive drain-source avalanche energy | V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 35.2 A; V <sub>sup</sub> ≤ 100 V; unclamped; R <sub>GS</sub> = 50 Ω; see <a href="#">Figure 3</a> | -   | 180  | mJ   |



**Fig 1. Continuous drain current as a function of mounting base temperature**



**Fig 2. Normalized total power dissipation as a function of mounting base temperature**

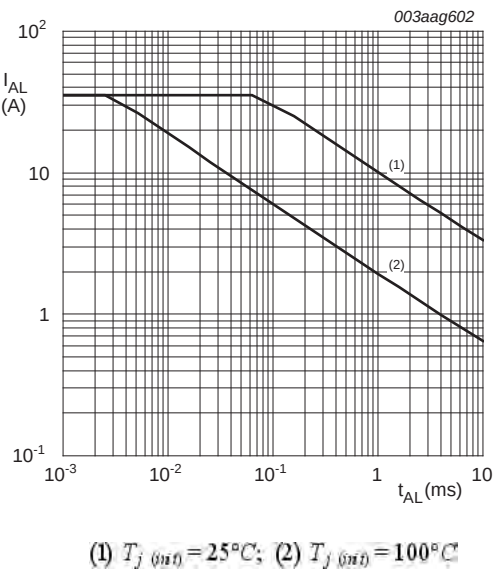


Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

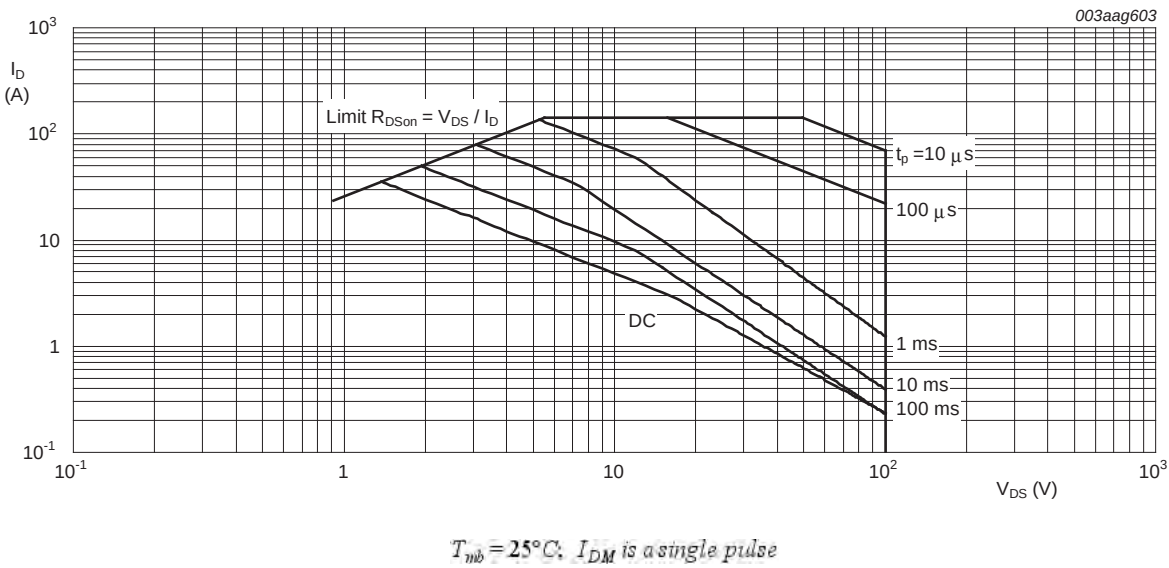
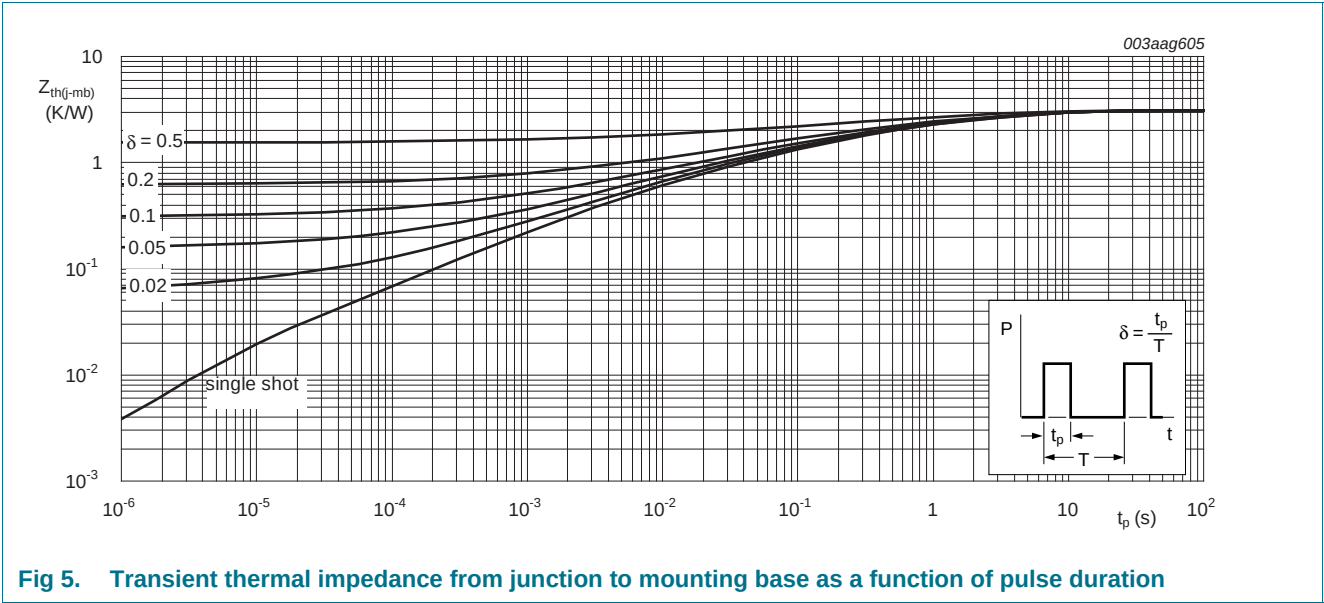


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol         | Parameter                                         | Conditions                   | Min | Typ  | Max | Unit |
|----------------|---------------------------------------------------|------------------------------|-----|------|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see <a href="#">Figure 5</a> | -   | 2.85 | 3.1 | K/W  |
| $R_{th(j-a)}$  | thermal resistance from junction to ambient       | vertical in free air         | -   | 55   | -   | K/W  |



6. Isolation characteristics

Table 6. Isolation characteristics

| Symbol          | Parameter             | Conditions                                                                                          | Min | Typ | Max  | Unit |
|-----------------|-----------------------|-----------------------------------------------------------------------------------------------------|-----|-----|------|------|
| $C_{isol}$      | isolation capacitance | $f = 1\text{ MHz}$                                                                                  | -   | 10  | -    | pF   |
| $V_{isol(RMS)}$ | RMS isolation voltage | $50\text{ Hz} \leq f \leq 60\text{ Hz}$ ; $RH \leq 65\%$ ; sinusoidal waveform; clean and dust free | -   | -   | 2500 | V    |

## 7. Characteristics

Table 7. Characteristics

| Symbol                         | Parameter                         | Conditions                                                                                                                               | Min | Typ  | Max  | Unit    |
|--------------------------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|-----|------|------|---------|
| <b>Static characteristics</b>  |                                   |                                                                                                                                          |     |      |      |         |
| $V_{(BR)DSS}$                  | drain-source breakdown voltage    | $I_D = 250\ \mu A$ ; $V_{GS} = 0\ V$ ; $T_j = 25\ ^\circ C$                                                                              | 100 | -    | -    | V       |
|                                |                                   | $I_D = 250\ \mu A$ ; $V_{GS} = 0\ V$ ; $T_j = -55\ ^\circ C$                                                                             | 90  | -    | -    | V       |
| $V_{GS(th)}$                   | gate-source threshold voltage     | $I_D = 1\ mA$ ; $V_{DS} = V_{GS}$ ; $T_j = 25\ ^\circ C$ ; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>                 | 2   | 3    | 4    | V       |
|                                |                                   | $I_D = 1\ mA$ ; $V_{DS} = V_{GS}$ ; $T_j = 175\ ^\circ C$ ; see <a href="#">Figure 10</a>                                                | 1   | -    | -    | V       |
|                                |                                   | $I_D = 1\ mA$ ; $V_{DS} = V_{GS}$ ; $T_j = -55\ ^\circ C$ ; see <a href="#">Figure 10</a>                                                | -   | -    | 4.6  | V       |
| $I_{DSS}$                      | drain leakage current             | $V_{DS} = 100\ V$ ; $V_{GS} = 0\ V$ ; $T_j = 25\ ^\circ C$                                                                               | -   | -    | 2    | $\mu A$ |
|                                |                                   | $V_{DS} = 100\ V$ ; $V_{GS} = 0\ V$ ; $T_j = 100\ ^\circ C$                                                                              | -   | -    | 40   | $\mu A$ |
| $I_{GSS}$                      | gate leakage current              | $V_{GS} = 20\ V$ ; $V_{DS} = 0\ V$ ; $T_j = 25\ ^\circ C$                                                                                | -   | 2    | 100  | nA      |
|                                |                                   | $V_{GS} = -20\ V$ ; $V_{DS} = 0\ V$ ; $T_j = 25\ ^\circ C$                                                                               | -   | 2    | 100  | nA      |
| $R_{DS(on)}$                   | drain-source on-state resistance  | $V_{GS} = 10\ V$ ; $I_D = 10\ A$ ; $T_j = 25\ ^\circ C$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>                  | -   | 10.8 | 13.9 | mΩ      |
|                                |                                   | $V_{GS} = 10\ V$ ; $I_D = 10\ A$ ; $T_j = 100\ ^\circ C$ ; see <a href="#">Figure 13</a>                                                 | -   | 18.9 | 24.3 | mΩ      |
|                                |                                   | $V_{GS} = 10\ V$ ; $I_D = 10\ A$ ; $T_j = 175\ ^\circ C$ ; see <a href="#">Figure 13</a>                                                 | -   | 30.2 | 38.9 | mΩ      |
| $R_G$                          | internal gate resistance (AC)     | $f = 1\ MHz$                                                                                                                             | -   | 1    | -    | Ω       |
| <b>Dynamic characteristics</b> |                                   |                                                                                                                                          |     |      |      |         |
| $Q_{G(tot)}$                   | total gate charge                 | $I_D = 10\ A$ ; $V_{DS} = 50\ V$ ; $V_{GS} = 10\ V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>                      | -   | 57.5 | -    | nC      |
| $Q_{GS}$                       | gate-source charge                |                                                                                                                                          | -   | 13.1 | -    | nC      |
| $Q_{GS(th)}$                   | pre-threshold gate-source charge  |                                                                                                                                          | -   | 8.8  | -    | nC      |
| $Q_{GS(th-pl)}$                | post-threshold gate-source charge |                                                                                                                                          | -   | 4.3  | -    | nC      |
| $Q_{GD}$                       | gate-drain charge                 |                                                                                                                                          | -   | 17.5 | -    | nC      |
| $V_{GS(pl)}$                   | gate-source plateau voltage       | $I_D = 10\ A$ ; $V_{DS} = 50\ V$ ; see <a href="#">Figure 14</a>                                                                         | -   | 4.5  | -    | V       |
| $C_{iss}$                      | input capacitance                 | $V_{DS} = 50\ V$ ; $V_{GS} = 0\ V$ ; $f = 1\ MHz$ ; $T_j = 25\ ^\circ C$ ; see <a href="#">Figure 16</a> ; see <a href="#">Figure 17</a> | -   | 3195 | -    | pF      |
| $C_{oss}$                      | output capacitance                | $V_{DS} = 50\ V$ ; $V_{GS} = 0\ V$ ; $f = 1\ MHz$ ; $T_j = 25\ ^\circ C$ ; see <a href="#">Figure 16</a>                                 | -   | 221  | -    | pF      |
| $C_{rss}$                      | reverse transfer capacitance      | $V_{DS} = 50\ V$ ; $V_{GS} = 0\ V$ ; $f = 1\ MHz$ ; $T_j = 25\ ^\circ C$ ; see <a href="#">Figure 16</a> ; see <a href="#">Figure 17</a> | -   | 136  | -    | pF      |
| $t_{d(on)}$                    | turn-on delay time                | $V_{DS} = 50\ V$ ; $R_L = 5\ \Omega$ ; $V_{GS} = 10\ V$ ; $R_{G(ext)} = 4.7\ \Omega$ ; $T_j = 25\ ^\circ C$                              | -   | 18   | -    | ns      |
| $t_r$                          | rise time                         |                                                                                                                                          | -   | 18   | -    | ns      |
| $t_{d(off)}$                   | turn-off delay time               |                                                                                                                                          | -   | 46   | -    | ns      |
| $t_f$                          | fall time                         |                                                                                                                                          | -   | 21   | -    | ns      |

Table 7. Characteristics ...continued

| Symbol             | Parameter             | Conditions                                                                            | Min | Typ | Max | Unit |
|--------------------|-----------------------|---------------------------------------------------------------------------------------|-----|-----|-----|------|
| Source-drain diode |                       |                                                                                       |     |     |     |      |
| $V_{SD}$           | source-drain voltage  | $I_S = 10\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_J = 25\text{ °C}$ ; see Figure 18    | -   | 0.8 | 1.2 | V    |
| $t_{rr}$           | reverse recovery time | $I_S = 10\text{ A}$ ; $dI_S/dt = -100\text{ A/}\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; | -   | 52  | -   | ns   |
| $Q_r$              | recovered charge      | $V_{DS} = 50\text{ V}$                                                                | -   | 109 | -   | nC   |

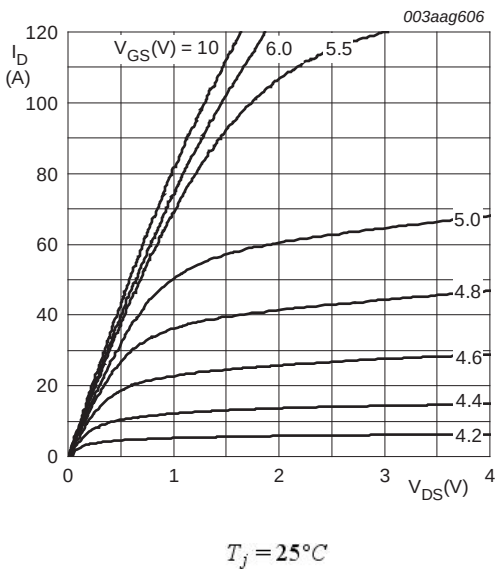


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values

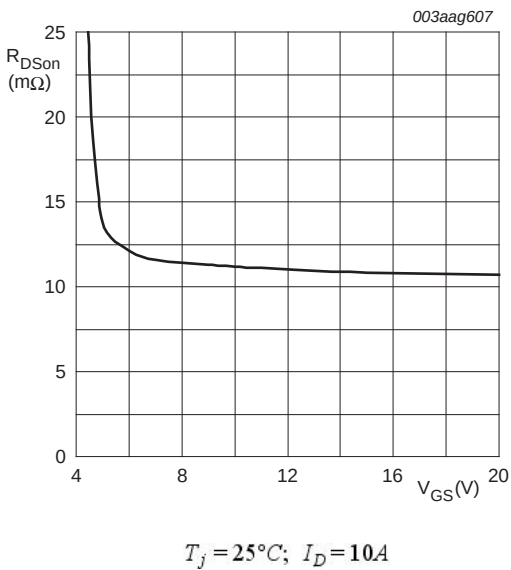


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

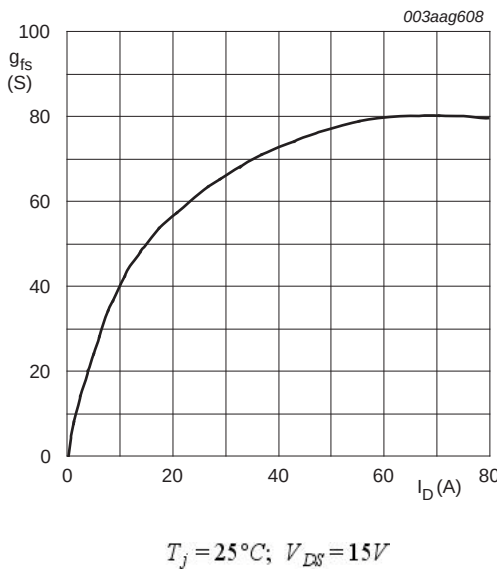


Fig 8. Forward transconductance as a function of drain current; typical values

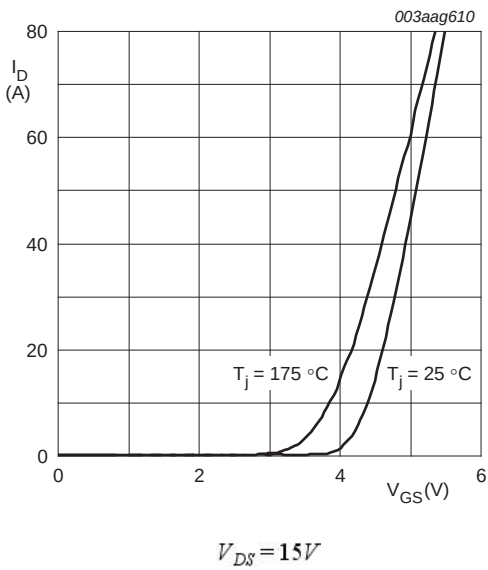
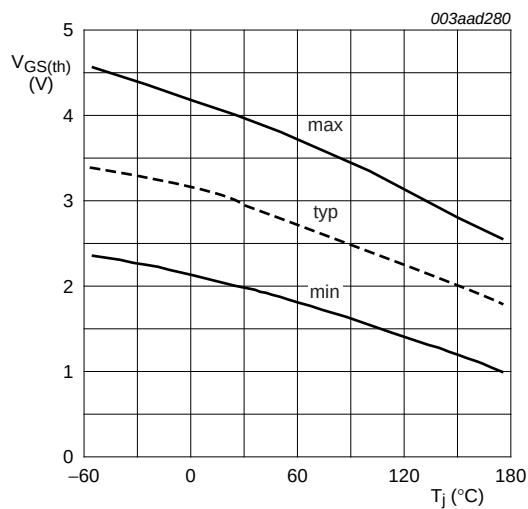
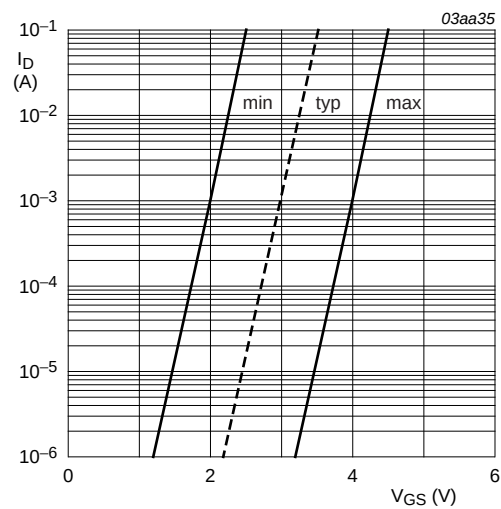


Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values



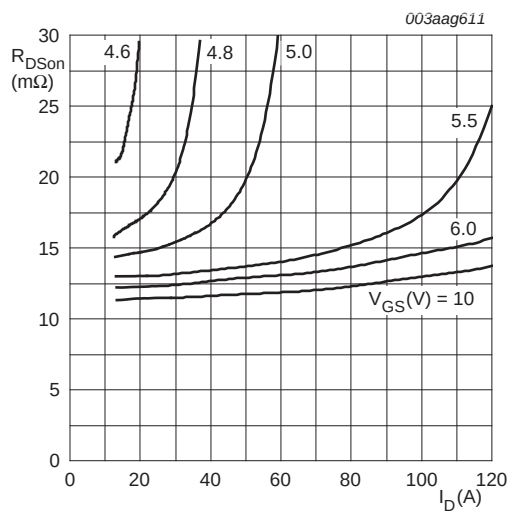
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



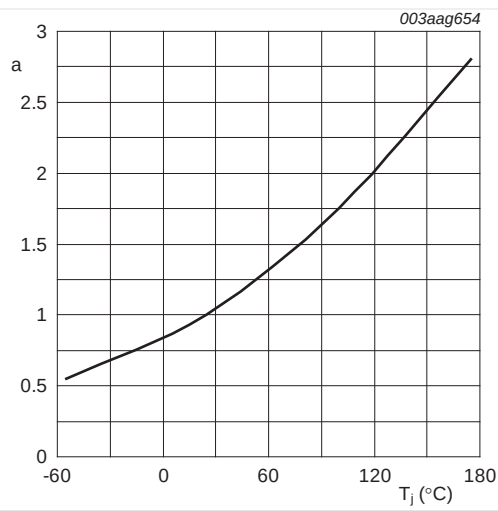
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25^\circ\text{C}$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values



$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



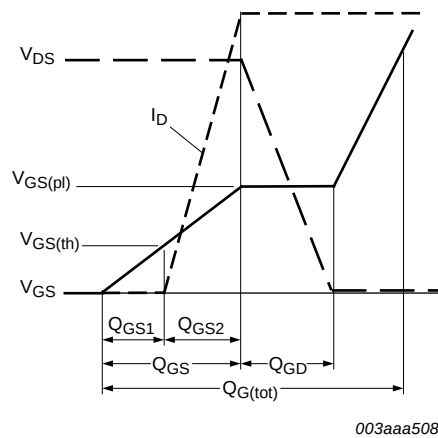
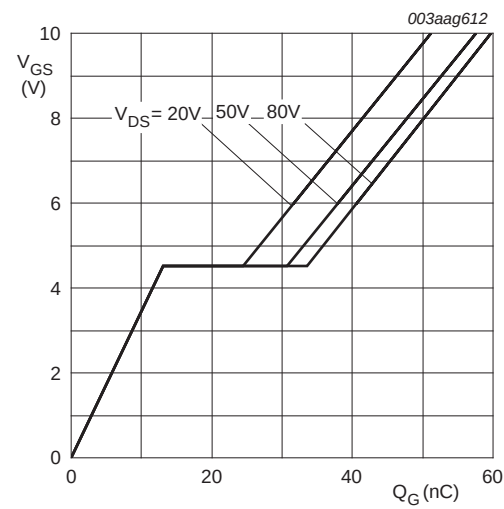
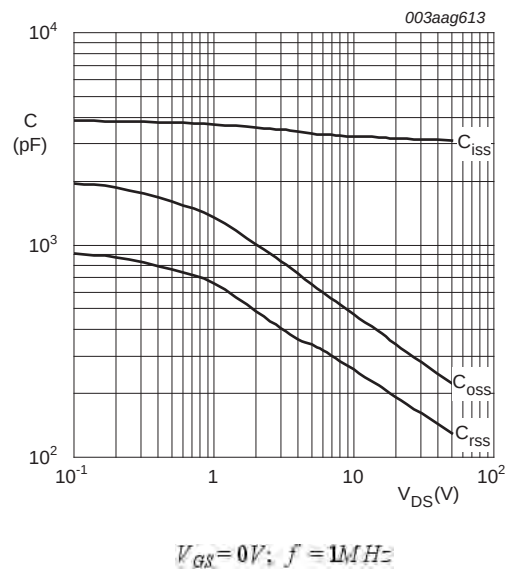


Fig 14. Gate charge waveform definitions



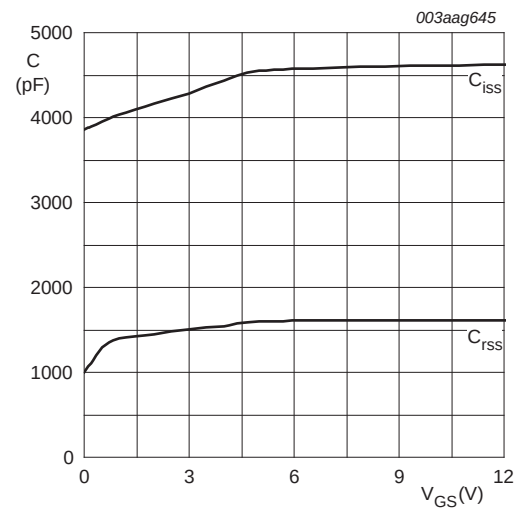
$T_j = 25^{\circ}C; I_D = 10A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$f = 1MHz; V_{DS} = 0V$

Fig 17. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

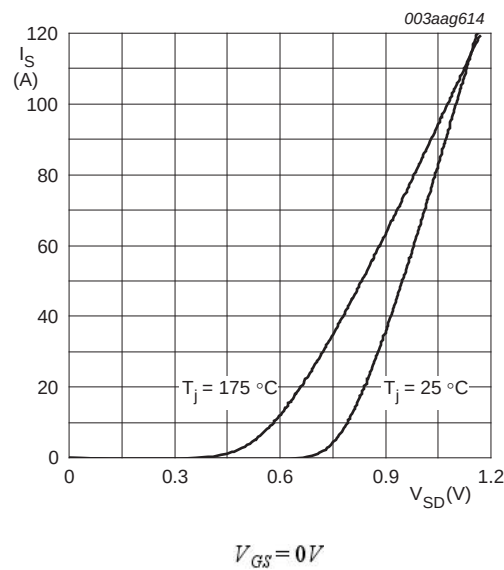


Fig 18. Source current as a function of source-drain voltage; typical values

8. Package outline

Plastic single-ended package; isolated heatsink mounted;  
1 mounting hole; 3-lead TO-220 'full pack'

SOT186A

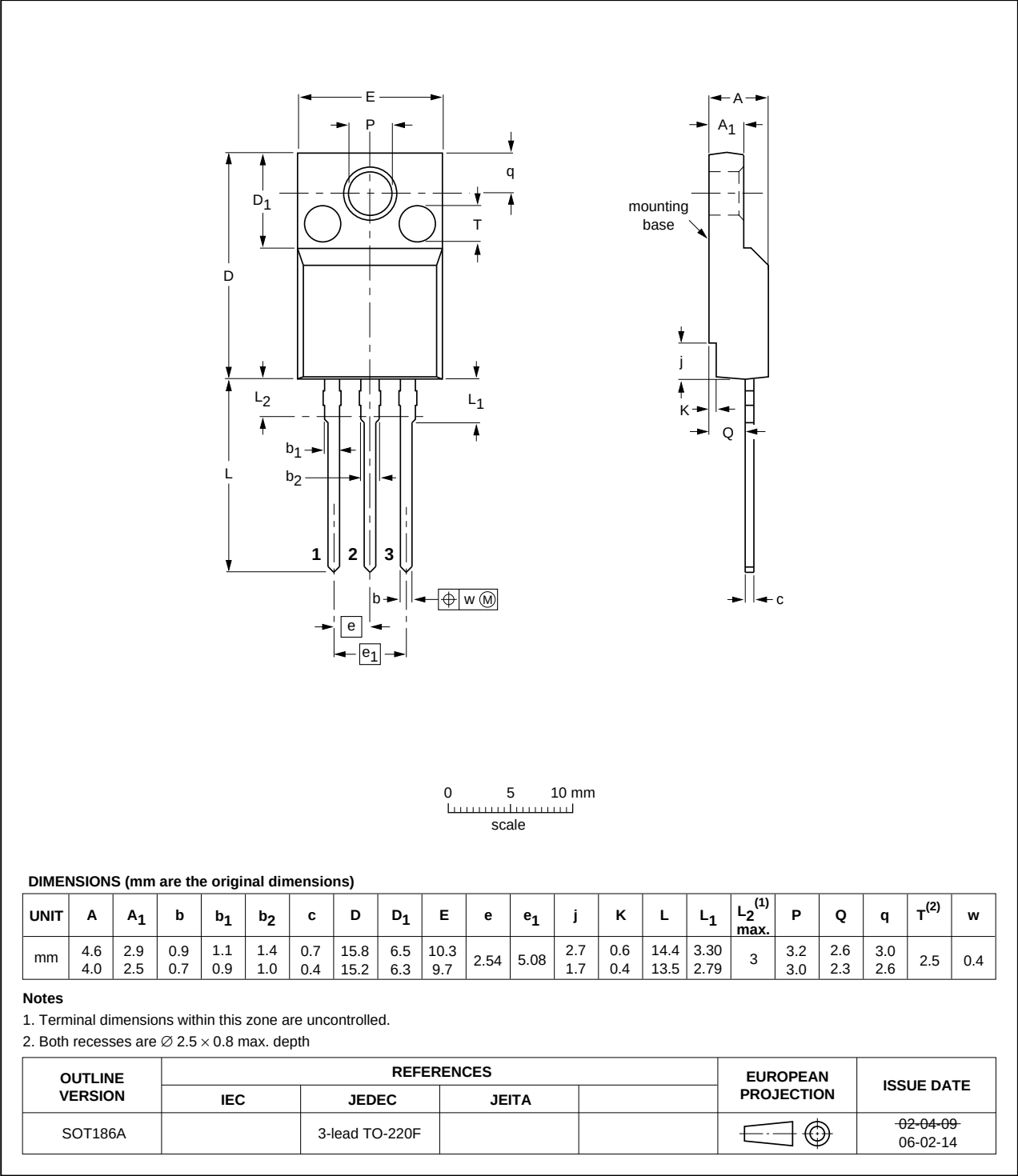


Fig 19. Package outline SOT186A (TO-220F)

## 9. Revision history

Table 8. Revision history

| Document ID       | Release date                                                                                                                        | Data sheet status      | Change notice | Supersedes        |
|-------------------|-------------------------------------------------------------------------------------------------------------------------------------|------------------------|---------------|-------------------|
| PSMN013-100XS v.2 | 20120306                                                                                                                            | Product data sheet     | -             | PSMN013-100XS v.1 |
| Modifications:    | <ul style="list-style-type: none"><li>• Status changed from preliminary to product.</li><li>• Various changes to content.</li></ul> |                        |               |                   |
| PSMN013-100XS v.1 | 20111213                                                                                                                            | Preliminary data sheet | -             | -                 |

## 10. Legal information

### 10.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 11. Contact information

For more information, please visit: <http://www.nxp.com>

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