

DATA SHEET

74F579

8-bit bidirectional binary counter (3-State)

Product specification
Supersedes data of 1992 May 04

2000 Dec 18

8-bit bidirectional binary counter (3-State)

74F579

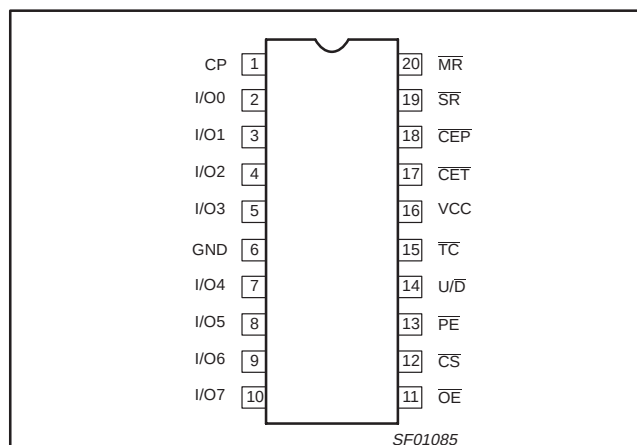
FEATURES

- Fully synchronous operation
- Multiplexed 3-State I/O ports for bus oriented applications
- Built in cascading carry capability
- $\overline{U/\overline{D}}$ pin to control direction of counting
- Separate pins for Master reset and Synchronous operation
- Center power pins to reduce effects of package inductance
- Count frequency 115 MHz Typ
- Supply current 100 mA Typ
- See 74F269 for 24-pin separate I/O port version
- See 74F779 for 16-pin version

DESCRIPTION

The 74F579 is a fully synchronous 8-stage Up/Down Counter with multiplexed 3-State I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a $\overline{U/\overline{D}}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock. $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

PIN CONFIGURATION



ORDERING INFORMATION

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F579	115MHz	100 mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5\text{ V} \pm 10\%$, $T_{amb} = 0\text{ to }+70\text{ }^{\circ}\text{C}$	PKG DWG #
20-Pin Plastic DIP	N74F579N	SOT146-1
20-Pin Plastic SOL	N74F579D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

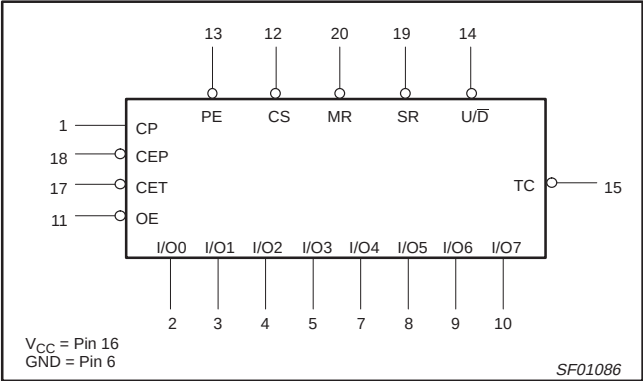
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH / LOW
I/O_n	Data Inputs	3.5/1.0	70 μA / 0.6 mA
	Data Outputs	150/40	3.0 mA / 24 mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20 μA / 0.6 mA
$\overline{U/\overline{D}}$	Up/Down count control input	1.0/1.0	20 μA / 0.6 mA
MR	Master Reset input (active Low)	1.0/1.0	20 μA / 0.6 mA
$\overline{SR}$	Synchronous Reset input (active Low)	1.0/1.0	20 μA / 0.6 mA
$\overline{CEP}$	Count Enable Parallel input (active Low)	1.0/1.0	20 μA / 0.6 mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20 μA / 0.6 mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20 μA / 0.6 mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20 μA / 0.6 mA
CP	Clock input (active Rising Edge)	1.0/1.0	20 μA / 0.6 mA
$\overline{TC}$	Terminal Count Output (active Low)	50/33	1.0 mA / 20 mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 μA in the High state and 0.6 mA in the Low state.

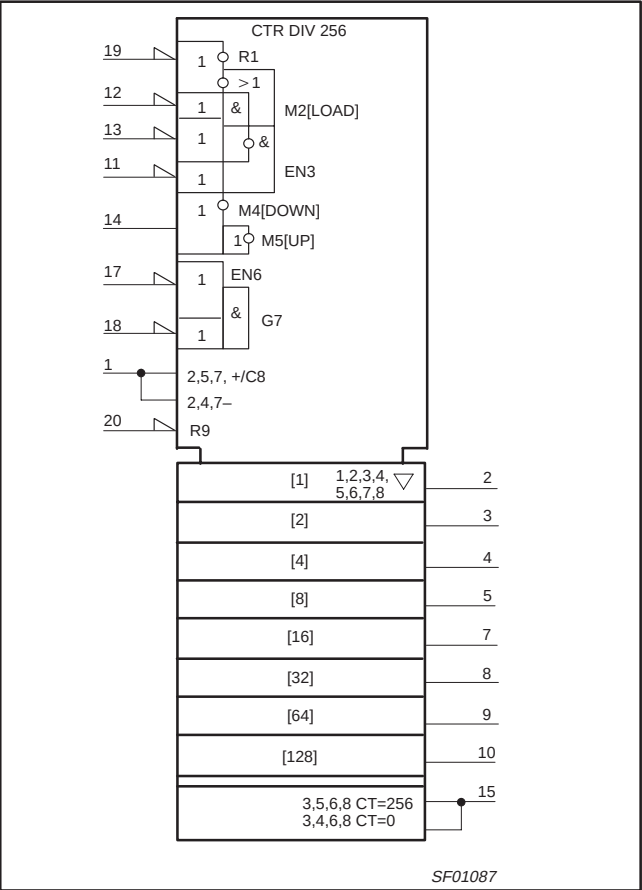
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LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

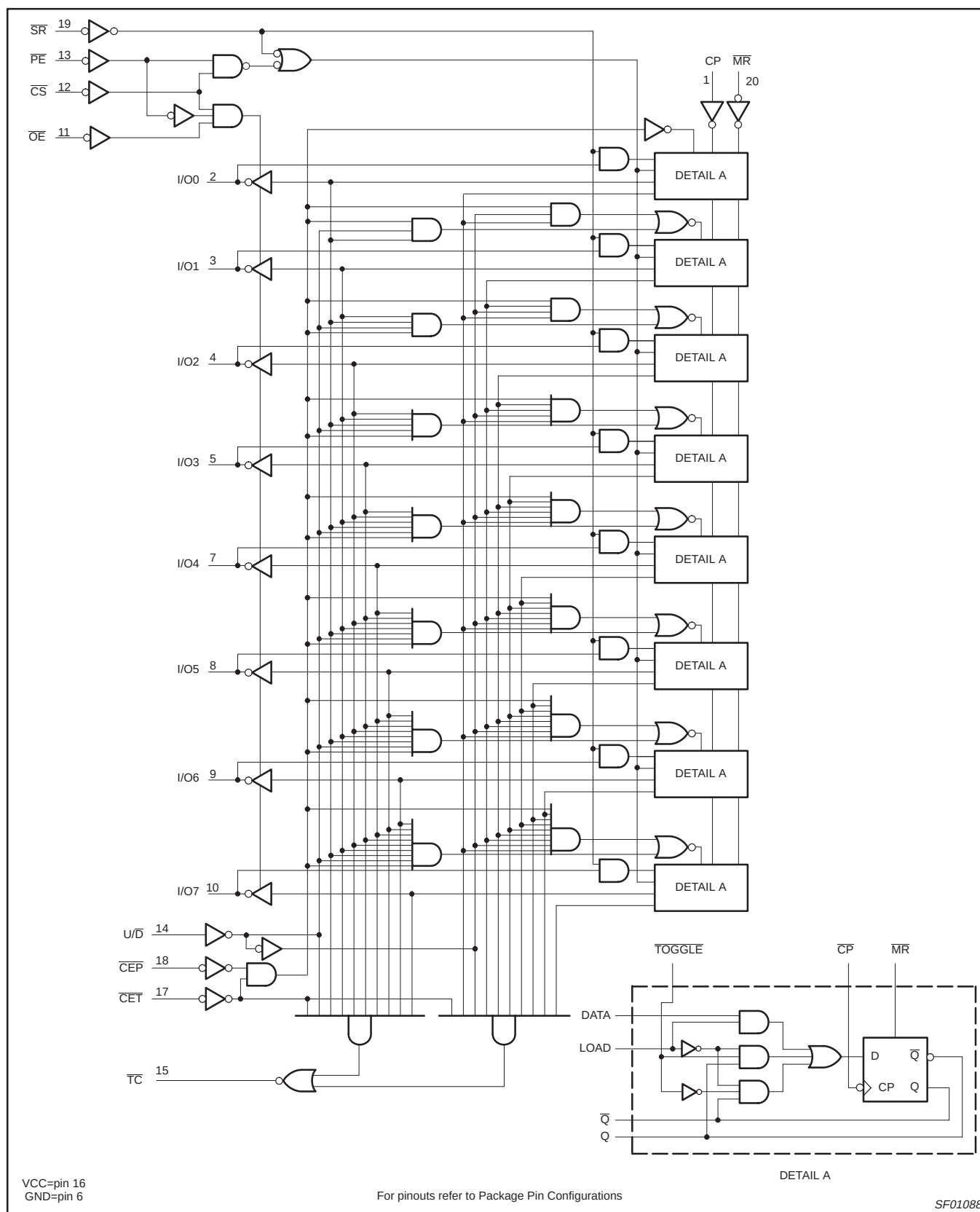
INPUTS									OPERATING MODE
MR	SR	CS	PE	CEP	CET	U/D	OE	CP	
X	X	H	X	X	X	X	X	X	I/O0 to I/O7 in high impedance ($\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/O0 to I/O7 in high impedance
X	X	L	H	X	X	X	L	X	Flip-flop output appears on I/O _n lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold (TC held High)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = $\overline{CS}$ and $\overline{PE}$ should never be Low voltage level at the same time.

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LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.

Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_O	Voltage applied to output in High output state		-0.5 to + V_{CC}	V
I_O	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/O ₀	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$\overline{TC}$			-1	mA
		I/O _n			-3	mA
I_{OL}	Low-level output current	$\overline{TC}$			20	mA
		I/O _n			24	mA
T_{amb}	Operating free-air temperature range		0		70	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹			LIMITS			UNIT
						MIN	TYP ²	MAX	
V _{OH}	High-level output voltage	T _C	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN (V _{IL} = 0.0 V, V _{IH} = 4.5 V for MR, CP inputs)	I _{OH} = −1 mA	±10%V _{CC}	2.5			V
					±5%V _{CC}	2.7	3.4		V
		I/O _n		I _{OH} = −3 mA	±10%V _{CC}	2.4	3.3		V
					±5%V _{CC}	2.7	3.3		V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = MAX,	±10%V _{CC}		0.35	0.50	V
					±5%V _{CC}		0.35	0.50	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}				−0.73	−1.2	V
I _I	Input current at maximum input voltage	I/O _n	V _{CC} = MAX, V _I = 5.5 V					1	mA
		others	V _{CC} = MAX, V _I = 7.0 V					100	μA
I _{IH}	High-level input current	except I/O _n	V _{CC} = MAX, V _I = 2.7 V					20	μA
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.5 V					−0.6	mA
I _{OZH} + I _{IH}	Off-state output current High-level voltage applied	I/O _n	V _{CC} = MAX, V _O = 2.7 V					70	μA
I _{OZL} + I _{IL}	Off-state output current Low-level voltage applied		V _{CC} = MAX, V _O = 0.5 V					−600	μA
I _{OS}	Short-circuit output current ³		V _{CC} = MAX			−60		−150	mA
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX				95	135	mA
		I _{CCL}					105	145	mA
		I _{CCZ}					105	150	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions for the applicable type.
- All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDI- TIONS	LIMITS					UNIT
			$T_{amb} = +25\text{ }^{\circ}\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}, R_L = 500\text{ }\Omega$			$T_{amb} = 0\text{ to }+70\text{ }^{\circ}\text{C}$ $V_{CC} = +5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}, R_L = 500\text{ }\Omega$		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	Waveform 1	100	115		80		MHz
t _{PLH} t _{PHL}	Propagation delay CP to I/O _n	Waveform 1	5.0 5.0	7.5 7.5	10.5 10.5	4.5 5.0	11.5 11.5	ns ns
t _{PLH} t _{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	5.5 5.5	7.5 7.5	10.0 10.0	5.0 5.0	11.0 11.0	ns ns
t _{PLH} t _{PHL}	Propagation delay U/D to $\overline{TC}$	Waveform 4	3.5 4.5	5.5 6.5	8.0 8.0	3.5 4.5	9.0 9.0	ns ns
t _{PLH} t _{PHL}	Propagation delay CET to $\overline{TC}$	Waveform 3	3.5 3.5	5.5 6.0	7.0 8.0	3.5 3.5	8.5 8.5	ns ns
t _{PHL}	Propagation delay MR to I/O _n	Waveform 2	5.0	7.0	9.0	5.0	10.0	ns
t _{PLH} t _{PHL}	Propagation delay $\overline{MR}$ to $\overline{TC}$	Waveform 4	4.0 6.0	6.5 8.0	9.0 10.5	4.0 6.0	10.5 12.5	ns ns
t _{PZH} t _{PZL}	Output Enable time $\overline{CS}$ to I/O _n	Waveform 6 Waveform 7	4.0 5.5	5.0 7.0	8.5 10.5	3.5 5.0	10.0 11.5	ns ns
t _{PHZ} t _{PLZ}	Output Disable time $\overline{CS}$ to I/O _n	Waveform 6 Waveform 7	3.0 5.0	5.0 7.5	7.5 9.5	3.0 4.5	9.0 11.0	ns ns
t _{PZH} t _{PZL}	Output Enable time PE to I/O _n	Waveform 6 Waveform 7	3.0 5.0	4.5 6.5	8.0 10.0	3.0 4.5	9.0 11.0	ns ns
t _{PHZ} t _{PLZ}	Output Disable time PE to I/O _n	Waveform 6 Waveform 7	3.0 2.5	4.0 4.0	7.5 7.5	3.0 2.0	9.0 8.5	ns ns
t _{PZH} t _{PZL}	Output Disable time $\overline{OE}$ to I/O _n	Waveform 6 Waveform 7	2.5 4.5	4.0 5.5	7.0 9.0	2.5 4.0	8.5 10.5	ns ns
t _{PHZ} t _{PLZ}	Output Enable time $\overline{OE}$ to I/O _n	Waveform 6 Waveform 7	1.0 2.0	2.5 4.0	4.0 7.0	1.0 2.0	5.5 8.0	ns ns

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AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_{amb} = +25\text{ }^{\circ}\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}, R_L = 500\text{ }\Omega$			$T_{amb} = 0\text{ to }+70\text{ }^{\circ}\text{C}$ $V_{CC} = +5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}, R_L = 500\text{ }\Omega$		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O _n to CP	Waveform 5	3.0 3.0			4.0 4.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O _n to CP	Waveform 5	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/ $\overline{D}$ to CP	Waveform 5	8.0 8.0			9.0 9.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/ $\overline{D}$ to CP	Waveform 5	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$, SR or CS to CP	Waveform 5	9.5 9.5			10.0 10.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$, $\overline{SR}$ or CS to CP	Waveform 5	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	5.0 9.0			5.5 10.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.5 4.5			4.5 4.5		ns ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	3.0			3.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

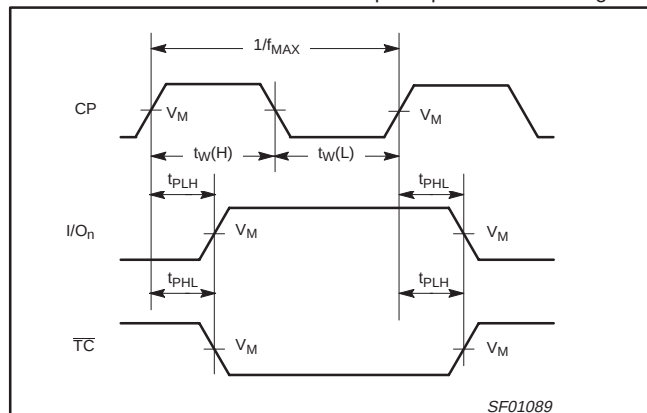
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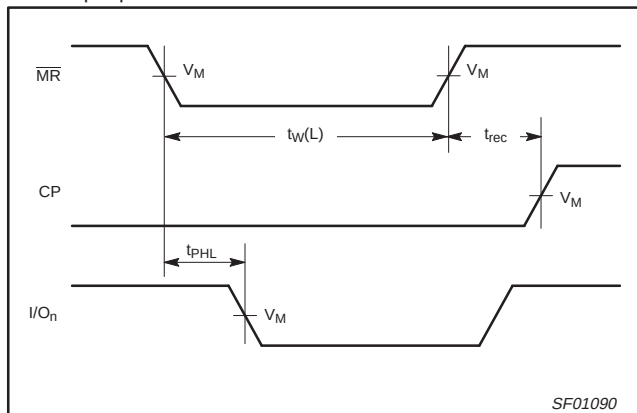
AC WAVEFORMS

NOTE: For all waveforms $V_M = 1.5$ V.

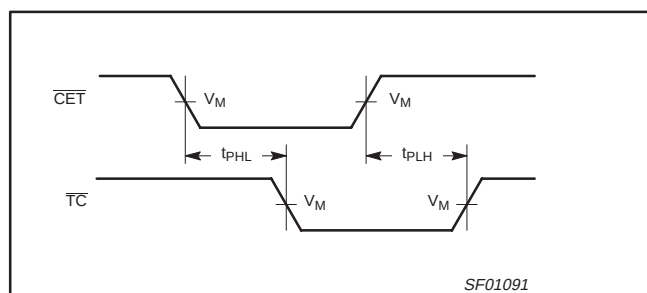
The shaded areas indicate when the input is permitted to change for predictable output performance.



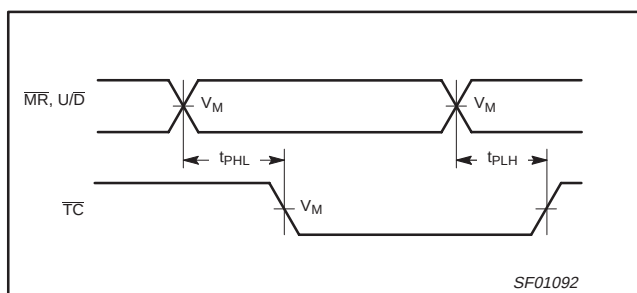
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency



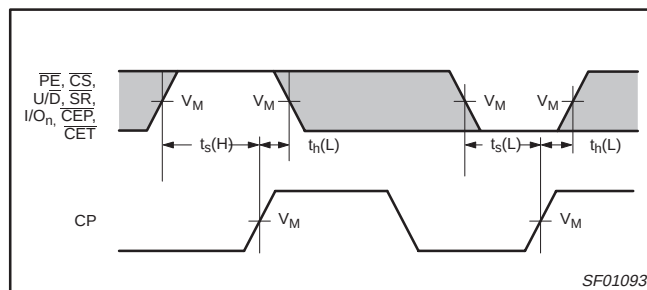
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



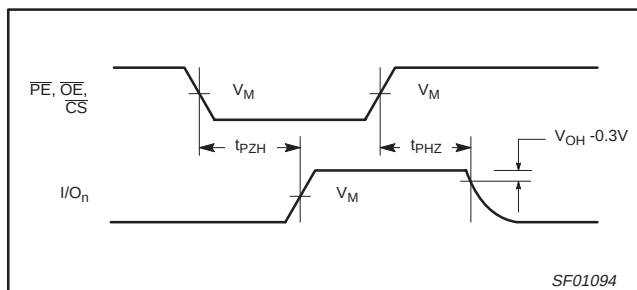
Waveform 3. Propagation Delay, $\overline{CET}$ Input to Terminal Count Output



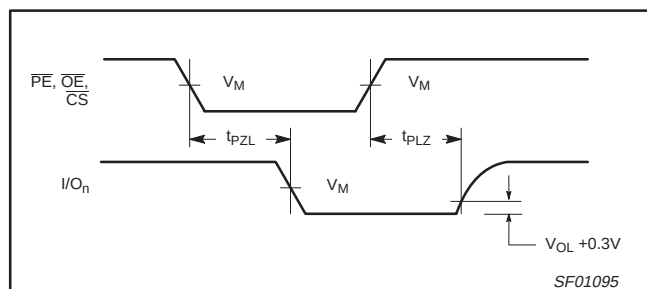
Waveform 4. Propagation Delay, $\overline{U/D}$ and $\overline{MR}$ Inputs to Terminal Count Output



Waveform 5. Setup and Hold Times



Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level

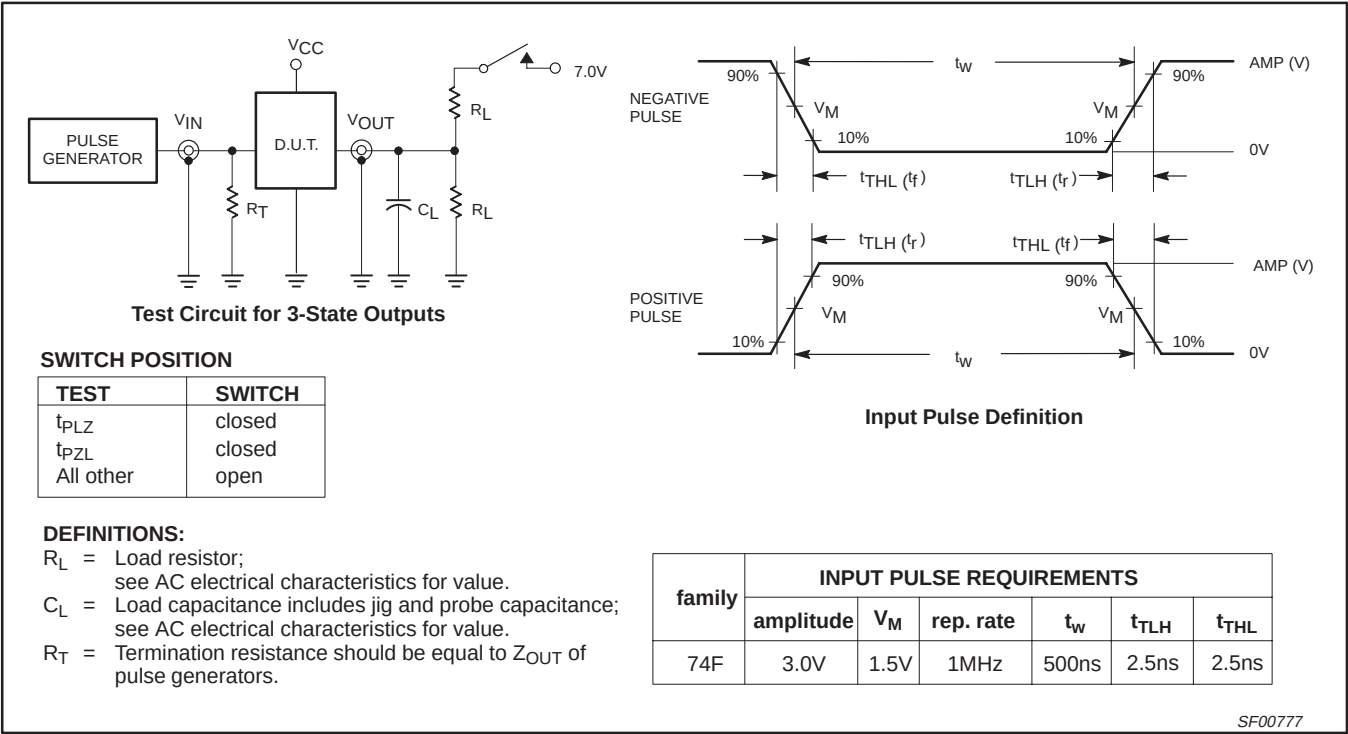


Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

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TEST CIRCUIT AND WAVEFORMS

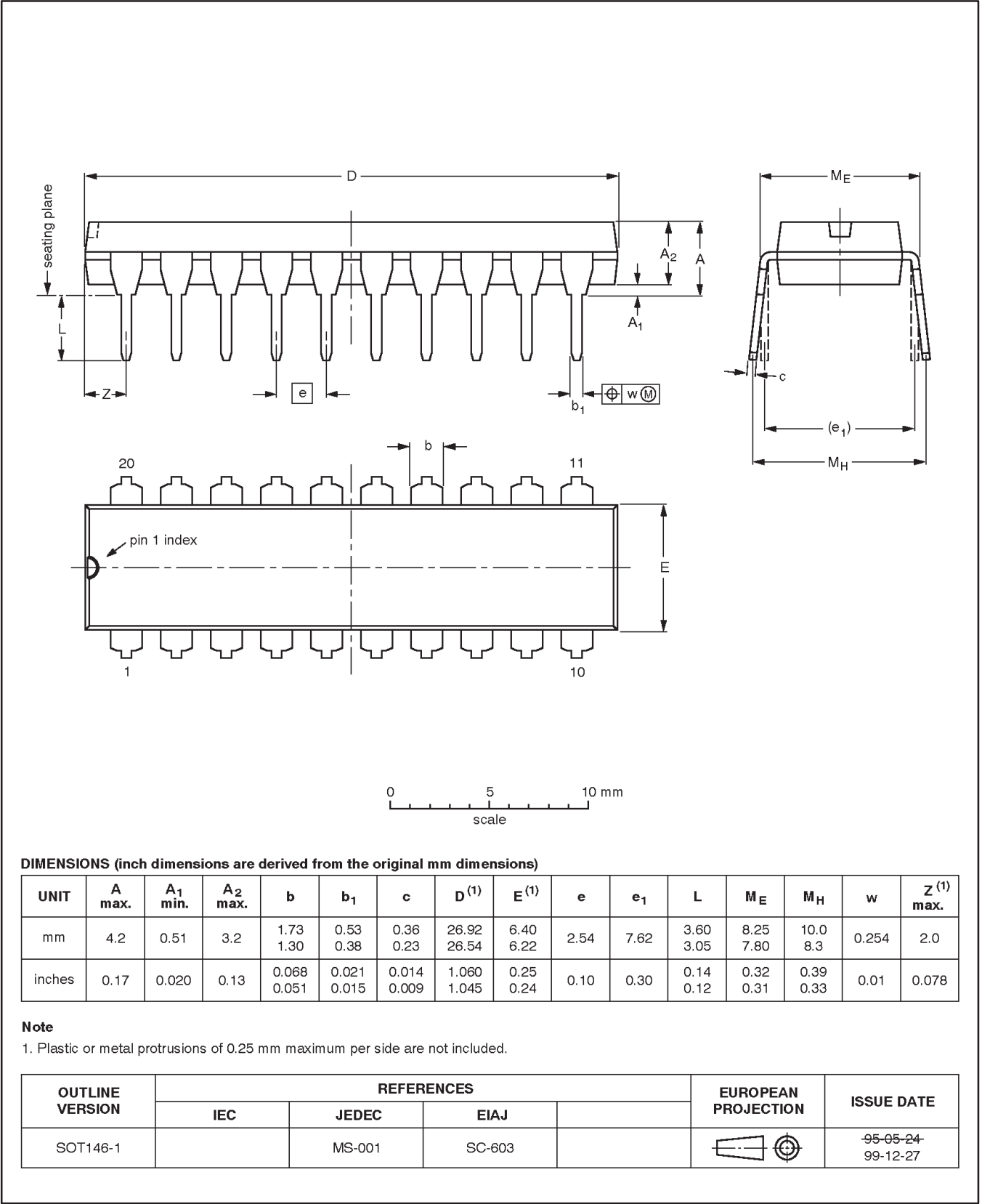


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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

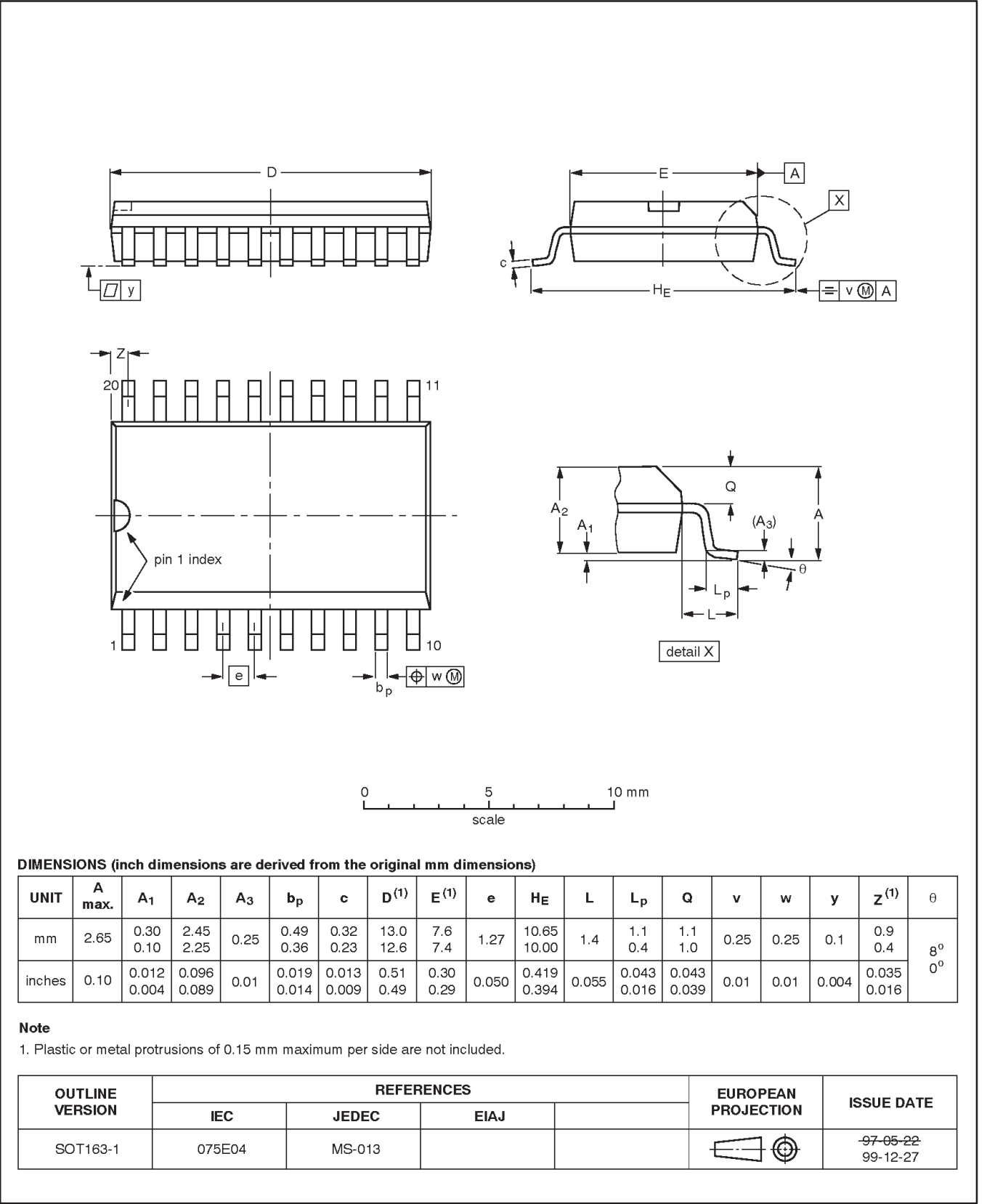


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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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