CY7C245A

2K x 8 Reprogrammable Registered PROM

Features

- **Windowed for reprogrammability**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 15-ns address set-up**
  - **— 10-ns clock to output**
- **Low power**
  - **— 330 mW (commercial) for -25 ns**
  - **— 660 mW (military)**
- **Programmable synchronous or asynchronous output enable**
- **On-chip edge-triggered registers**
- **Programmable asynchronous register ($\overline{\text{INIT}}$)**
- **EPROM technology, 100% programmable**
- **Slim, 300-mil, 24-pin plastic or hermetic DIP**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2001V static discharge**

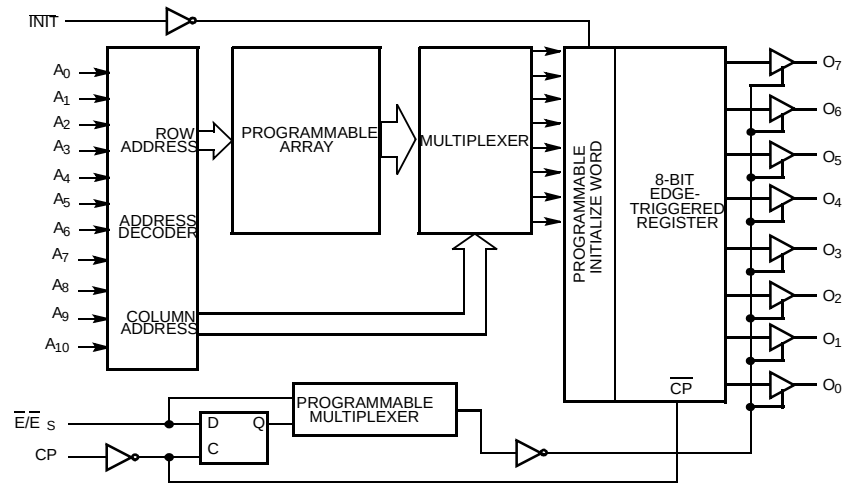
Functional Description

The CY7C245A is a high-performance, 2K x 8, electrically programmable, read only memory packaged in a slim 300-mil plastic or hermetic DIP. The ceramic package may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C245A replaces bipolar devices and offers the advantages of lower power, reprogrammability, superior performance and high programming yield. The EPROM cell requires only 12.5V for the supervoltage, and low current requirements allow gang programming. The EPROM cells allow each memory location to be tested 100%, because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

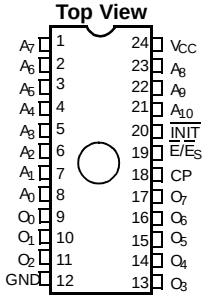
The CY7C245A has an asynchronous initialize function ($\overline{\text{INIT}}$). This function acts as a 2049th 8-bit word loaded into the on-chip register. It is user programmable with any desired word, or may be used as a PRESET or CLEAR function on the outputs. $\overline{\text{INIT}}$ is triggered by a low level, not an edge.

Logic Block Diagram

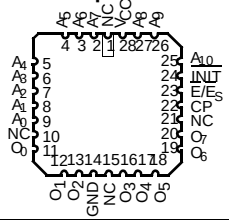


PinConfigurations

DIP
Top View



LCC/PLCC (Opaque only)
Top View



Selection Guide

			7C245A-15	7C245A-18	7C245A-25	7C245A-35	Unit
Minimum Address Set-Up Time			15	18	25	35	ns
Maximum Clock to Output			10	12	12	15	ns
Maximum Operating Current	Standard	Commercial	120	120	90	90	mA
		Military		120	120	120	mA

Maximum Ratings[1]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12).....–0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .....–0.5V to +7.0V

DC Input Voltage .....–3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

UV Erasure..... 7258 Wsec/cm^2

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[2]	–55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3,4]

Parameter	Description	Test Conditions		7C245A-15 Min.	7C245A-15 Max.	7C245A-18 Min.	7C245A-18 Max.	7C245A-25 7C245A-35 7C245A-45 Min.	7C245A-25 7C245A-35 7C245A-45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA, V_{IN} = V_{IH} or V_{IL}		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}			0.4		0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		–10	+10	–10	+10	–10	+10	µA
V_{CD}	Input Clamp Diode Voltage	Note 4								
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled[5]		–10	+10	–10	+10	–10	+10	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		–20	–90	–20	–90	–20	–90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		120		90	mA
			Mil				120		120	
V_{PP}	Programming Supply Voltage			12	13	12	13	12	13	V
I_{PP}	Programming Supply Current				50		50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4		0.4	V

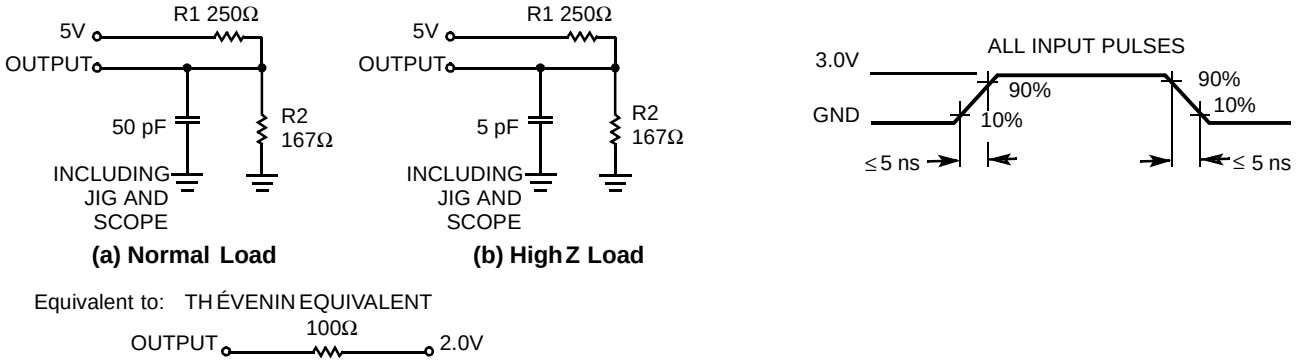
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms[3, 4]



Switching Characteristics Over Operating Range[3, 4]

Parameter	Description	7C245A-15		7C245A-18		7C245A-35		7C245A-25		7C245A-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	15		18		25		35		45		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		10		12		12		15		25	ns
t_{PWC}	Clock Pulse Width	10		12		15		20		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	10		10		12		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		5		5		5		5		ns
t_{DI}	Delay from $\overline{INIT}$ to Valid Output		15		20		20		20		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock HIGH	10		12		15		20		20		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	10		12		15		20		25		ns
t_{COS}	Valid Output from Clock HIGH[7]		15		15		15		20		30	ns
t_{HZC}	Inactive Output from Clock HIGH[7]		15		15		15		20		30	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW[8]		12		15		15		20		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[8]		15		15		15		20		30	ns

Notes:
7. Applies only when the synchronous ($\overline{E}_S$) function is used.
8. Applies only when the asynchronous ($\overline{E}$) function is used.

Operating Modes

The CY7C245A is a CMOS electrically programmable read only memory organized as 2048 words x 8 bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C245A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with a programmable synchronous ($\overline{E}_S$) or asynchronous ($\overline{E}$) output enable and asynchronous initialization ($\overline{INIT}$).

Upon power-up the state of the outputs will depend on the programmed state of the enable function ($\overline{E}_S$ or $\overline{E}$). If the synchronous enable ($\overline{E}_S$) has been programmed, the register will be in the set condition causing the outputs (O_0–O_7) to be in the OFF or high-impedance state. If the asynchronous enable ($\overline{E}$) is being used, the outputs will come up in the OFF or high-impedance state only if the enable ($\overline{E}$) input is at a HIGH logic level. Data is read by applying the memory location to the address inputs (A_0–A_{10}) and a logic LOW to the enable input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O_0–O_7).

If the asynchronous enable ($\overline{E}$) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

If the synchronous enable ($\overline{E}_S$) is being used, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C245A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

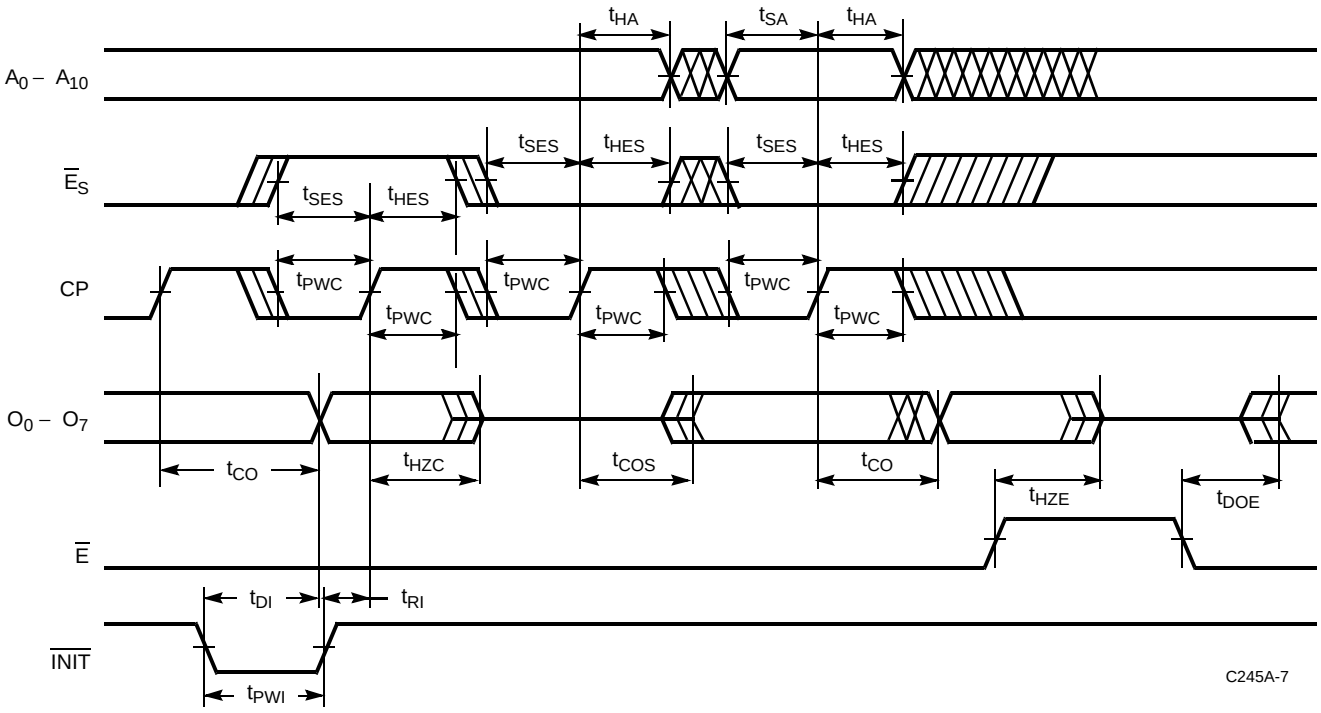
Operating Modes (Continued)

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C245A has an asynchronous initialize input ($\overline{INIT}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated, the initialize control input causes the contents of a user-programmed 2049th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1s and 0s into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

Switching Waveforms[4]



Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C245A. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 35 minutes. The 7C245A needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Bit Map Data

Programmer Address		RAM Data
Decimal	**Hex**	**Contents**
0	0	Data
.	.	.
.	.	.
.	.	.
2047	7FF	Data
2048	800	Init Byte
2049	801	Control Byte

Control Byte

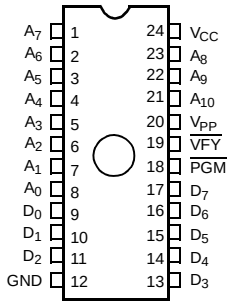
00 ..... Asynchronous output enable (default state)
01 ..... Synchronous output enable

Table 1. Mode Selection

Mode		Pin Function[9]							
	Read or Output Disable	A_{10}–A_4	A_3	A_2–A_1	A_0	CP	$\overline{E}$, $\overline{E_S}$	INIT	O_7–O_0
	Other	A_{10}–A_4	A_3	A_2–A_1	A_0	PGM	VFY	V_{PP}	D_7–D_0
Read		A_{10}–A_4	A_3	A_2–A_1	A_0	V_{IL}/V_{IH}	V_{IL}	V_{IH}	O_7–O_0
Output Disable		A_{10}–A_4	A_3	A_2–A_1	A_0	X	V_{IH}	V_{IH}	High Z
Initialize		A_{10}–A_4	A_3	A_2–A_1	A_0	X	V_{IL}	V_{IL}	Init. Byte
Program		A_{10}–A_4	A_3	A_2–A_1	A_0	V_{ILP}	V_{IHP}	V_{PP}	D_7–D_0
Program Verify		A_{10}–A_4	A_3	A_2–A_1	A_0	V_{IHP}	V_{ILP}	V_{PP}	O_7–O_0
Program Inhibit		A_{10}–A_4	A_3	A_2–A_1	A_0	V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		A_{10}–A_4	A_3	A_2–A_1	A_0	V_{ILP}	V_{IHP}	V_{PP}	D_7–D_0
Program Synchronous Enable		A_{10}–A_4	V_{IHP}	A_2–A_1	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	High Z
Program Initialization Byte		A_{10}–A_4	V_{ILP}	A_2–A_1	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	D_7–D_0
Blank Check Zeros		A_{10}–A_4	A_3	A_2–A_1	A_0	V_{IHP}	V_{ILP}	V_{PP}	Zeros

Note:
9. X = “don’t care” but not to exceed V_{CC} +5%.

DIP
Top View



LCC/PLCC (Opaque Only)
Top View

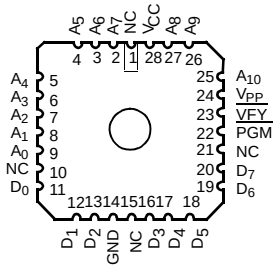
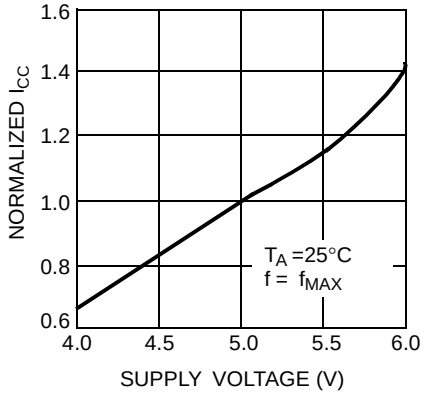


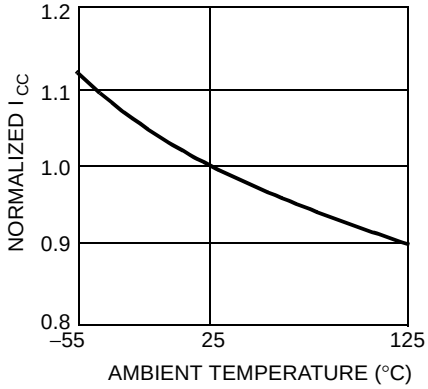
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

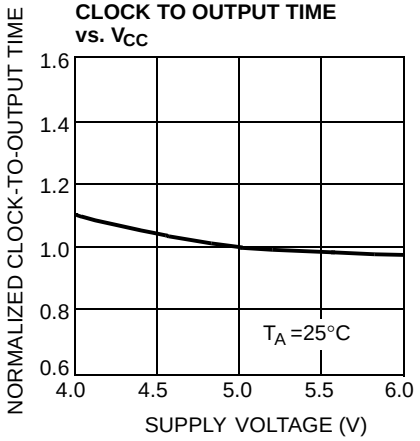
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



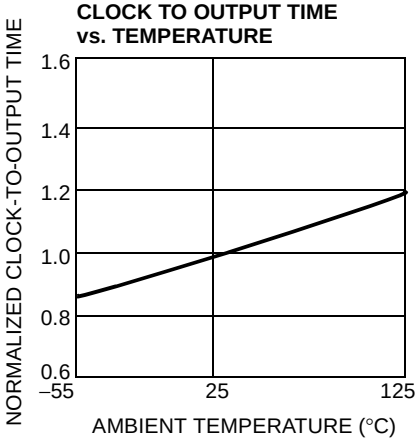
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



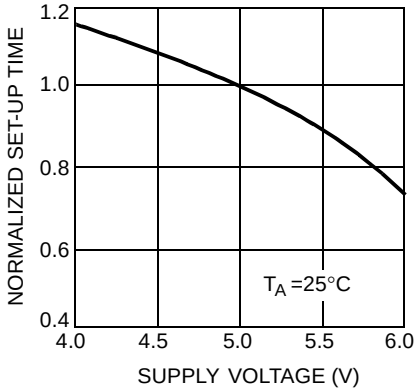
CLOCK TO OUTPUT TIME vs. V_{CC}



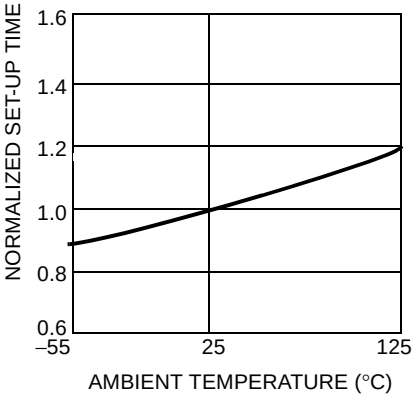
CLOCK TO OUTPUT TIME vs. TEMPERATURE



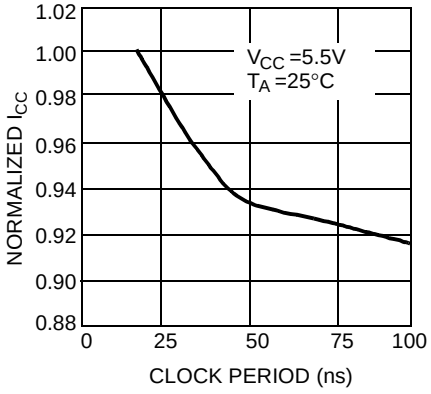
NORMALIZED SET-UP TIME vs. SUPPLYVOLTAGE



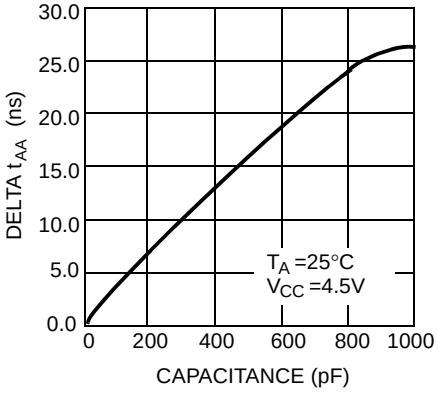
NORMALIZED SET-UP TIME vs. TEMPERATURE



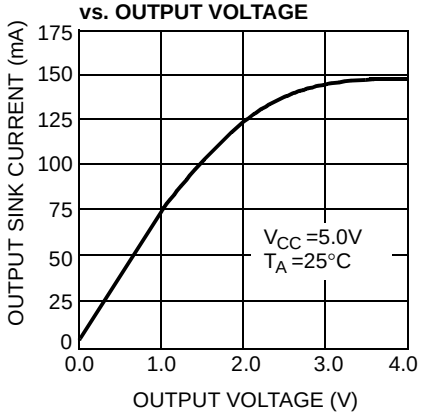
NORMALIZED SUPPLY CURRENT vs. CLOCK PERIOD



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information

Speed (ns)		I_{CC} (mA)	Ordering Code	Package Type	Package Type	Operating Range
t_{SA}	t_{CO}					
15	10	120	CY7C245A-15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
18	12	120	CY7C245A-18JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
			CY7C245A-18PC	P13	24-Lead (300-Mil) Molded DIP	
			CY7C245A-18WC	W14	24-Lead (300-Mil) Windowed CerDIP	
18	12	120	CY7C245A-18DMB	D14	24-Lead (300-Mil) CerDIP	Military
			CY7C245A-18QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
			CY7C245A-18WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
25	15	60	CY7C245A-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
			CY7C245A-25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
		90	CY7C245A-25JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY7C245A-25SC	S13	24-Lead Molded SOIC	
35	20	60	CY7C245A-35WC	W14	24-Lead (300-Mil) Windowed CerDIP	Commercial
		90	CY7C245A-35JC	J64	28-Lead Plastic Leaded Chip Carrier	
		120	CY7C245A-35DMB	D14	24-Lead (300-Mil) CerDIP	Military
			CY7C245A-35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

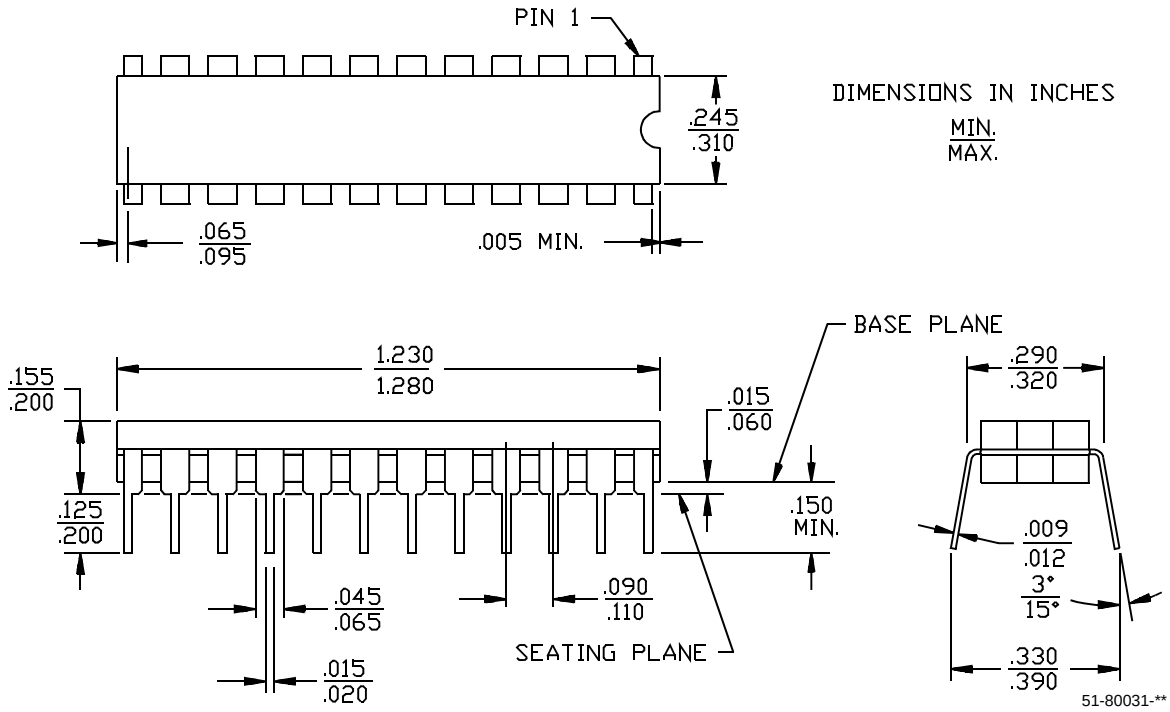
Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11

SMD Cross Reference

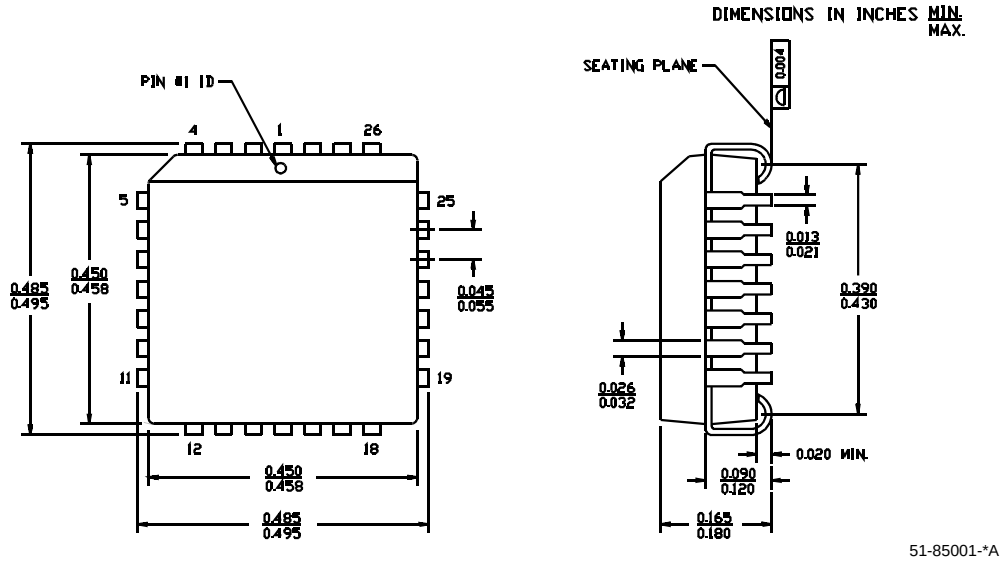
SMD Number	Suffix	Cypress Number
5962-88735	033X	CY7C245A-25LMB
5962-88735	04LX	CY7C245A-25DMB

Package Diagrams

24-Lead (300-Mil) CerDIP D14
MIL-STD-1835 D- 9 Config.A

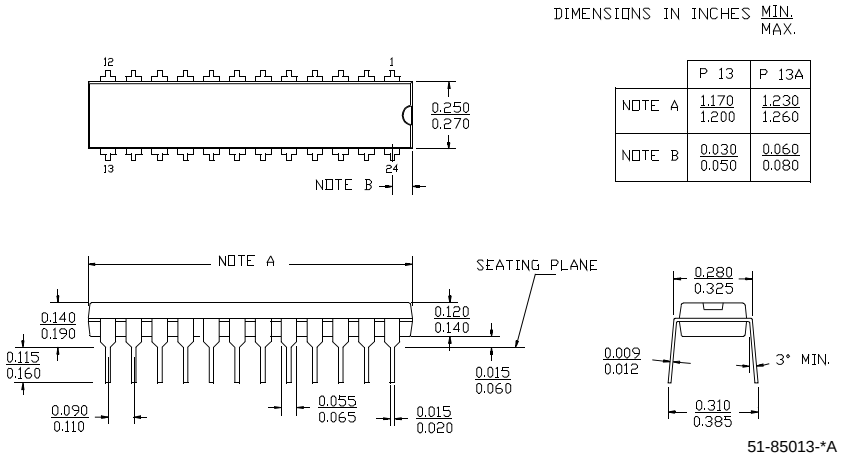


28-Lead Plastic Leaded Chip Carrier J64



Package Diagrams (continued)

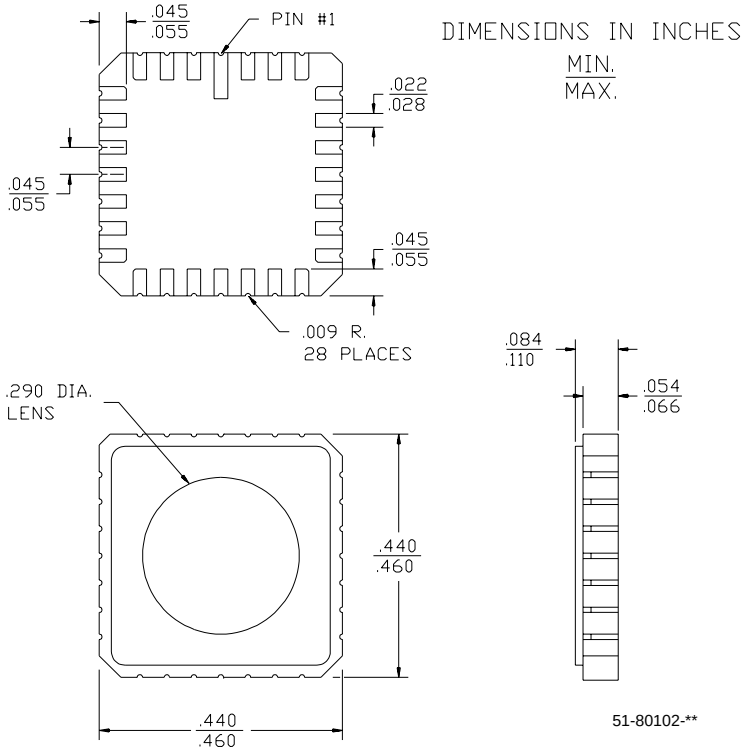
24-Lead (300-Mil) Molded DIP P13



51-85013-*A

28-Pin Windowed Leadless Chip Carrier Q64

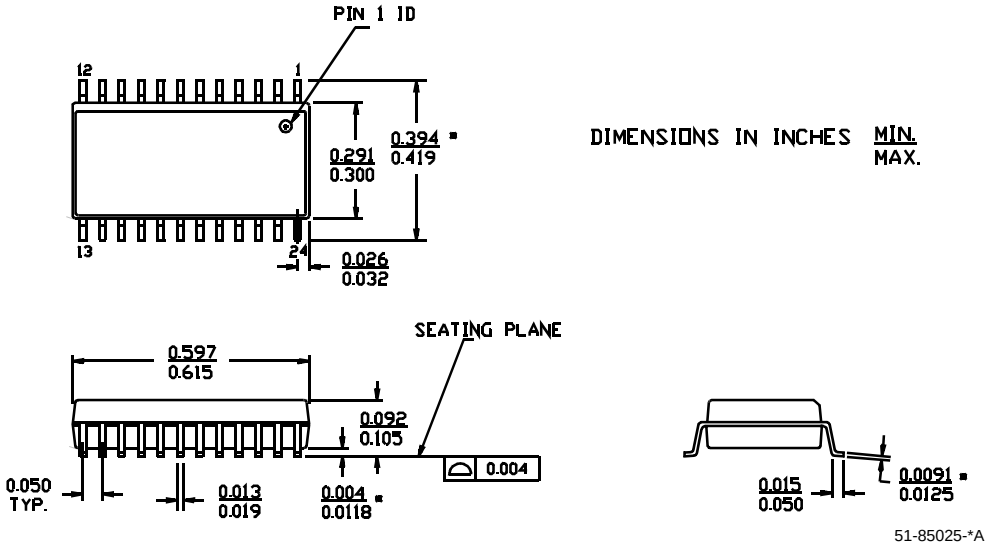
MIL–STD–1835 C–4



51-80102-**

Package Diagrams (continued)

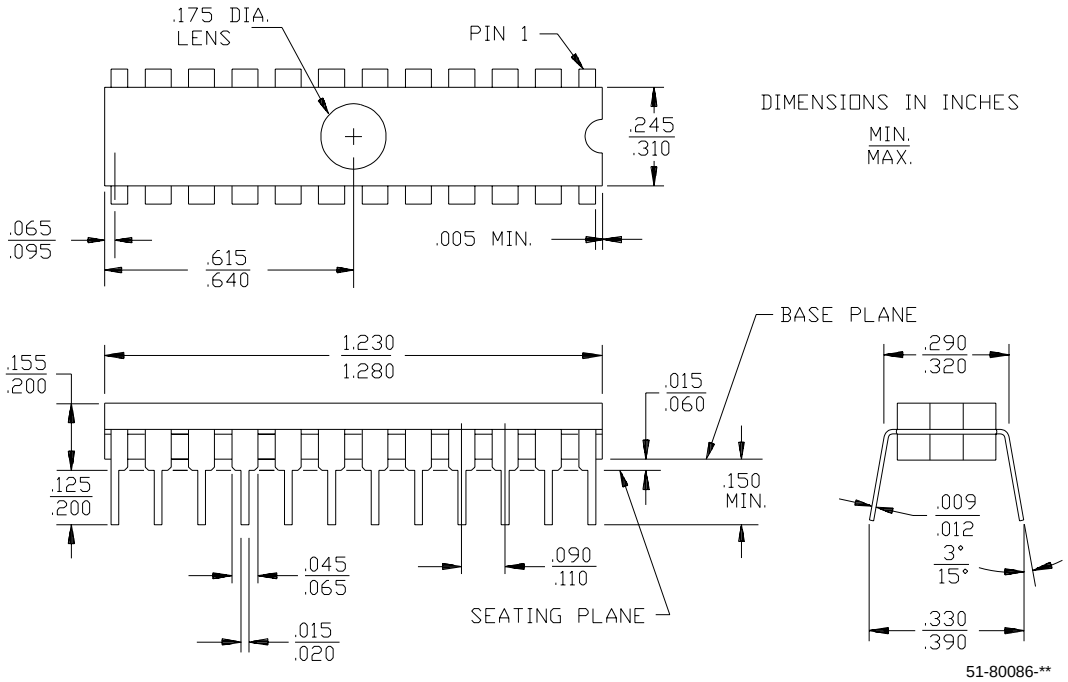
24-Lead (300-Mil) Molded SOIC S13



51-85025-*A

24-Lead (300-Mil) Windowed CerDIP W14

MIL-STD-1835 D-9 Config. A



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Document History Page

Document Title: CY7C245A 2K x 8 Reprogrammable Registered PROM Document Number: 38-04007				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	113863	3/6/02	DSG	Change from Spec number: 38-00074 to 38-04007
*A	118894	10/09/02	GBI	Update ordering information
*B	122248	12/27/02	RBI	Add power up requirements to Operating Conditions information