GaAs IC SPDT 4 W T/R Switch DC–2.5 GHz

AH002R2-11

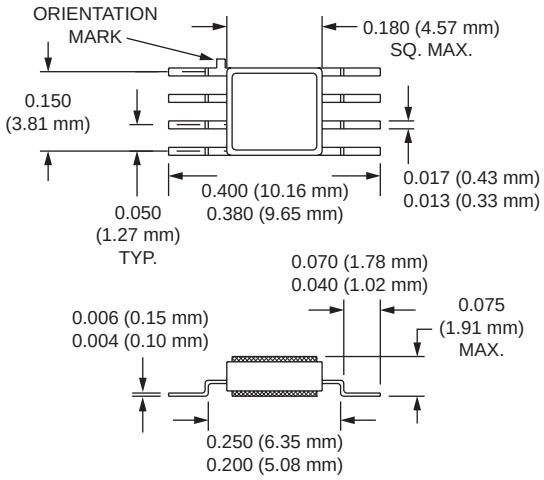
Features

- Low DC Power Consumption
- High Power, T/R Switch
- 8 Lead Hermetic Surface Mount Package
- Capable of Meeting MIL-STD Requirements[5]

Description

The AH002R2-11 is a GaAs IC FET SPDT reflective switch designed for low distortion at medium power levels for T/R switch applications. This switch has a 1 dB compression point of 4 W at 450 MHz and -10 V bias.

-11



Electrical Specifications at 25°C

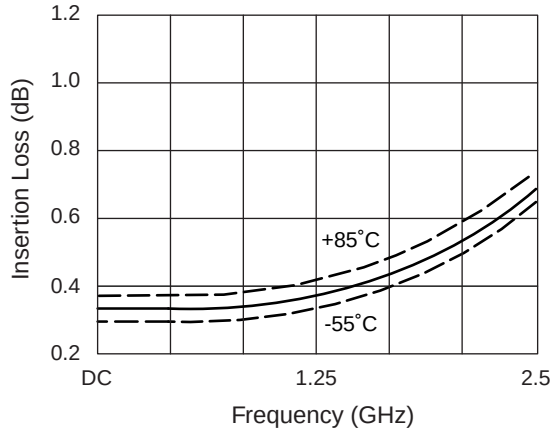
Parameter[1]	Frequency[4]	Min.	Typ.	Max.	Unit
Insertion Loss[2]	DC–1.0 GHz DC–2.0 GHz DC–2.5 GHz		0.3 0.5 0.7	0.4 0.7 0.8	dB dB dB
Isolation	DC–1.0 GHz DC–2.0 GHz DC–2.5 GHz	26 22 20	35 25 22		dB dB dB
VSWR	DC–0.5 GHz DC–1.0 GHz DC–2.5 GHz		1.2:1 1.5:1 1.7:1	1.3:1 1.6:1 1.8:1	

Operating Characteristics at 25°C

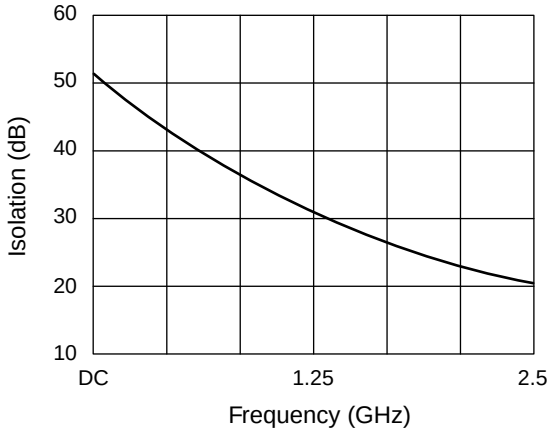
Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Switching Characteristics	Rise, Fall (10/90% or 90/10% RF) On, Off (50% CTL to 90/10% RF) Video Feedthru[3]			3 6 30		ns ns mV
Input Power for 1 dB Compression	0/-5 (0/-10)	≥ 850 MHz 450 MHz		33 (37) 30 (36)		dBm dBm
Intermodulation Intercept Point (IP3)	For Two-tone Input Power 13 dBm	≥ 9 GHz 0.001 GHz		56 42		dBm dBm
Total Harmonic Distortion	0/-5 (0/-10)	850 MHz @ 33 dBm		-55 (-70)		dBc
Control Voltages	V_{Low} = 0 V to -0.2 V @ 20 µA Max. V_{High} = -5 V @ 100 µA to -10 V @ 400 µA Max.					

1. All measurements made in a 50 Ω system, unless otherwise specified.
2. Insertion loss changes by 0.003 dB/°C.
3. Video feedthru measured with 1 ns risetime pulse and 500 MHz bandwidth.
4. DC = 300 kHz
5. See Quality/Reliability section.

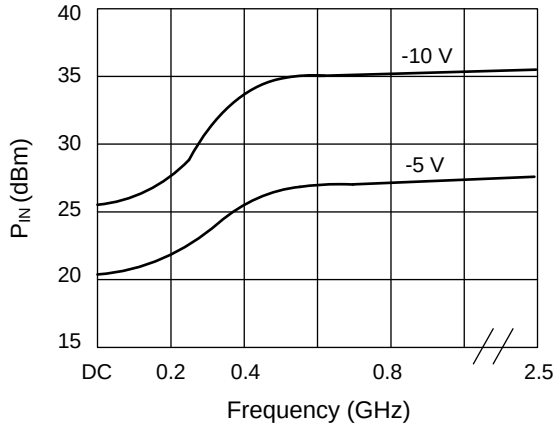
Typical Performance Data



Insertion Loss vs. Frequency



Isolation vs. Frequency



P_{IN} at 1 dB Compression vs. Frequency and Control Voltage

Absolute Maximum Ratings

Characteristic	Value
RF Input Power (RF In)	5 W > 500 MHz 0/-12 1.5 W @ 50 MHz 0/-12
Control Voltage (V_C)	+0.2 V, -12.0 V
Operating Temperature (T_{OP})	-55°C to +125°C
Storage Temperature (T_{ST})	-65°C to +150°C
Thermal Resistance (Θ_{JC})	35°C/W

Truth Table

V_1	V_2	J_1–J_2	J_1–J_3
0	-10 (-5)	Insertion Loss	Isolation
-10 (-5)	0	Isolation	Insertion Loss

Pin Out