SiI9127A HDMI Receiver with Deep Color Outputs

Data Brief

Document # SiI-DB-1059-A03

September 2010

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Introduction

The SiI9127A HDMI Receiver with Deep Color Outputs is a 2-port receiver that allows DTVs that can display 10/12-bit color depth to provide the highest quality protected digital audio and video over a single cable. The SiI9127A receiver can receive Deep Color video up to 12-bit, 1080p at 60 Hz. Efficient color space conversion receives RGB or YCbCr video data and sends either standard-definition or high-definition RGB or YCbCr formats.

The SiI9127A receiver supports the extended gamut YCC or xvYCC color space described in the IEC 61966-2-4 Specification, which supports approximately 1.8 times the number of colors as the RGB color space. The xvYCC color space also makes full use of the range provided by the standard 8-bit resolution per pixel format.

The SiI9127A receiver is pre-programmed with High-bandwidth Digital Content Protection (HDCP) keys and contains an integrated HDCP decryption engine for receiving protected audio and video content. This set of keys helps reduce programming overhead, lowers manufacturing costs, and provides the highest level of security.

An integrated Extended Display Identification Data (EDID) block stored in non-volatile memory (NVM) can be programmed at the time of manufacture using the local I^2C bus. On-board RAM can also be loaded through the I^2C bus with EDID data from the system micro-controller during initialization if the EDID content of the NVM is not used. The EDID is reflected on the two HDMI ports through the DDC bus. The device allows different EDID formats to be mixed in an application. Having the flexibility to provide EDID content from the sources described above or from external ROM can eliminate up to two EDID ROMs and save board space.

Flexible power management provides extremely low standby power consumption. Standby power can be supplied from an HDMI 5 V signal or from a separate standby power pin. If the NVM stores the EDID, only the 5 V power from the source device is needed to read the EDID.

Inputs

- two HDMI/DVI-compatible ports
- the TMDS™ core runs at 25–225 MHz
- dynamic cable equalization automatically detects the equalization required for the incoming signal

Digital Video Output

- xvYCC to extended RGB
- 36-bit RGB/YCbCr 4:4:4
- 16/20/24-bit YCbCr 4:2:2
- 8/10/12-bit YCbCr 4:2:2 (ITU BT.656)
- true 12-bit accurate output data using an internal 14-bit wide processing path
- drive strength is programmable from 2 mA to 14 mA

Digital Audio Interface

- sends and receives up to two channels of uncompressed digital audio at the rate of 192 kHz
- I^2S output with one data signal for stereo formats
- S/PDIF output supports PCM, Dolby Digital, DTS digital audio transmission with a 32–192 kHz Fs sample rate
- intelligent audio mute capability avoids pops and noise with automatic soft mute and unmute
- IEC60958 or IEC61937 compatible

Consumer Electronic Control

- Consumer Electronics Control (CEC) interface incorporates an HDMI CEC I/O
- an integrated CEC Programming Interface (CPI) relieves the burden of the microcontroller having to write low-level commands
- Automatic Feature Abort response for unsupported commands
- Automatic Message Retry on transmit

Package

- 14 mm x 14 mm 128-pin TQFP package with ePad™

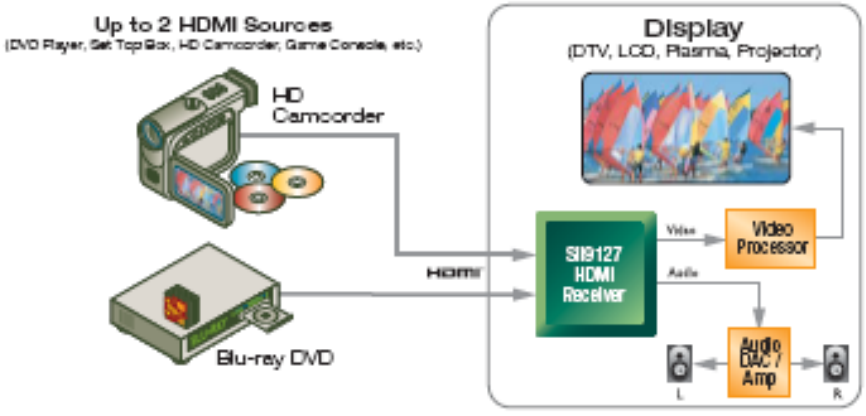


Figure 1. Digital Television System Diagram

System Applications

The SiI9127A receiver is designed for digital televisions that require support for HDMI Deep Color. The device allows receipt of 10/12-bit color depth up to 1080p resolutions. A single receiver chip provides two HDMI input ports. The video output interfaces to a video processor and the audio output can interface directly to an audio DAC or an audio DSP for further processing as shown in Figure 1.

Comparing SiI9127A with SiI9125, SiI9135A, SiI9223A and SiI9233A

Table 1 summarizes the functional differences among the SiI9127A, SiI9125, SiI9135A, SiI9223A and the SiI9233A receivers.

Table 1. Summary of New Features

Feature	SiI9125	SiI9127A	SiI9135A	SiI9223A	SiI9233A
HDMI Input Connections					
TMDS Input Ports	2	2	2	4	4
Color Depth	8/10/12-bit	8/10/12-bit	8/10/12-bit	8/10/12-bit	8/10/12-bit
DDC Input Ports	2	2	2	4	4
Maximum TMDS Input Clock	225 MHz	225 MHz	225 MHz	225 MHz	225 MHz
Video Output					
Digital Video Output Ports	1	1	1	1	1
Maximum Output Pixel Clock	165 MHz.	165 MHz.	165 MHz.	165 MHz.	165 MHz.
Maximum Output Bus Width	36	36	36	36	36
Audio Formats					
S/PDIF Output Ports	1	1	1	1	1
I^2S Output	2 channel	2 channel	8 channel	2 channel	8 channel
DSD Output	2 channel	NA	6 channel	NA	8 channel
High Bit Rate Audio Support Compressed DTS-HD and Dolby True-HD	No	No	Yes	No	Yes
Maximum Audio Sample Rate (Fs)	192 kHz	192 kHz	192 kHz	192 kHz	192 kHz
Video Processing					
Color Space Converter	RGB to/from YCbCr	RGB to/from YCbCr xvYCC to RGB	RGB to/from YCbCr	RGB to/from YCbCr xvYCC to RGB	RGB to/from YCbCr xvYCC to RGB
Pixel Clock Divider	÷ 4, ÷ 2	÷ 4, ÷ 2	÷ 4, ÷ 2	÷ 4, ÷ 2	÷ 4, ÷ 2
Digital Video Bus Mapping	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins
Other Features					
CEC	No	Yes	No	Yes	Yes
EDID	No	NVRAM	No	NVRAM	NVRAM
HDCP Repeater Support	No	No	Yes	No	Yes
Interlaced Format Detection Pin	Yes	Yes	Yes	Yes	Yes
Package	144-pin TQFP ePad	128-pin TQFP ePad	144-pin TQFP ePad	144-pin TQFP ePad	144-pin TQFP ePad

Pin Diagram

Figure 2 shows the SiI9127A pin assignments of the receiver. Pin names are generalized by type for this document. The list below the diagram describes the purpose of each type. The package is a 14 mm x 14 mm 128-pin TQFP with an ePad.

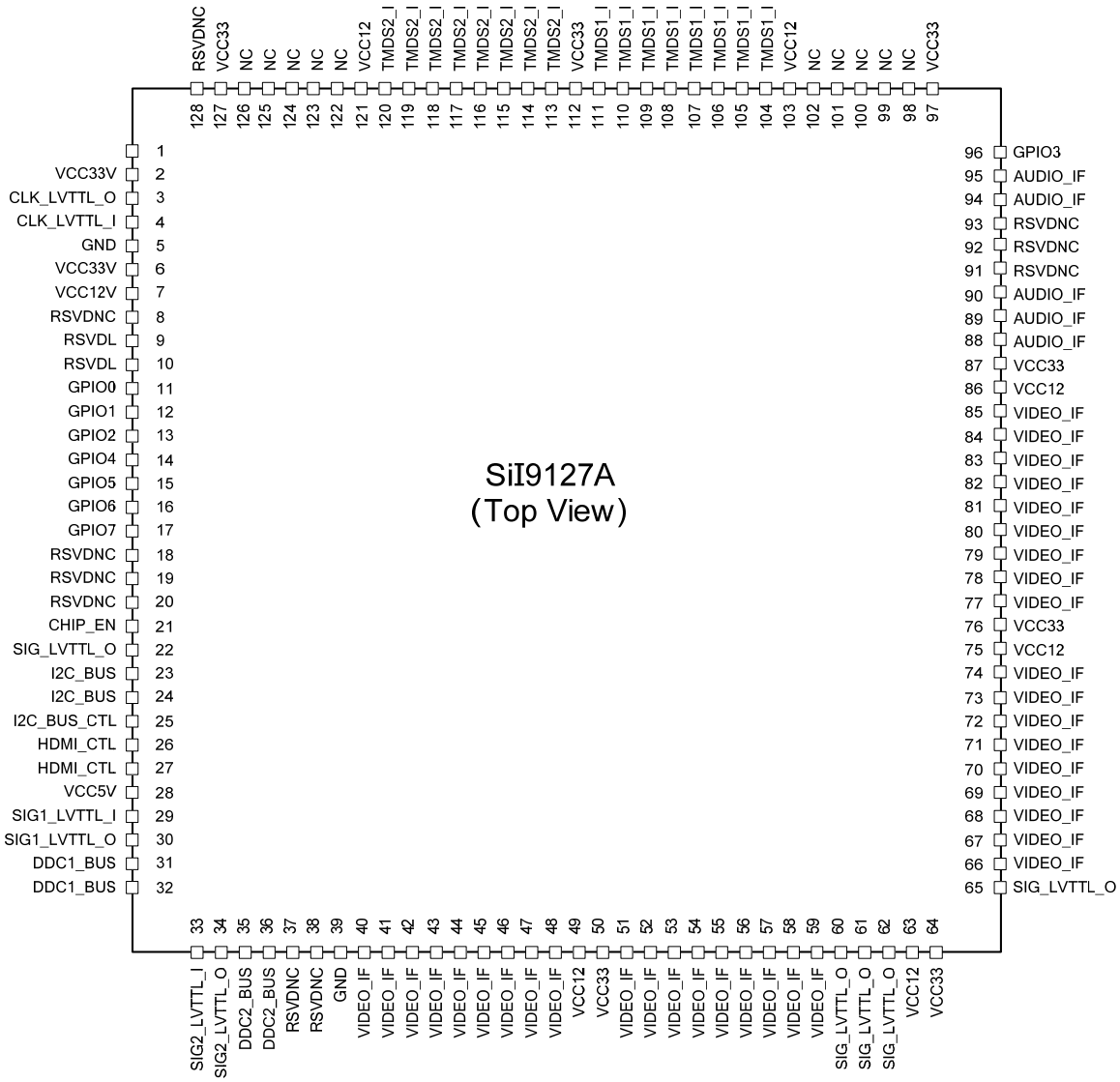


Figure 2. Pin Diagram

Package Information

ePad Requirements

The SiI9127A receiver is packaged in a 128-pin, 14 mm x 14 mm TQFP package with an ExposedPad™ (ePad™) that is used for the electrical ground of the device and for improved thermal transfer characteristics. The ePad dimensions are 4.445 mm x 4.0604 mm ±0.15 mm. Soldering the ePad to the ground plane of the PCB is ***required*** to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground. A clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical shorts.

The thermal land area on the PCB may use thermal vias to improve heat removal from the package. These thermal vias also double as the ground connections of the chip and must attach internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package. For optimum thermal performance, the via diameter should be 12 mils to 13 mils (0.30 mm to 0.33 mm) and the via barrel should be plated with 1-ounce copper to plug the via. This design helps to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off when mounting the device also needs to be considered. For a nominal stand-off of approximately 0.1 mm the stencil thickness of 5 mils to 8 mils should provide a good solder joint between the ePad and the thermal land.

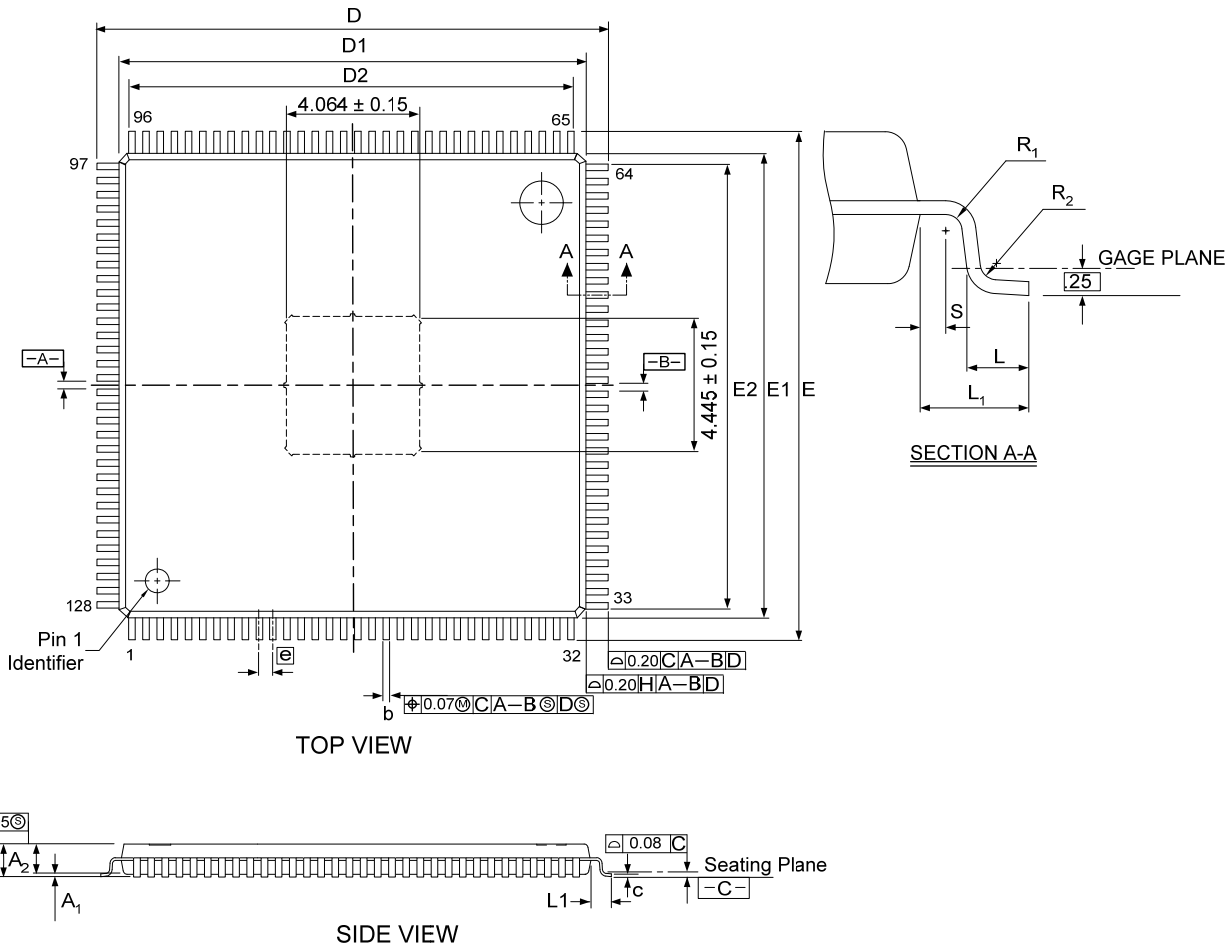
Figure 3 on the next page shows the package dimensions of the SiI9127A receiver.

PCB Layout Guidelines

Refer to Silicon Image application note *PCB Layout Guidelines: Designing with Exposed Pads* for basic PCB design guidelines when designing with thermally enhanced packages using the exposed pad. This application note is intended for use by PCB layout designers.

Package Dimensions

Figure 3 shows the layout and dimensions of the 128-pin TQFP package. Package drawings are not to scale.



JEDEC Package Code MS-026-AFB

Item	Description	Typ	Max
A	Thickness	1.10	1.20
A1	Stand-off	0.10	0.15
A2	Body thickness	1.00	1.05
D	Footprint	16.00	
E	Footprint	16.00	
D1	Body size	14.00	
E1	Body size	14.00	
D2	Lead Row Width	12.40	
E2	Lead Row Width	12.40	

Item	Description	Typ	Max
b	Lead width	0.16	0.23
c	Lead thickness	—	0.20
e	Lead pitch	0.40	
L	Lead foot length	0.60	0.75
L1	Lead length	1.00	

Dimensions are in millimeters.

Overall thickness A = A1 + A2.

Figure 3. 128-Pin TQFP Package Diagram

Marking Specification

Drawing is not to scale and pin count shown is representative. Refer to the specifics in Figure 3 on page 5.

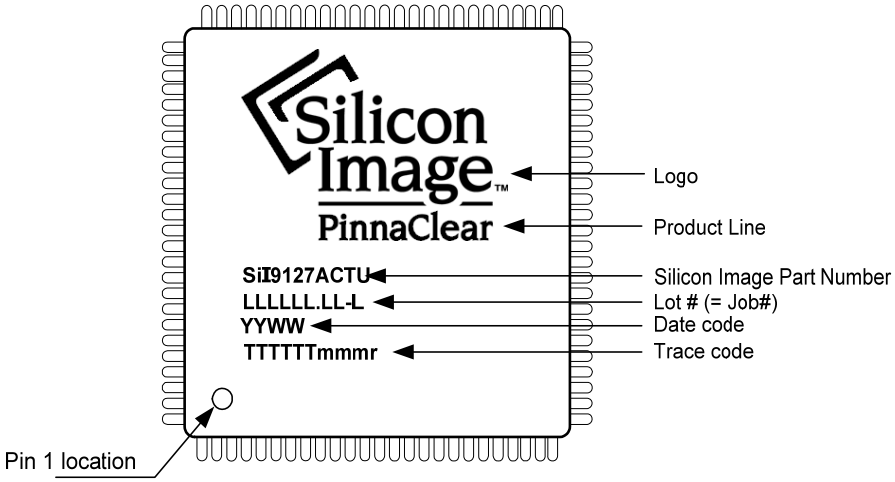


Figure 4. Marking Diagram

Ordering Information

Production Part Numbers:

TMDS Input Clock Range	Part Number
25–225 MHz	SiI9127ACTU

The universal package may be used in lead-free and ordinary process lines.

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