## FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **DOC™ (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation**
- **Dynamic Drive Capability Is Equivalent to Standard Outputs With $I_{OH}$ and $I_{OL}$ of ±24 mA at 2.5-V $V_{CC}$**
- **Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Thin Very Small-Outline (DGV) Packages**

## DESCRIPTION/ORDERING INFORMATION

A Dynamic Output Control (DOC) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical $V_{OL}$ vs $I_{OL}$ and $V_{OH}$ vs $I_{OH}$ curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC) Circuitry Technology and Applications*, literature number SCEA009.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | TSSOP – DGG | Tape and reel | SN74AVC16374DGGR | AVC16374 |
| | TVSOP – DGV | Tape and reel | SN74AVC16374DGVR | CVA374 |
| | VFBGA – GQL | Tape and reel | SN74AVC16374GQLR | CVA374 |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

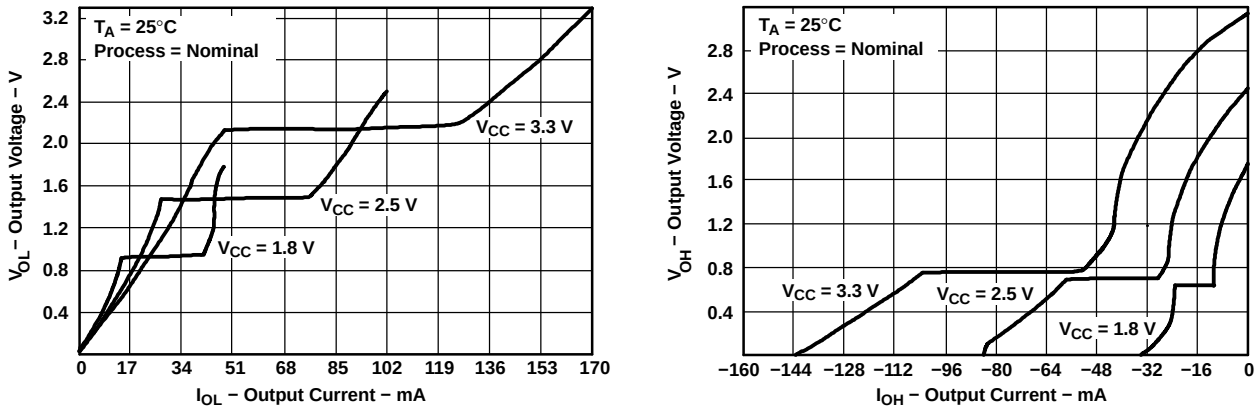


**Figure 1. Output Voltage vs Output Current**

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## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This 16-bit edge-triggered D-type flip-flop is operational at 1.2-V to 3.6-V $V_{CC}$, but is designed specifically for 1.65-V to 3.6-V $V_{CC}$ operation.

The SN74AVC16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels at the data (D) inputs. $\overline{OE}$ can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

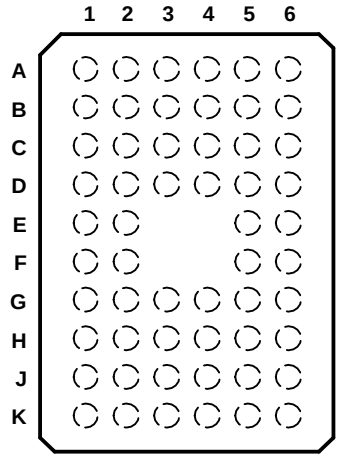
$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using Ioff. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74AVC16374 is characterized for operation from –40°C to 85°C.

**GQL PACKAGE**
**(TOP VIEW)**

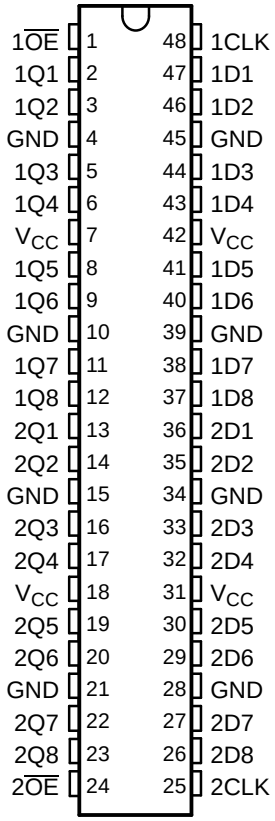



**TERMINAL ASSIGNMENTS(1)**

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | 1$\overline{OE}$ | NC | NC | NC | NC | 1CLK |
| **B** | 1Q2 | 1Q1 | GND | GND | 1D1 | 1D2 |
| **C** | 1Q4 | 1Q3 | $V_{CC}$ | $V_{CC}$ | 1D3 | 1D4 |
| **D** | 1Q6 | 1Q5 | GND | GND | 1D5 | 1D6 |
| **E** | 1Q8 | 1Q7 | | | 1D7 | 1D8 |
| **F** | 2Q1 | 2Q2 | | | 2D2 | 2D1 |
| **G** | 2Q3 | 2Q4 | GND | GND | 2D4 | 2D3 |
| **H** | 2Q5 | 2Q6 | $V_{CC}$ | $V_{CC}$ | 2D6 | 2D5 |
| **J** | 2Q7 | 2Q8 | GND | GND | 2D8 | 2D7 |
| **K** | 2$\overline{OE}$ | NC | NC | NC | NC | 2CLK |

(1) NC - No internal connection

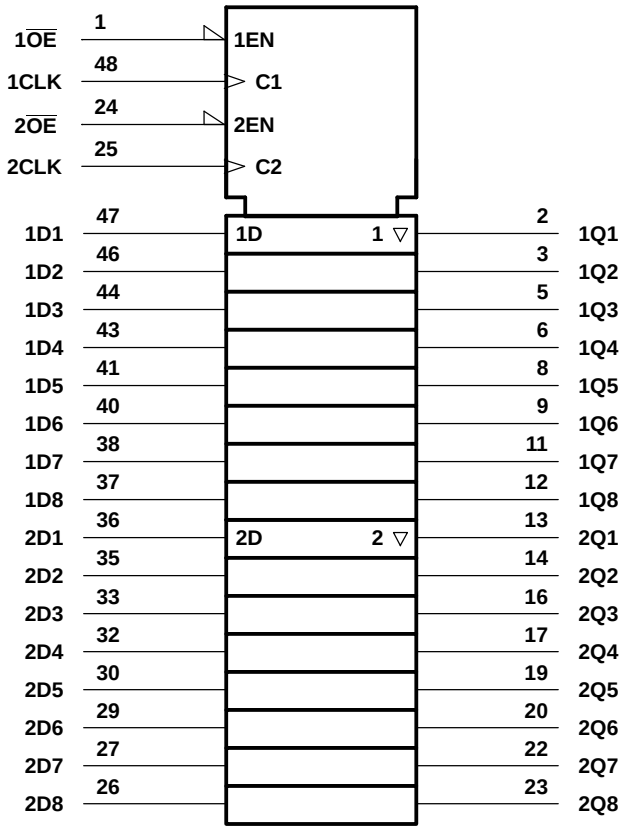
**DGG OR DGV PACKAGE**
**(TOP VIEW)**




**FUNCTION TABLE**
**(EACH 8-BIT FLIP FLOP)**

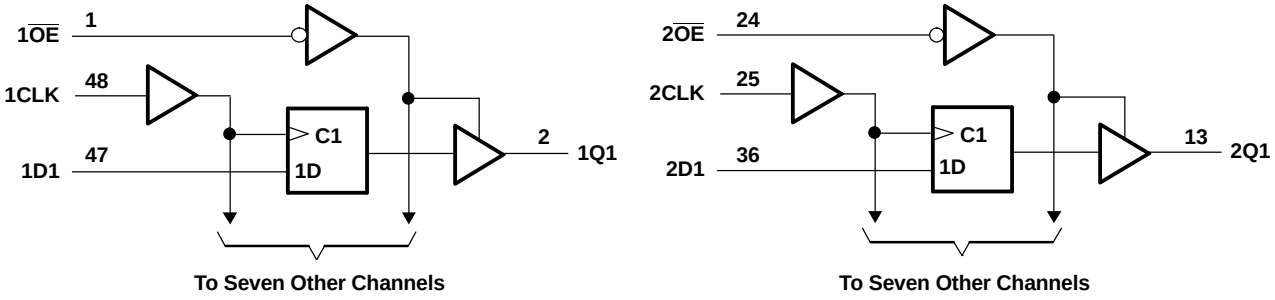
| INPUTS | | | OUTPUT Q |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | $Q_0$ |
| H | X | X | Z |

## LOGIC SYMBOL(1)




(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## LOGIC DIAGRAM (POSITIVE LOGIC)



## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 4.6 | V |
| $V_I$ | Input voltge range(2) | | –0.5 | 4.6 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 4.6 | V |
| $V_O$ | Voltage range applied to any output in the high or low state(2)(3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through each $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance(4) | DGG package | | 70 | °C/W |
| | | DGV package | | 58 | |
| | | GQL package | | 42 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current ratings is observed.
(4) The package thermal impedance is calculated in accordance with JESD 51.

## Recommended Operating Conditions[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.4 | 3.6 | V |
| | | Data retention only | 1.2 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.2 V | $V_{CC}$ | | V |
| | | $V_{CC}$ = 1.4 V to 1.6 V | $0.65 \times V_{CC}$ | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | $0.65 \times V_{CC}$ | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.2 V | | GND | V |
| | | $V_{CC}$ = 1.4 V to 1.6 V | | $0.35 \times V_{CC}$ | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | $0.35 \times V_{CC}$ | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | 3.6 | V |
| $V_O$ | Output voltage | Active state | 0 | $V_{CC}$ | V |
| | | 3-state | 0 | 3.6 | |
| $I_{OHS}$ | Static high-level output current[2] | $V_{CC}$ = 1.4 V to 1.6 V | | –2 | mA |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | –4 | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | –8 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | –12 | |
| $I_{OLS}$ | Static low-level output current[2] | $V_{CC}$ = 1.4 V to 1.6 V | | 2 | mA |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | 4 | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 8 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 1.4 V to 3.6 V | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Dynamic drive capability is equivalent to standard outputs with $I_{OH}$ and $I_{OL}$ of ±24 mA at 2.5-V $V_{CC}$. See Figure 1 for $V_{OL}$ vs $I_{OL}$ and $V_{OH}$ vs $I_{OH}$ characteristics. Refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OHS}$ = –100 μA | | 1.4 V to 3.6 V | $V_{CC}$ – 0.2 | | | V |
| | | $I_{OHS}$ = –2 mA, | $V_{IH}$ = 0.91 V | 1.4 V | 1.05 | | | |
| | | $I_{OHS}$ = –4 mA, | $V_{IH}$ = 1.07 V | 1.65 V | 1.2 | | | |
| | | $I_{OHS}$ = –8 mA, | $V_{IH}$ = 1.7 V | 2.3 V | 1.75 | | | |
| | | $I_{OHS}$ = –12 mA, | $V_{IH}$ = 2 V | 3 V | 2.3 | | | |
| $V_{OL}$ | | $I_{OLS}$ = 100 μA | | 1.4 V to 3.6 V | | | 0.2 | V |
| | | $I_{OLS}$ = 2 mA, | $V_{IL}$ = 0.49 V | 1.4 V | | | 0.4 | |
| | | $I_{OLS}$ = 4 mA, | $V_{IL}$ = 0.57 V | 1.65 V | | | 0.45 | |
| | | $I_{OLS}$ = 8 mA, | $V_{IL}$ = 0.7 V | 2.3 V | | | 0.55 | |
| | | $I_{OLS}$ = 12 mA, | $V_{IL}$ = 0.8 V | 3 V | | | 0.7 | |
| $I_I$ | | $V_I$ = $V_{CC}$ or GND | | 3.6 V | | | ±2.5 | μA |
| $I_{off}$ | | $V_I$ or $V_O$ = 3.6 V | | 0 | | | ±10 | μA |
| $I_{OZ}$ | | $V_O$ = $V_{CC}$ or GND | | 3.6 V | | | ±10 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 3.6 V | | | 40 | μA |
| $C_i$ | Control inputs | $V_I$ = $V_{CC}$ or GND | | 2.5 V | | 3 | | pF |
| | | | | 3.3 V | | 3 | | |
| | Data inputs | $V_I$ = $V_{CC}$ or GND | | 2.5 V | | 2.5 | | |
| | | | | 3.3 V | | 2.5 | | |
| $C_o$ | Outputs | $V_O$ = $V_{CC}$ or GND | | 2.5 V | | 6.5 | | pF |
| | | | | 3.3 V | | 6.5 | | |

(1) Typical values are measured at $V_{CC}$ = 2.5 V and 3.3 V, $T_A$ = 25°C.

## Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

| | | $V_{CC}$ = 1.2 V | | $V_{CC}$ = 1.5 V ± 0.1 V | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | | | | 160 | | 200 | | 200 | MHz |
| $t_w$ | Pulse duration, CLK high or low | | | | | 3.1 | | 2.5 | | 2.5 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 4.1 | | 2.7 | | 1.9 | | 1.4 | | 1.4 | | ns |
| $t_h$ | Hold time, data after CLK↑ | 1.7 | | 1.3 | | 1.2 | | 1.1 | | 1.1 | | ns |

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2 through Figure 5)

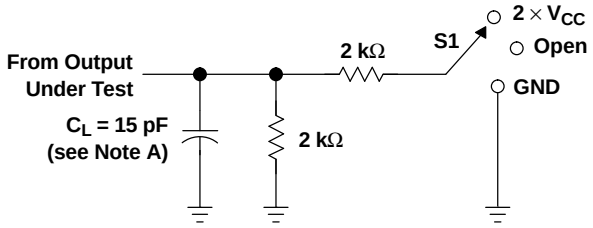
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.2 V | $V_{CC}$ = 1.5 V ± 0.1 V | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | | | | 160 | | 200 | | 200 | | MHz |
| $t_{pd}$ | CLK | Q | 7.3 | 1.5 | 8.4 | 1.2 | 6.7 | 0.8 | 4.1 | 0.7 | 3.3 | ns |
| $t_{en}$ | $\overline{OE}$ | Q | 7.4 | 1.6 | 8.5 | 1.6 | 6.7 | 0.9 | 4.3 | 0.7 | 3.4 | ns |
| $t_{dis}$ | $\overline{OE}$ | Q | 8.4 | 2.5 | 9.4 | 2.3 | 7.8 | 1 | 4.2 | 1.5 | 3.9 | ns |

## Operating Characteristics

$T_A$ = 25°C

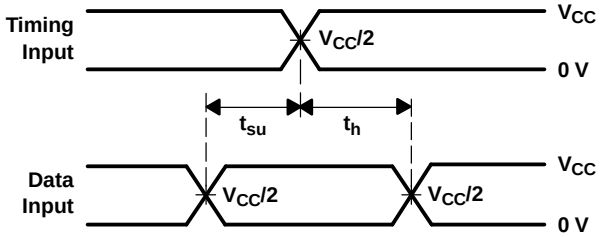
| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 0, f = 10 MHz | 74 | 81 | 89 | pF |
| | | Outputs disabled | | 52 | 57 | 63 | |

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 1.2 V AND 1.5 V ± 0.1 V

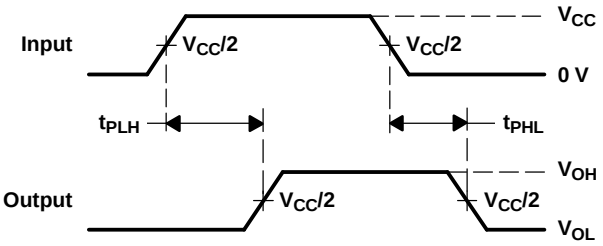



LOAD CIRCUIT

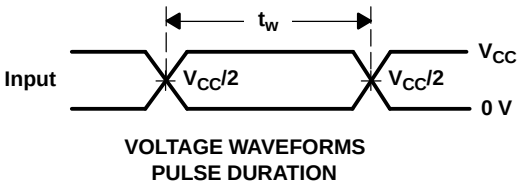
| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



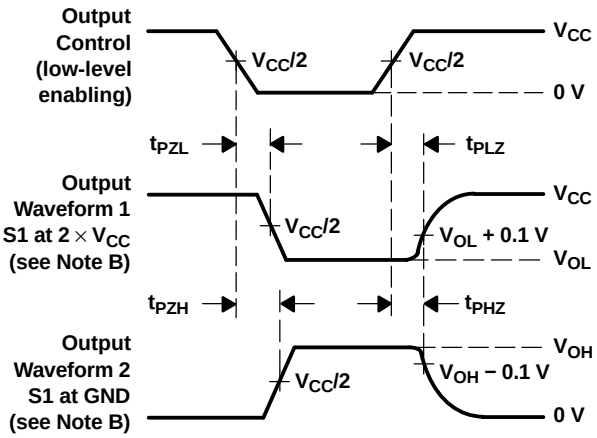

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

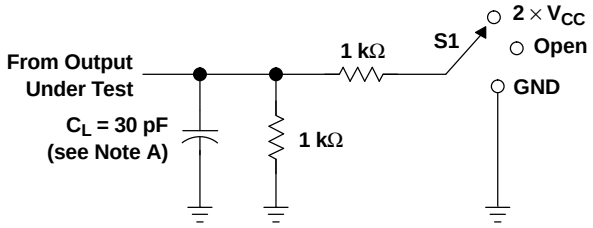



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

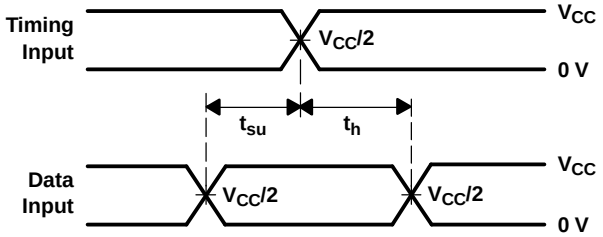
**Figure 2. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 1.8 V ± 0.15 V

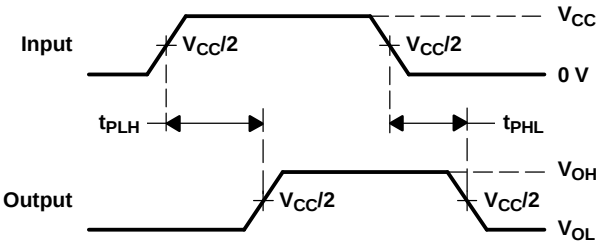



LOAD CIRCUIT

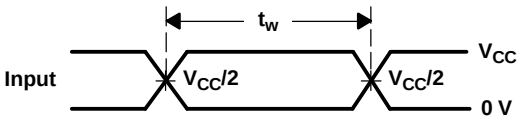
| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



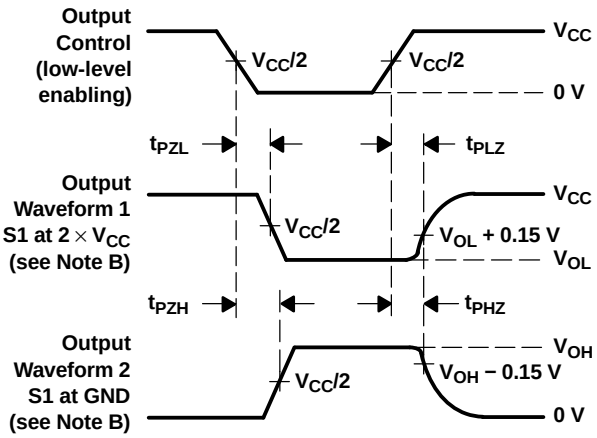

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

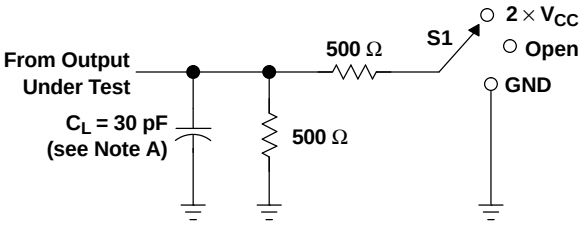



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

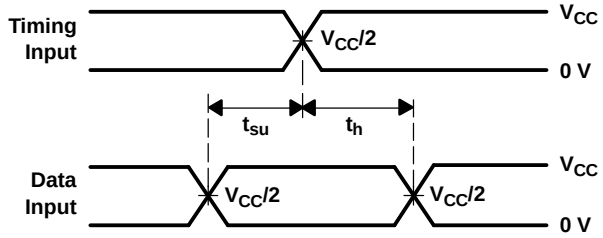
**Figure 3. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V

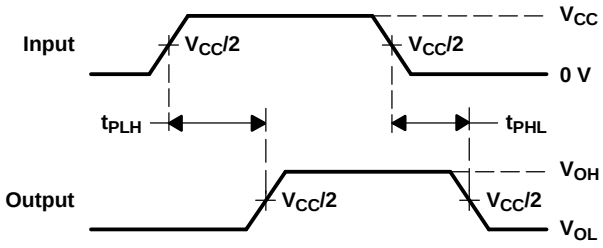



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

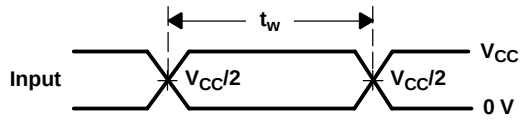
LOAD CIRCUIT



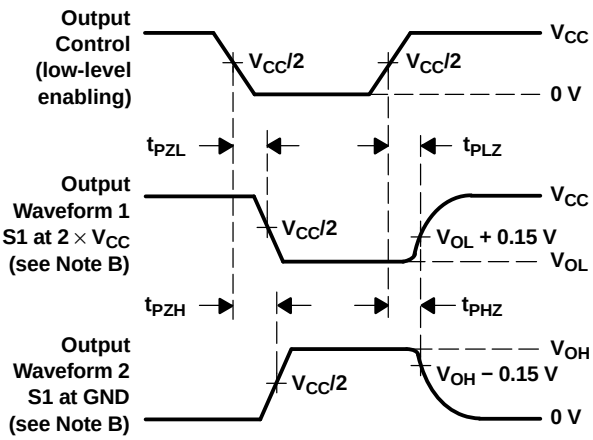

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

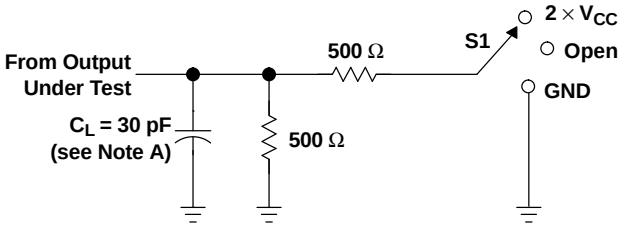



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

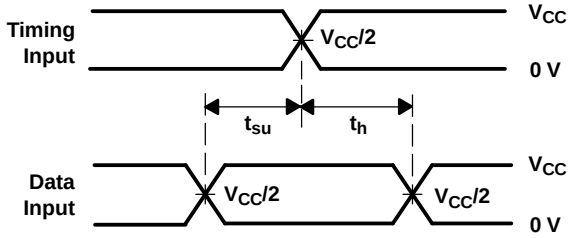
**Figure 4. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 3.3 V ± 0.3 V

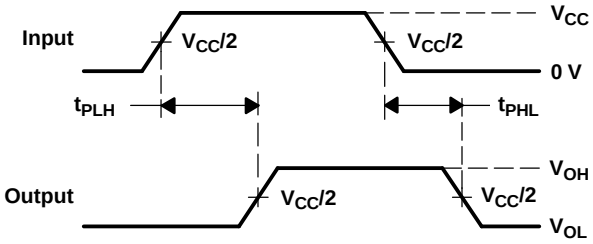



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

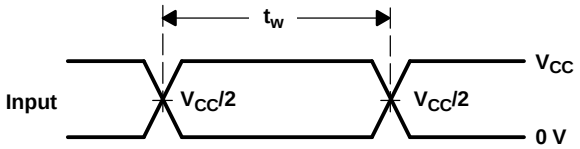
LOAD CIRCUIT



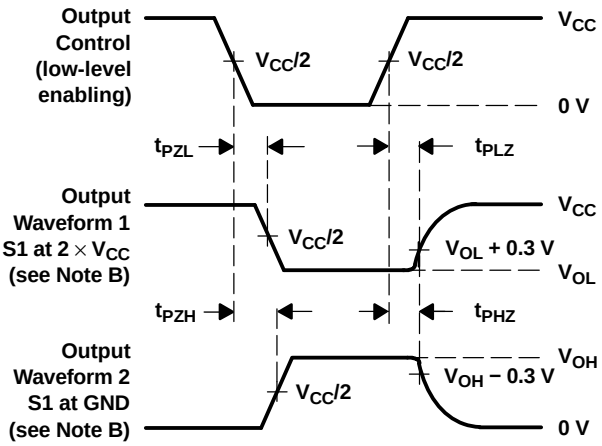

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 5. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| 74AVC16374DGGRE4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| 74AVC16374DGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| 74AVC16374DGVRE4 | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| 74AVC16374DGVRG4 | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AVC16374DGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AVC16374DGVR | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AVC16374GQLR | OBSOLETE | BGA MICROSTAR JUNIOR | GQL | 56 | | TBD | Call TI | Call TI | |
| SN74AVC16374ZQLR | ACTIVE | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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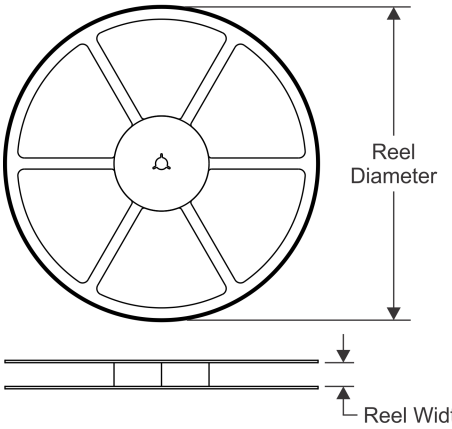
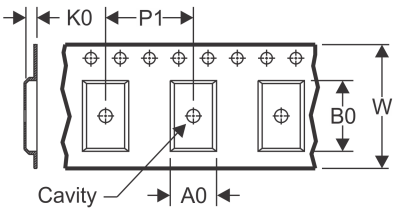
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

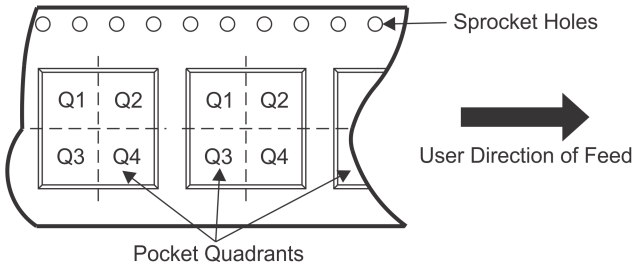



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

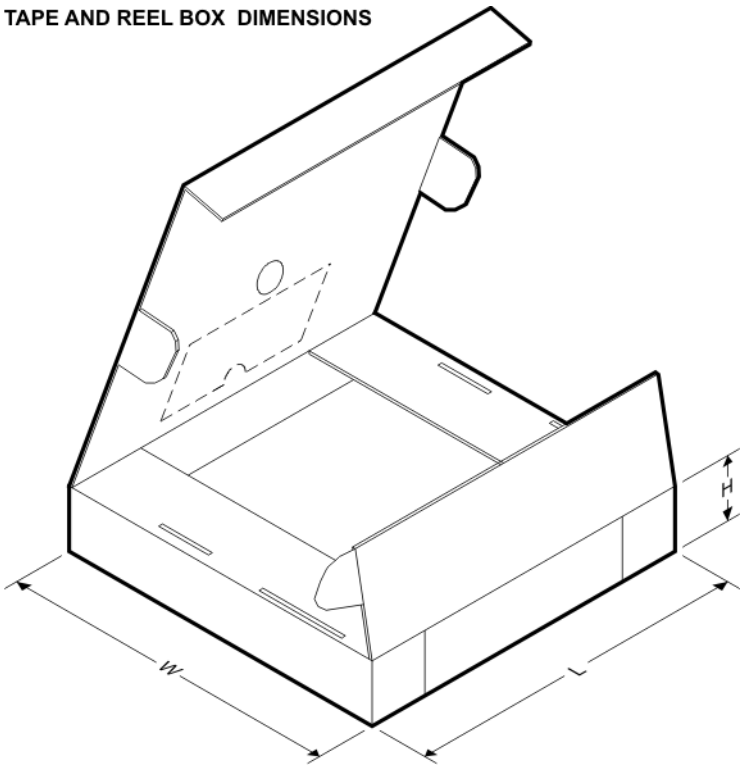
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AVC16374DGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 15.8 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74AVC16374DGVR | TVSOP | DGV | 48 | 2000 | 330.0 | 16.4 | 7.1 | 10.2 | 1.6 | 12.0 | 16.0 | Q1 |
| SN74AVC16374ZQLR | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 330.0 | 16.4 | 4.8 | 7.3 | 1.5 | 8.0 | 16.0 | Q1 |

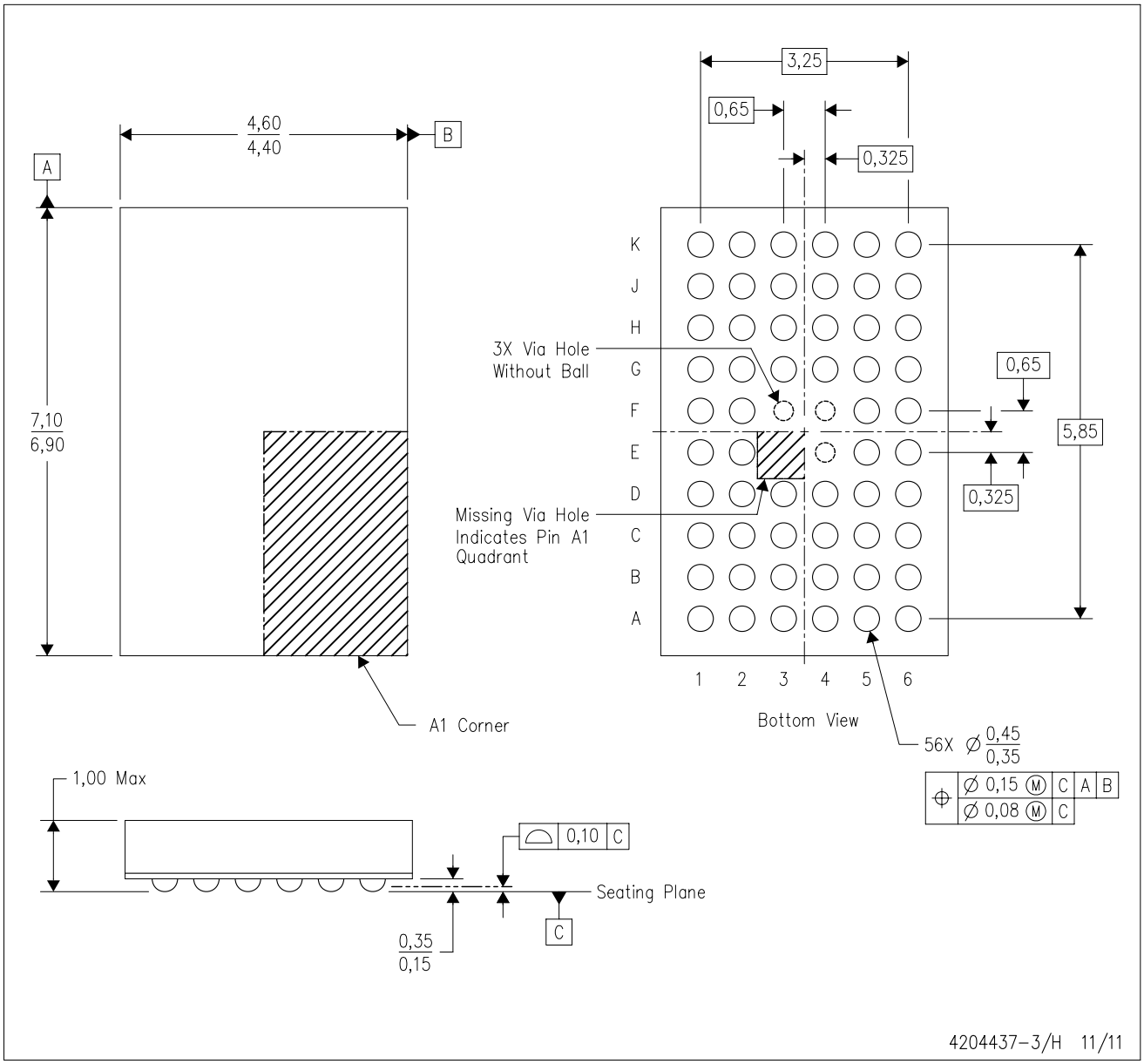
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AVC16374DGGR | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AVC16374DGVR | TVSOP | DGV | 48 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74AVC16374ZQLR | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 333.2 | 345.9 | 28.6 |

ZQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–285 variation BA–2.
D. This package is Pb–free. Refer to the 56 GQL package (drawing 4200583) for tin–lead (SnPb).

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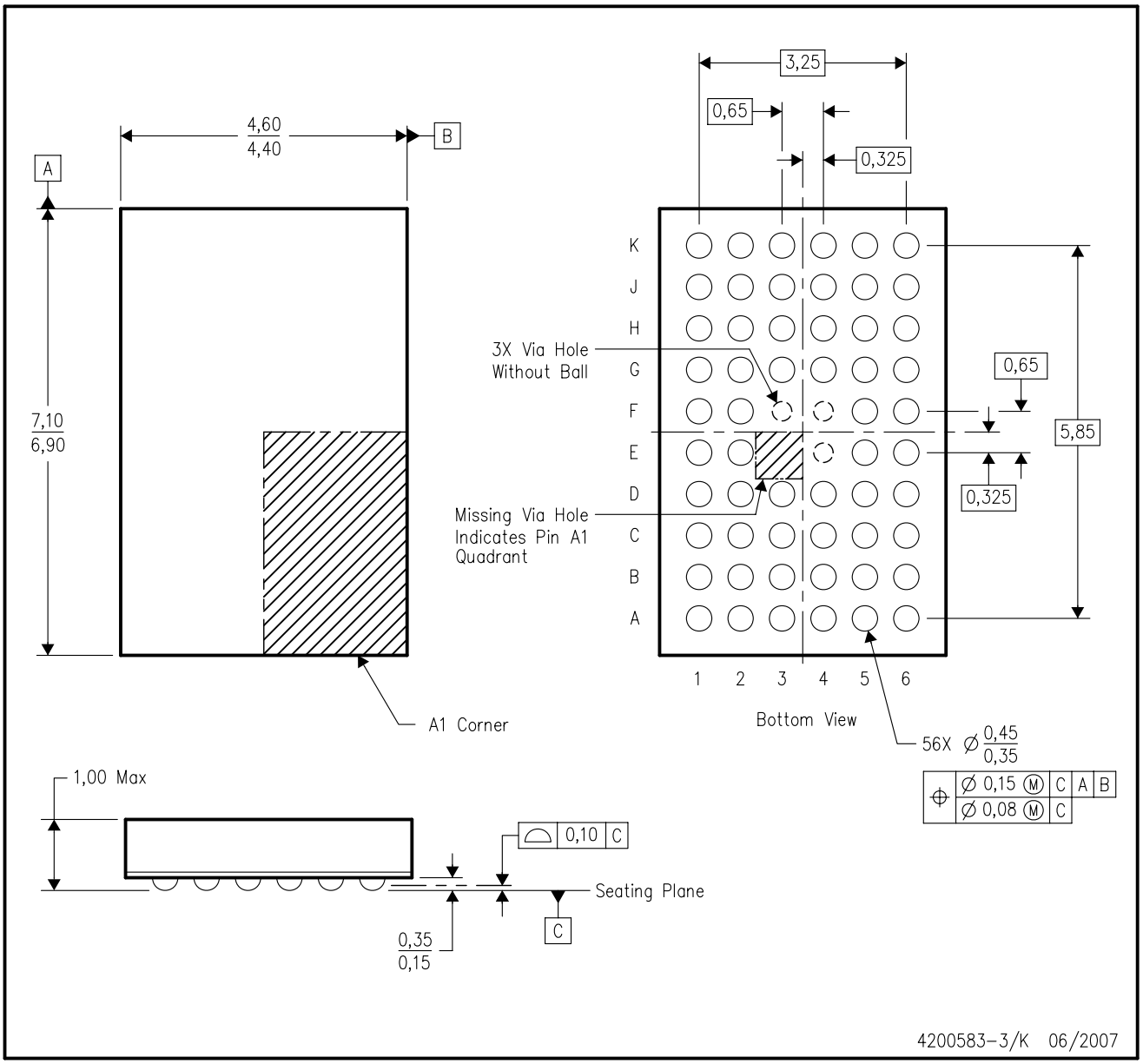
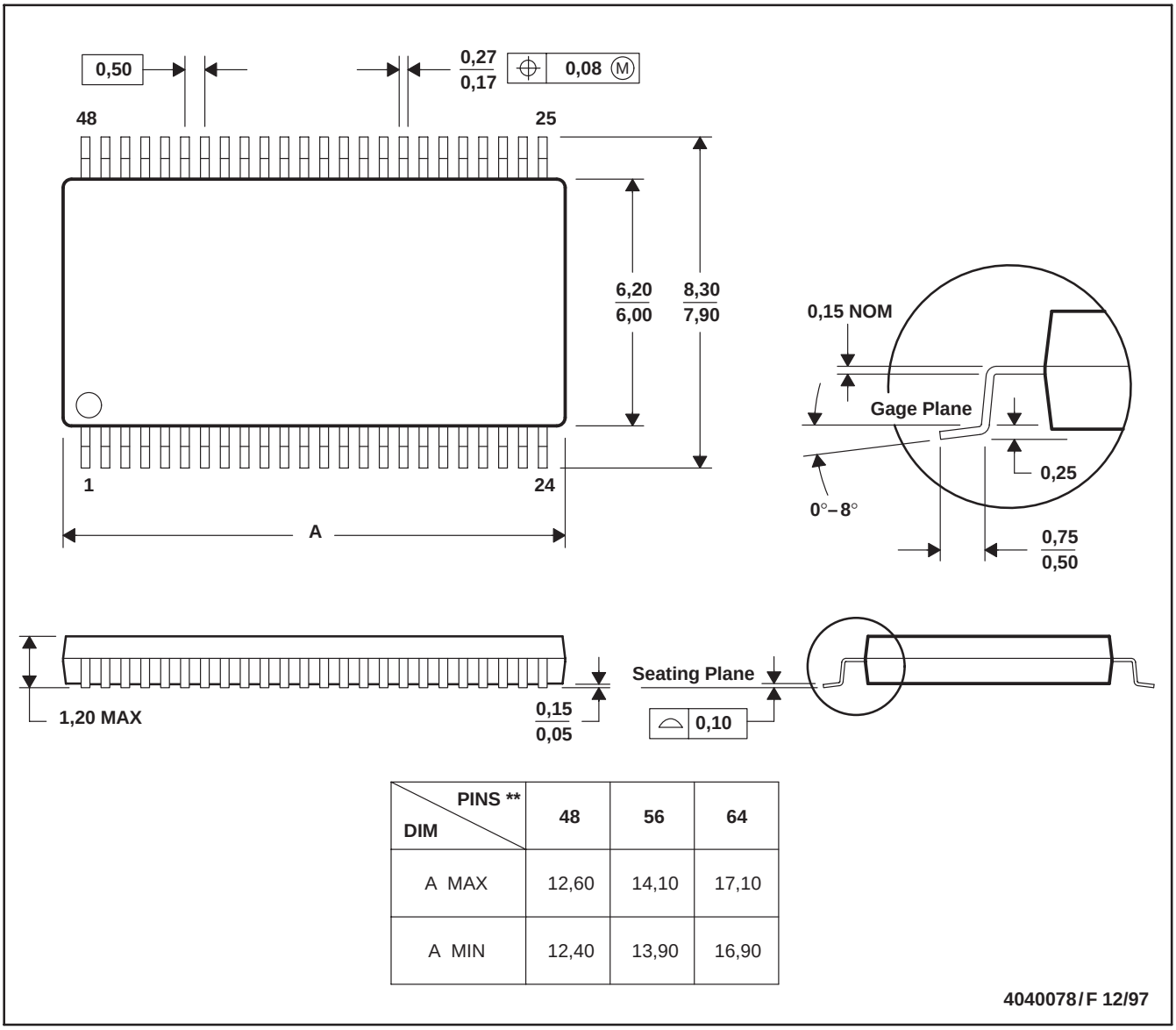
## GQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–285 variation BA–2.
D. This package is tin–lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead–free.

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**




| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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