

AZ10E111

AZ100E111

ECL/PECL 1:9 Differential Clock Driver

FEATURES

- Low Skew
- Differential Design
- Clock Enable
- V_{BB} Output
- Operating Range of 4.2V to 5.46V
- 75k Ω Internal Input Pulldown Resistors
- Direct Replacement for ON Semiconductor MC10E111 & MC100E111

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING
PLCC 28	AZ10E111FN	AZM10E111
PLCC 28 T&R	AZ10E111FNR2	AZM10E111
PLCC 28	AZ100E111FN	AZM100E111
PLCC 28 T&R	AZ100E111FNR2	AZM100E111

DESCRIPTION

The AZ10/100E111 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. The IN signal is fanned-out to nine identical differential outputs. An Enable input is also provided. A HIGH disables the device by forcing all Q outputs LOW and all \bar{Q} outputs HIGH.

The AZ100E111 provides a V_{BB} output for single-ended use or a DC bias reference for AC coupling to the device. For single-ended input applications, the V_{BB} reference should be connected to one side of the IN/ \bar{IN} differential input pair. The input signal is then fed to the other IN/ \bar{IN} input. The V_{BB} pin should be used only as a bias for the E111 as its sink/source capability is limited. When used, the V_{BB} pin should be bypassed to ground via a 0.01 μ F capacitor.

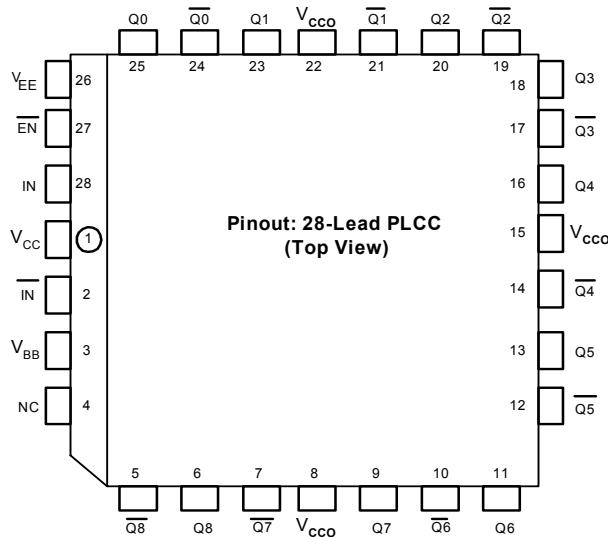
The device is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within-device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot-to-lot. The net result is a dependable, low skew device.

To ensure that the tight skew specification is met, both sides of the differential output must be terminated into 50Ω , even if only one side is used. In most applications all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same V_{CC0}) as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10-20ps) of the output(s) being used that, while not being catastrophic to most designs, will mean a loss of skew margin.

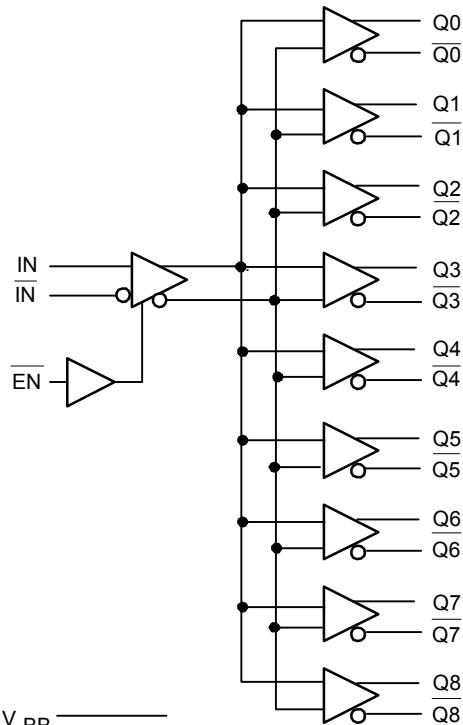
NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.

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LOGIC SYMBOL



PIN DESCRIPTION

PIN	FUNCTION
IN, IN̄	Differential Input Pair
EN	Enable
Q0, Q0̄ - Q8, Q8̄	Differential Outputs
V _{BB}	V _{BB} Output
V _{CC} , V _{CCO}	Positive Supply
V _{EE}	Negative Supply

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating			Unit
		Min	Typ	Max	
V _{CC}	PECL Power Supply (V _{EE} = 0V)	0	to +8.0		Vdc
V _I	PECL Input Voltage (V _{EE} = 0V)	0	to +6.0		Vdc
V _{EE}	ECL Power Supply (V _{CC} = 0V)	-8.0	to 0		Vdc
V _I	ECL Input Voltage (V _{CC} = 0V)	-6.0	to 0		Vdc
I _{OUT}	Output Current --- Continuous		50		
	--- Surge		100		
T _A	Operating Temperature Range		-40	to +85	°C
T _{STG}	Storage Temperature Range		-65	to +150	°C

10K ECL DC Characteristics (V_{EE} = -4.94V to -5.46V, V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max										
V _{OH}	Output HIGH Voltage ¹	-1080		-890	-1020		-840	-980		-810	-910		-720	mV
V _{OL}	Output LOW Voltage ¹	-1950		-1650	-1950		-1630	-1950		-1630	-1950		-1595	mV
V _{IH}	Input HIGH Voltage	-1230		-890	-1170		-840	-1130		-810	-1060		-720	mV
V _{IL}	Input LOW Voltage	-1950		-1500	-1950		-1480	-1950		-1480	-1950		-1445	mV
V _{BB}	Reference Voltage	-1430		-1300	-1380		-1270	-1350		-1250	-1310		-1190	mV
I _{IH}	Input HIGH Current			150			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA
I _{EE}	Power Supply Current		48	60		48	60		48	60		48	60	mA

1. Each output is terminated through a 50Ω resistor to V_{CC} - 2V.

AZ10E111**AZ100E111****10K PECL DC Characteristics (V_{EE} = GND, V_{CC} = V_{CCO} = +5.0V)**

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	3920		4110	3980		4160	4020		4190	4090		4280	mV
V _{OL}	Output LOW Voltage ^{1,2}	3050		3350	3050		3370	3050		3370	3050		3405	mV
V _{IH}	Input HIGH Voltage ¹	3770		4110	3830		4160	3870		4190	3940		4280	mV
V _{IL}	Input LOW Voltage ¹	3050		3500	3050		3520	3050		3520	3050		3555	mV
V _{BB}	Reference Voltage ¹	3570		3700	3620		3730	3650		3750	3690		3810	mV
I _{IH}	Input HIGH Current			150			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA
I _{EE}	Power Supply Current		48	60		48	60		48	60		48	60	mA

1. For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.

2. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

100K ECL DC Characteristics (V_{EE} = -4.2V to -5.46V, V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max										
V _{OH}	Output HIGH Voltage ¹	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	-1025	-955	-880	mV
V _{OL}	Output LOW Voltage ¹	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	-1810	-1705	-1620	mV
V _{IH}	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	-1165		-880	mV
V _{IL}	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	-1810		-1475	mV
V _{BB}	Reference Voltage	-1380		-1260	-1380		-1260	-1380		-1260	-1380		-1260	mV
I _{IH}	Input HIGH Current			150			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA
I _{EE}	Power Supply Current		48	60		48	60		48	60		55	69	mA

1. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

100K PECL DC Characteristics (V_{EE} = GND, V_{CC} = V_{CCO} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	3915	3995	4120	3975	4045	4120	3975	4045	4120	3975	4045	4120	mV
V _{OL}	Output LOW Voltage ^{1,2}	3170	3305	3445	3190	3295	3380	3190	3295	3380	3190	3295	3380	mV
V _{IH}	Input HIGH Voltage ¹	3835		4120	3835		4120	3835		4120	3835		4120	mV
V _{IL}	Input LOW Voltage ¹	3190		3525	3190		3525	3190		3525	3190		3525	mV
V _{BB}	Reference Voltage ¹	3620		3740	3620		3740	3620		3740	3620		3740	mV
I _{IH}	Input HIGH Current			150			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA
I _{EE}	Power Supply Current		48	60		48	60		48	60		55	69	mA

1. For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.

2. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

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AC Characteristics ($V_{EE} = 10E(-4.94V \text{ to } -5.46V)$, $100E(-4.2V \text{ to } -5.46V)$; $V_{CC} = V_{CCO} = GND$ or $V_{EE} = GND$; $V_{CC} = V_{CCO} = 10E(+4.94V \text{ to } +5.46V)$, $100E(+4.2V \text{ to } +5.46V)$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max										
t_{PLH} / t_{PHL}	Propagation Delay to Output IN (Diff) ¹	380		680	460		560	480		580	510		610	ps
	IN (SE) ²	280		780	410		610	430		630	460		660	
	Enable ³	400		900	450		850	450		850	450		850	
	Disable ³	400		900	450		850	450		850	450		850	
t_S	Setup Time EN to IN ⁵	250	0		200	0		200	0		200	0		ps
t_H	Hold Time IN to EN ⁶	50	-200		0	-200		0	-200		0	-200		ps
t_R	Release Time EN to IN ⁷	350	100		300	100		300	100		300	100		ps
t_{SKEW}	Within-Device Skew ⁴		25	75		25	50		25	50		25	50	ps
$V_{PP}(\text{AC})$	Minimum Input Swing ⁸	250			250			250			250			mV
V_{CMR}	Common Mode Range ⁹	$V_{CC} - 1.6$		$V_{CC} - 0.4$	$V_{CC} - 1.6$		$V_{CC} - 0.4$	$V_{CC} - 1.6$		$V_{CC} - 0.4$	$V_{CC} - 1.6$		$V_{CC} - 0.4$	V
t_r / t_f	Rise/Fall Time	250		650	275		600	275		600	275		600	ps

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
3. Enable is defined as the propagation delay from the 50% point of a negative transition on \bar{EN} to the 50% point of a positive transition on Q (or a negative transition on \bar{Q}). Disable is defined as the propagation delay from the 50% point of a positive transition on \bar{EN} to the 50% point of a negative transition on Q (or a positive transition on \bar{Q}).
4. The within-device skew is defined as the worst-case difference between any two similar delay paths within a single device.
5. The setup time is the minimum time that \bar{EN} must be asserted prior to the next transition of IN/ \bar{IN} to prevent an output response greater than $\pm 75mV$ to that IN/ \bar{IN} transition (see Figure 1).
6. The hold time is the minimum time that \bar{EN} must remain asserted after a negative going IN or a positive going \bar{IN} to prevent an output response greater than $\pm 75mV$ to that IN/ \bar{IN} transition (see Figure 2).
7. The release time is the minimum time that \bar{EN} must be de-asserted prior to the next IN/ \bar{IN} transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
8. $V_{PP}(\text{min})$ is defined as the minimum peak-to-peak input differential voltage which will cause no increase in the propagation delay. The $V_{PP}(\text{min})$ is AC limited for the E111, because differential input as low as 50 mV will still produce full ECL levels at the output.
9. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to $V_{PP}(\text{min})$.

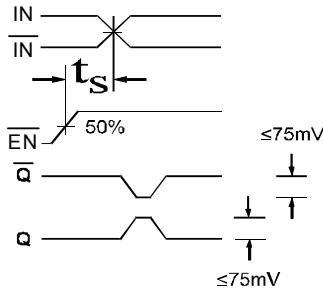


Figure 1. Setup Time

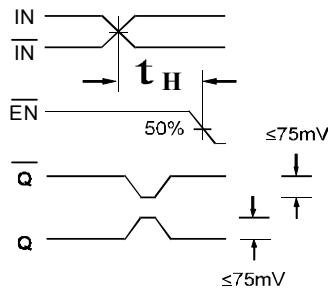


Figure 2. Hold Time

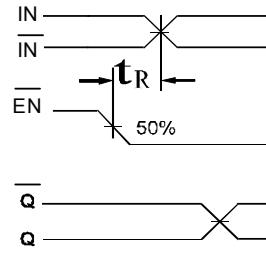
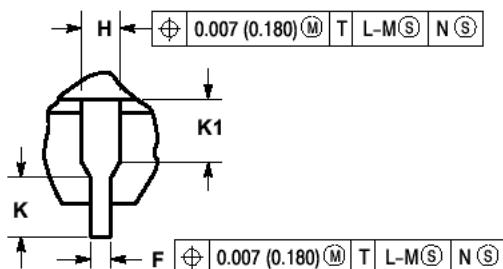
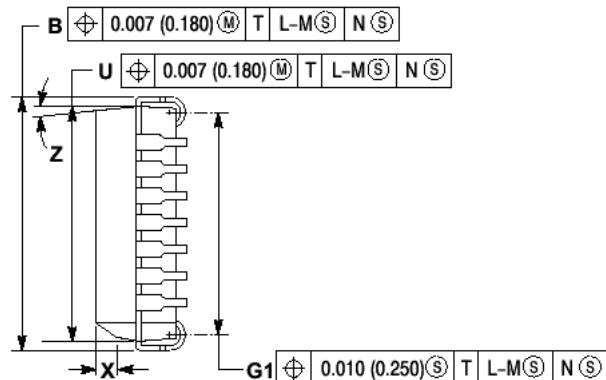
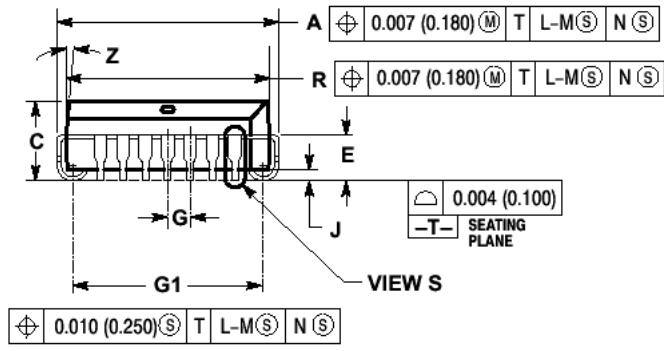
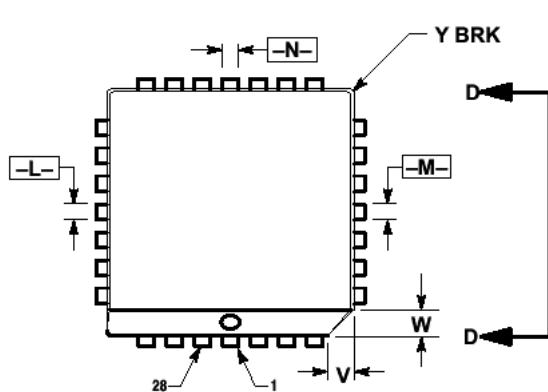


Figure 3. Release Time

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**PACKAGE DIAGRAM
PLCC 28**



VIEW D-D

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51		0.020	
K	0.64		0.025	
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
T		0.50		0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02		0.040	

NOTES:

1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010mm (0.250in.) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012mm (0.300in.). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025mm (0.635in.).

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