EB51F3C50N-20.480M

ECLIPTEK® CORPORATION

DRC CONFLICT FREE

ITEM DESCRIPTION

Temperature Compensated Quartz Crystal Clock Oscillators TCXO HCMOS/TTL (CMOS) 5.0Vdc 14-Pin DIP Metal Thru-Hole 20.480MHz ±5.0ppm Maximum -20°C to +70°C

ELECTRICAL SPECIFICATIONS

Nominal Frequency	20.480MHz
Frequency Stability	±5.0ppm Maximum (Inclusive of Operating Temperature Range)
Frequency Stability vs. Input Voltage	±0.3ppm Maximum (±5%)
Frequency Stability vs. Load	±0.2ppm Maximum (±2pF)
Aging at 25°C	±1ppm/Year Maximum
Operating Temperature Range	-20°C to +70°C
Supply Voltage	5.0Vdc ±5%
Input Current	30mA Maximum
Output Voltage Logic High (Voh)	2.4Vdc Minimum w/TTL Load, Vdd-0.5Vdc Minimum w/HCMOS Load
Output Voltage Logic Low (Vol)	0.4Vdc Maximum w/TTL Load, 0.5Vdc Maximum w/HCMOS Load
Rise/Fall Time	10nSec Maximum (Measured at 0.4Vdc to 2.4Vdc w/TTL Load, 20% to 80% of waveform w/HCMOS Load)
Duty Cycle	50 ±10(%) (Measured at 1.4Vdc w/TTL Load, at 50% of waveform w/HCMOS Load)
Load Drive Capability	10TTL Load or 15pF HCMOS Load Maximum
Output Logic Type	CMOS
Control Voltage	None (No Connect on Pin 1)
Internal Trim	±3ppm Minimum (Top of Can)
Modulation Bandwidth	10kHz Minimum (Measured at -3dB with a Control Voltage of 2.5Vdc)
Input Impedance	10kOhms Typical
Phase Noise	-70dBc at 10Hz Offset, -100dBc at 100Hz Offset, -130dBc at 1kHz Offset, -140dBc at 10kHz Offset, -145dBc at 100kHz Offset
Storage Temperature Range	-40°C to +85°C

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

Fine Leak Test	MIL-STD-883, Method 1014 Condition A (Internal Crystal Only)
Gross Leak Test	MIL-STD-883, Method 1014 Condition C (Internal Crystal Only)
Lead Integrity	MIL-STD-883, Method 2004
Mechanical Shock	MIL-STD-202, Method 213 Condition C
Resistance to Soldering Heat	MIL-STD-202, Method 210
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010
Vibration	MIL-STD-883, Method 2007 Condition A

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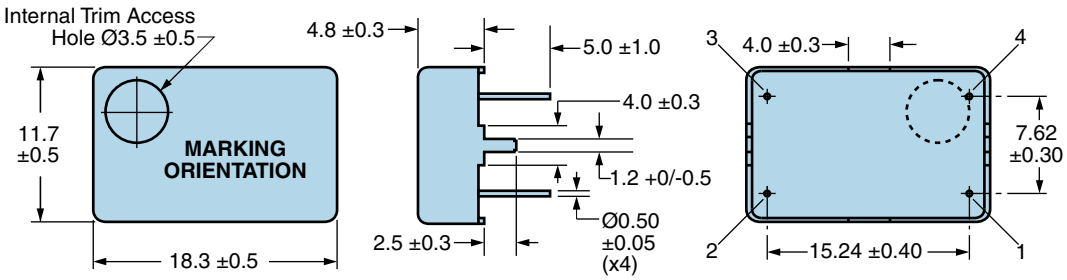
MECHANICAL DIMENSIONS (all dimensions in millimeters)



PIN	CONNECTION
1	No Connect
2	Case Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	**ECLIPTEK**
2	**20.480M**
3	**XXYZZ** *XX=Ecliptek Manufacturing Code* *Y=Last Digit of the Year* *ZZ=Week of the Year*

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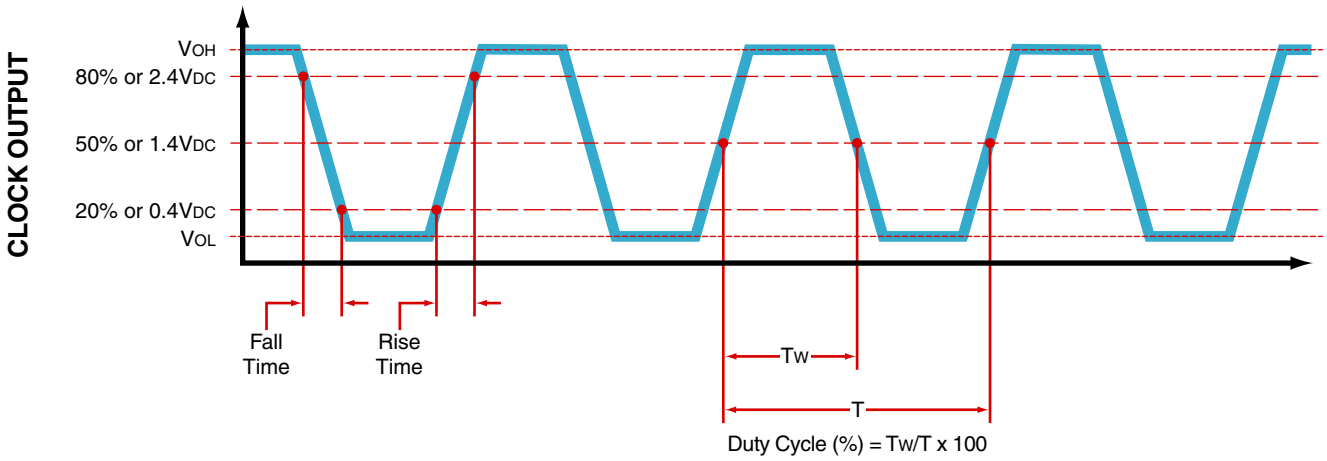
OUTPUT WAVEFORM



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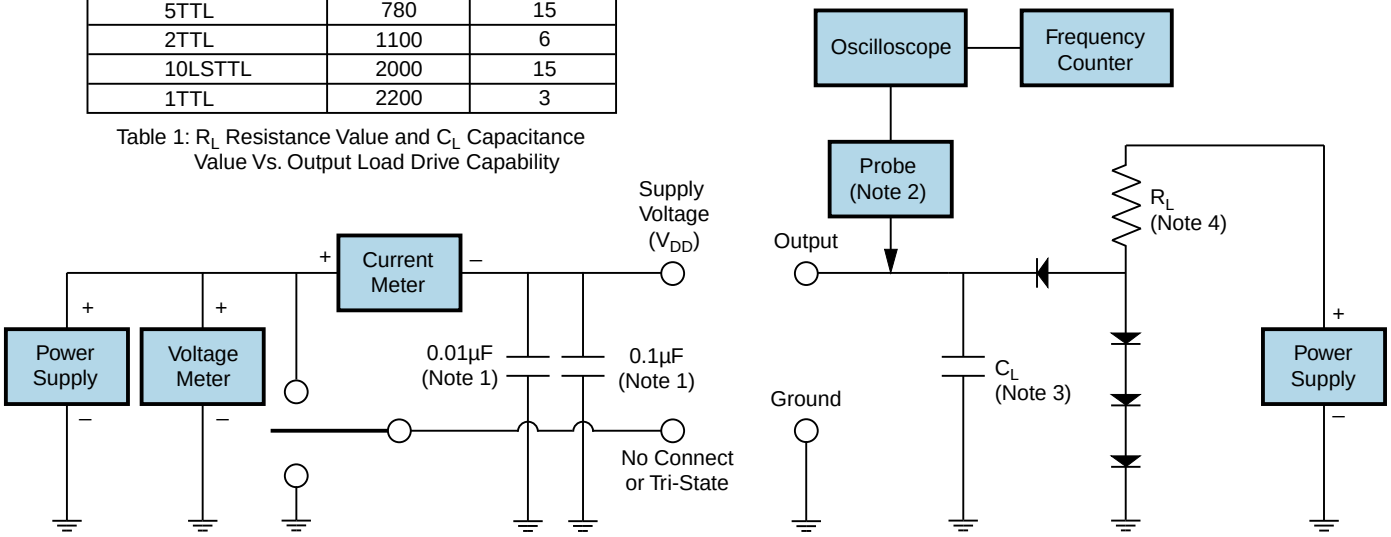
Test Circuit for TTL Output

Output Load Drive Capability	R_L Value (Ohms)	C_L Value (pF)
10TTL	390	15
5TTL	780	15
2TTL	1100	6
10LSTTL	2000	15
1TTL	2200	3

Table 1: R_L Resistance Value and C_L Capacitance Value Vs. Output Load Drive Capability



Note 1: An external 0.1µF low frequency tantalum bypass capacitor in parallel with a 0.01µF high frequency ceramic bypass capacitor close to the package ground and V_{DD} pin is required.
Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.
Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.
Note 4: Resistance value R_L is shown in Table 1. See applicable specification sheet for 'Load Drive Capability'.
Note 5: All diodes are MMBD7000, MMBD914, or equivalent.

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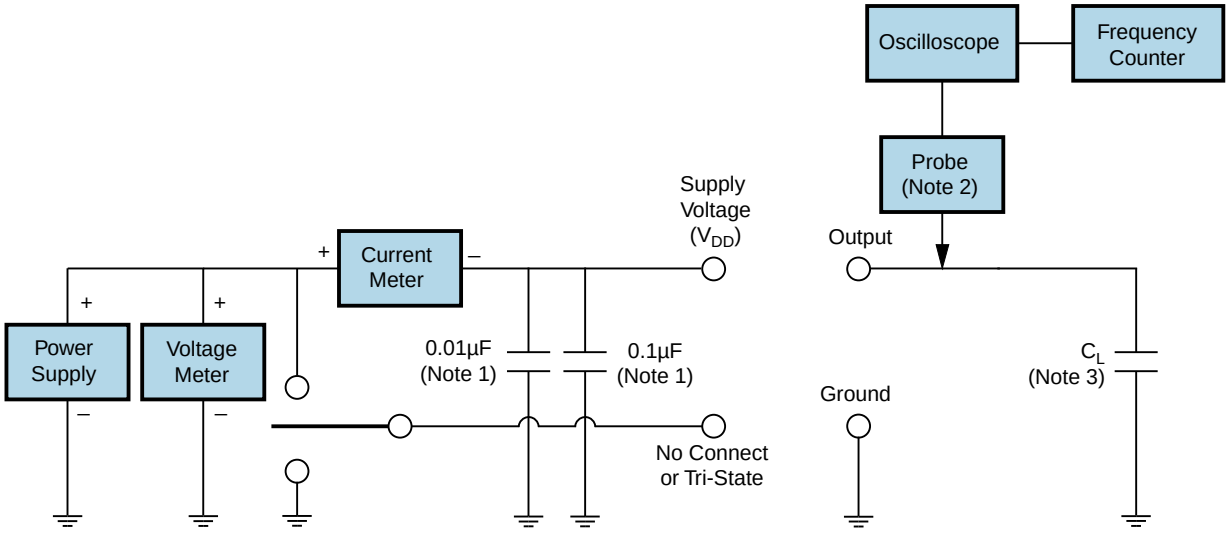
Test Circuit for CMOS Output



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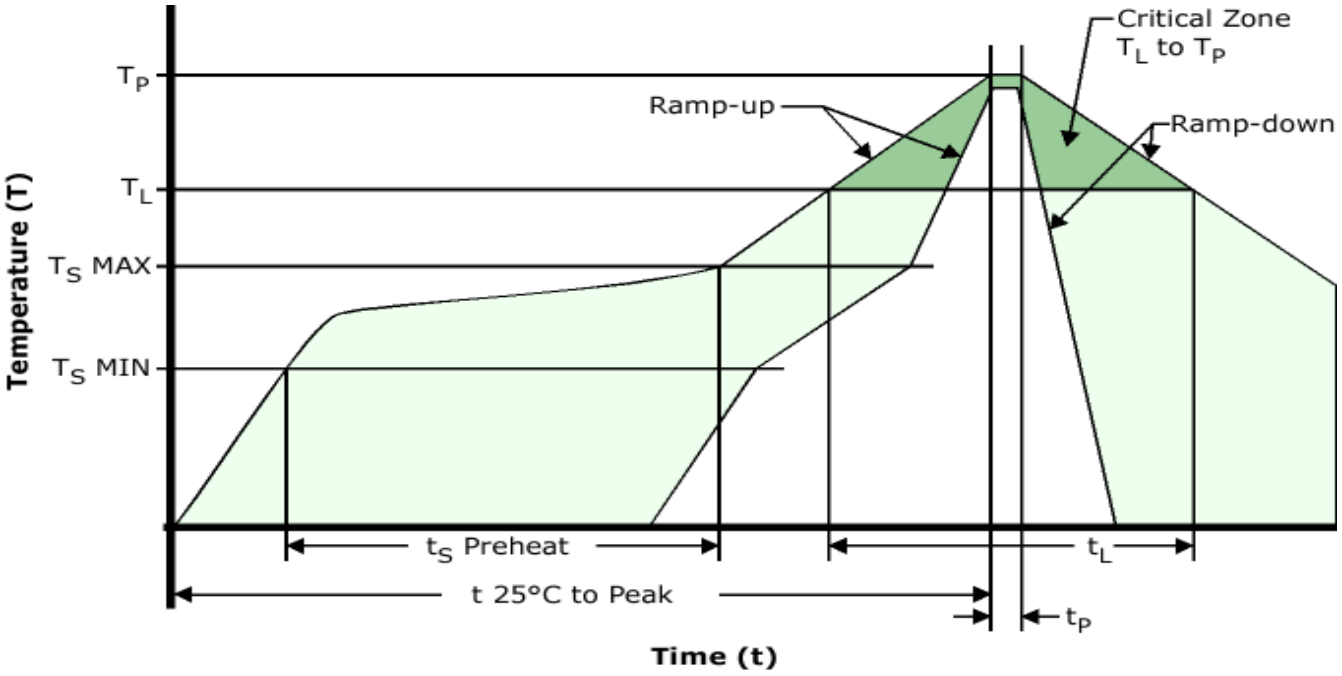
Recommended Solder Reflow Methods



Low Temperature Solder Bath (Wave Solder)

T_S MAX to T_L (Ramp-up Rate)	5°C/Second Maximum
Preheat	
- Temperature Minimum (T_S MIN)	N/A
- Temperature Typical (T_S TYP)	150°C
- Temperature Maximum (T_S MAX)	N/A
- Time (t_S MIN)	30 - 60 Seconds
Ramp-up Rate (T_L to T_P)	5°C/Second Maximum
Time Maintained Above:	
- Temperature (T_L)	150°C
- Time (t_L)	200 Seconds Maximum
Peak Temperature (T_P)	245°C Maximum
Target Peak Temperature (T_P Target)	245°C Maximum 1 Time / 235°C Maximum 2 Times
Time within 5°C of actual peak (t_p)	5 Seconds Maximum 1 Time / 15 Seconds Maximum 2 Times
Ramp-down Rate	5°C/Second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1

Low Temperature Manual Soldering

185°C Maximum for 10 Seconds Maximum, 2 times Maximum. (Temperatures listed are applied to device leads only.)

High Temperature Manual Soldering

260°C Maximum for 5 Seconds Maximum, 2 times Maximum. (Temperatures listed are applied to device leads only.)

Low Temperature Solder Bath (Wave Solder) Note 1

Device is non-hermetic; Post reflow aqueous wash is not recommended

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Low Temperature Solder Bath (Wave Solder) Note 2

Temperatures shown are applied to back of PCB board and device leads only.

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