Low-Voltage Dual SPST Analog Switch

DESCRIPTION

The DG9432, DG9433, DG9434 is a dual single-pole/single-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed (t_{ON}: 25 ns, t_{OFF}: 20 ns), the DG9432, DG9433, DG9434 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG9432, DG9433, DG9434 is built on Vishay Siliconix's low voltage BCD-15 process. An epitaxial layer prevents latchup. Break-before-make is guaranteed for DG9432, DG9433, DG9434.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FEATURES

- Wide operation voltage (+ 2.7 V to + 12 V)
- Low charge injection - Q_{INJ}: 1 pC
- Low power consumption
- TTL/CMOS logic compatible over the full operating voltage range
- Available in MSOP-8 and SOT23-8
- **Compliant to RoHS Directive 2002/95/EC**

Pb-free
RoHS COMPLIANT

BENEFITS

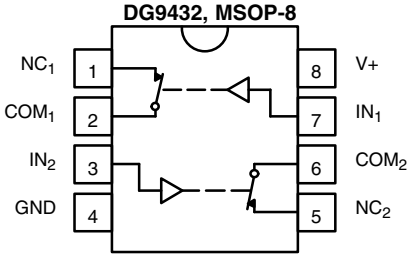
- Reduced power consumption
- Simple logic interface
- High accuracy
- Reduce board space

APPLICATIONS

- Battery operated systems
- Portable test equipment
- Sample and hold circuits
- Cellular phones
- Communication systems
- Military radio
- PBX, PABX guidance and control systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION - DG9432

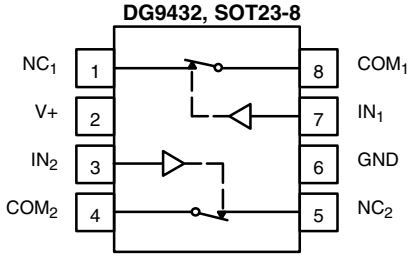
DG9432, MSOP-8



Top View

Device Marking: 9432

DG9432, SOT23-8



Top View

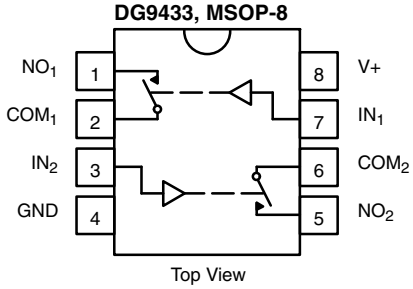
Device Marking: 4G

TRUTH TABLE DG9432

Logic	Switch
0	On
1	Off

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION - DG9433/DG9434

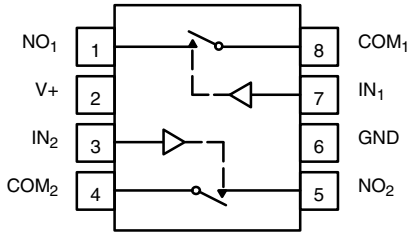
DG9433, MSOP-8



Top View

Device Marking: 9433

DG9433. SOT23-8

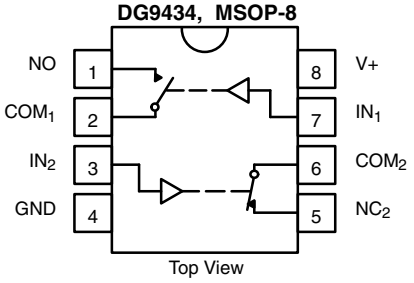


Top View

Device Marking: 4H

TRUTH TABLE DG9433	
Logic	**Switch**
0	Off
1	On

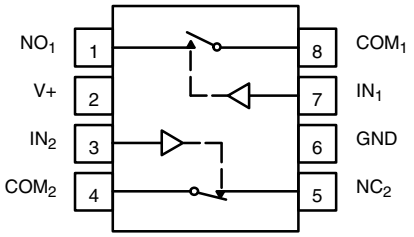
DG9434, MSOP-8



Top View

Device Marking: 9434

DG9434. SOT23-8



Top View

Device Marking: 4I

TRUTH TABLE DG9434		
Logic	**Switch-1**	**Switch-2**
0	Off	On
1	On	Off

ORDERING INFORMATION		
Temp. Range	**Package**	**Part Number**
- 40 °C to 85 °C	MSOP-8	DG9432DQ-T1-E3
		DG9433DQ-T1-E3
		DG9434DQ-T1-E3
	SOT23-8	DG9432DS-T1-E3
		DG9433DS-T1-E3
		DG9433DS-T1-E3

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 13.5	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3)	
Continuous Current (Any terminal)		± 10	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 20	
Storage Temperature (D suffix)		- 65 to 150	°C
Power Dissipation (Packages)[b]	MSOP-8[c]	320	mW
	SOT23-8[c]	515	

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6.5 mW/°C above 75 °C.

SPECIFICATIONS V+ = 3 V

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3.3 V, ± 10 %, V_{IN} = 0.4 V or 1.8 V[e]	Temp.[a]	Limits - 40 °C °C to 85 °C Min.[c]	Typ.[b]	Max.[c]	Unit
Switch On Resistance							
Analog Signal Range[e]	V_{ANALOG}		Full	V-		V+	V
Drain-Source On- Resistance	$R_{(on)}$	V+ = 2.7 V, I_{COM} = 1 mA, V_{COM} = 1.5 V	Room Full		81	100 120	Ω
R_{ON} Match[d]	ΔR_{on}		Room		0.4	3.0	
Digital Control							
Input, High Voltage	V_{INH}	V+ Ranges 2.7 to 5 V	Full	1.8			V
Input, Low Voltage	V_{INL}		Full			0.4	
Input Current	I_{INH}			- 1		1	µA
Dynamic Characteristics							
Break-Before-Make[d,g]	t_{OPEN}	V+ = 3 V, R_L = 300 Ω V_{NO} = V_{NC} = 1.5 V C_L = 35 pF, V_{IN} = 0 V, 3 V	Room Full	1			ns
Turn-On Time[d]	t_{ON}		Room Full		60	80 100	
Turn-Off Time[d]	t_{OFF}		Room Full		14	25 35	
Charge Injection[d]	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_g = 0 V	Room		0.16		pC
Off-Isolation[d]	OIRR	C_L = 5 pF, R_L = 50 Ω, f = 1 MHz	Room		77		dB
		C_L = 5 pF, R_L = 50 Ω, f = 10 MHz	Room		55		
Crosstalk[d]	X_{TALK}	R_L = 50 Ω, f = 1 MHz, V+ = 2.5 V	Room		98		
Source Off Capacitance[d]	$C_{NO/NC(off)}$	f = 1 MHz, $V_{NC/NO}$ = 0 V	Room		7.5		pF
Drain Off Capacitance[d]	$C_{COM(off)}$	f = 1 MHz V_{COM} = 0 V	Room		7.8		
Drain On Capacitance[d]	$C_{COM(on)}$		Room		22		
Supply Current	I+	V+ = 3.3 V, V_{IN} = 0 or V+	Room	- 1		- 1	µA

Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, not subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 12 V leakage testing, not production tested.
g. Applies for DG9434 only.

SPECIFICATIONS V+ = 5 V							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 5 V, ± 10 %, V_{IN} = 0.4 V or 1.8 V[e]	**Temp.[a]**	**Limits** - 40 °C °C to 85 °C **Min.[c]**	**Typ.[b]**	**Max.[c]**	**Unit**
Switch On Resistance							
Analog Signal Range[e]	V_{ANALOG}		Full	V-		V+	V
Drain-Source On-Resistance	$R_{(on)}$	V+ = 4.5 V, I_{COM} = 1 mA V_{COM} = 2.5 V or 3.5 V	Room Full		39	60 70	Ω
$R_{DS(on)}$ Match	$\Delta R_{(on)}$	V+ = 4.5 V, I_{COM} = 1 mA, V_{COM} = 3.5 V	Room		0.3	3.0	
Switch Off Leakage Current[f]	$I_{NC/NO(off)}$	V+ = 5 V, V_{COM} = 0.5 V, 4.5 V $V_{NC/NO}$ = 4.5 V, 0.5 V	Room Full	- 1 - 10	0.3	1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10	0.3	1 10	
Channel On Leakage Current[f]	$I_{COM(on)}$		Room Full	- 1 - 10	0.3	1 10	
Digital Control							
Input, High Voltage	V_{INH}	V+ Ranges 2.7 to 5 V	Full	1.8			V
Input, Low Voltage	V_{INL}		Full			0.4	
Input Current	I_{INH}			- 1		1	µA
Dynamic Characteristics							
Break-Before-Make[d,g]	t_{OPEN}	V+ = 5 V, R_L = 300 Ω V_{NO} = V_{NC} = 3 V C_L = 35 pF, V_{IN} = 0 V, 5 V	Room Full	1			ns
Turn-On Time	t_{ON}		Room Full		33	60 70	
Turn-Off Time	t_{OFF}		Room Full		10	20 30	
Charge Injection[d]	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_g = 0 V	Room		0.56		pC
Off-Isolation[d]	OIRR	C_L = 5 pF, R_L = 50 Ω, f = 1 MHz	Room		76		dB
		C_L = 5 pF, R_L = 50 Ω, f = 10 MHz, V+ = 5 V	Room		54		
Crosstalk[d]	X_{TALK}	R_L = 50 Ω, f = 1 MHz, V+ = 5 V	Room		96		
Source Off Capacitance[d]	$C_{NC/NO(off)}$	f = 1 MHz, $V_{NC/NO}$ = 0 V	Room		7.5		pF
Drain Off Capacitance[d]	$C_{COM(off)}$	f = 1 MHz, V_{COM} = 0 V	Room		7.8		
Drain On Capacitance[d]	$C_{COM(on)}$		Room		22		
Supply Current	I+	V+ = 5.5 V, V_{IN} = 0 or V+	Room	- 1		- 1	µA

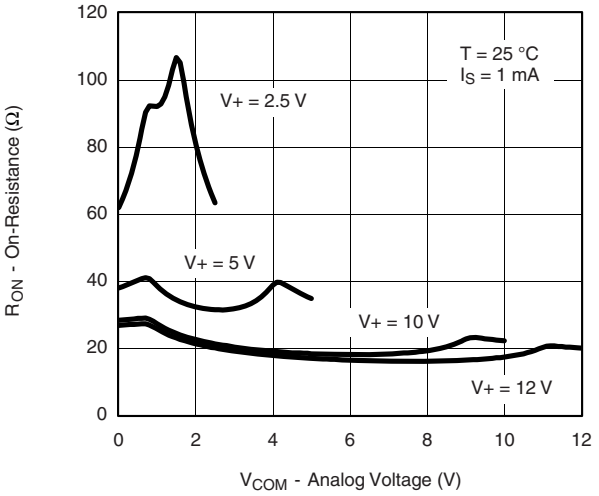
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, not subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 12 V leakage testing, not production tested.
g. Applies for DG9434 only.

SPECIFICATIONS V+ = 12 V							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 12 V, ± 10 %, V_{IN} = 0.8 V or 2.4 V[e]	**Temp.[a]**	**Limits** - 40 °C °C to 85 °C **Min.[c]**	**Typ.[b]**	**Max.[c]**	**Unit**
Switch On Resistance							
Analog Signal Range[e]	V_{ANALOG}		Full	V-		V+	V
Drain-Source On-Resistance	$R_{(on)}$	V+ = 10.8 V, I_{COM} = 1 mA, V_{COM} = 9 V	Room Full		19	30 40	Ω
$R_{DS(on)}$ Match	$\Delta R_{(on)}$		Room		0.3	3.0	
Switch Off Leakage Current[a]	$I_{NC/NO(off)}$	V+ = 12 V, V_S = 1/11 V, V_{COM} = 11/1 V	Room Full	- 1 - 10	0.3	1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10	0.3	1 10	
Channel On Leakage Current[a]	$I_{COM(on)}$		Room Full	- 1 - 10	0.3	1 10	
Digital Control							
Input, High Voltage	V_{INH}	V+ = 12 V	Full			2.4	V
Input, Low Voltage	V_{INL}		Full	0.8			
Input Current	I_{INH}			- 1		1	µA
Dynamic Characteristics							
Break-Before-Make[d,g]	t_{OPEN}	V+ = 12 V, R_L = 300 Ω V_{NO} = V_{NC} = 8 V C_L = 35 pF, V_{IN} = 0 V, 12 V	Room Full	1			ns
Turn-On Time	t_{ON}		Room Full		21	35 40	
Turn-Off Time	t_{OFF}		Room Full		6	18 25	
Charge Injection[d]	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_g = 0 V, V+ = 5 V	Room		0.36		pC
Off-Isolation[d]	OIRR	C_L = 5 pF, R_L = 50 Ω, f = 1 MHz	Room		75		dB
		C_L = 5 pF, R_L = 50 Ω, f = 10 MHz	Room		53		
Crosstalk[d]	X_{TALK}	R_L = 50 Ω, f = 1 MHz, V+ = 5 V	Room		96		
Source Off Capacitance[d]	$C_{NO/NC(off)}$	f = 1 MHz, $V_{NC/NO}$ = 0 V	Room		7.5		pF
Drain Off Capacitance[d]	$C_{COM(off)}$	f = 1 MHz, V_{COM} = 0 V	Room		7.8		
Drain On Capacitance[d]	$C_{COM(on)}$		Room		22		
Supply Current	I+	V+ = 12 V, V_{IN} = 0 or V+	Room	- 1		- 1	µA

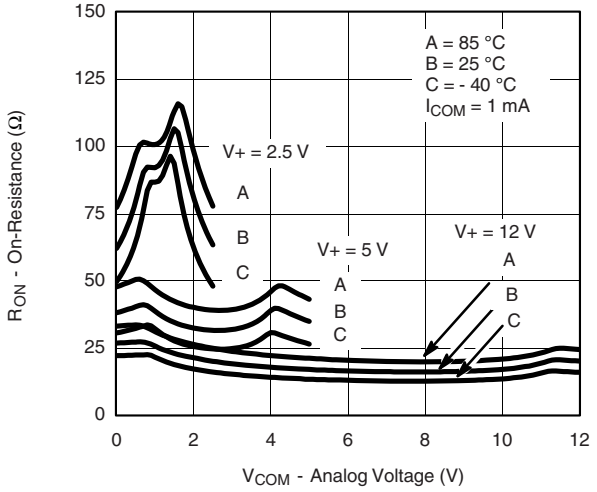
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, not subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 12 V leakage testing, not production tested.
g. Applies for DG9434 only.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

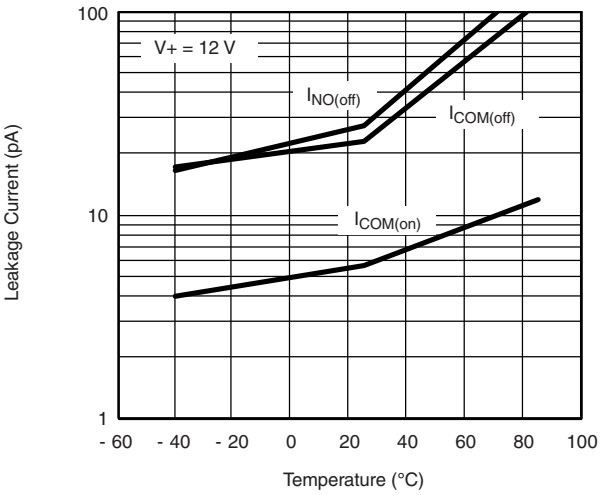
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



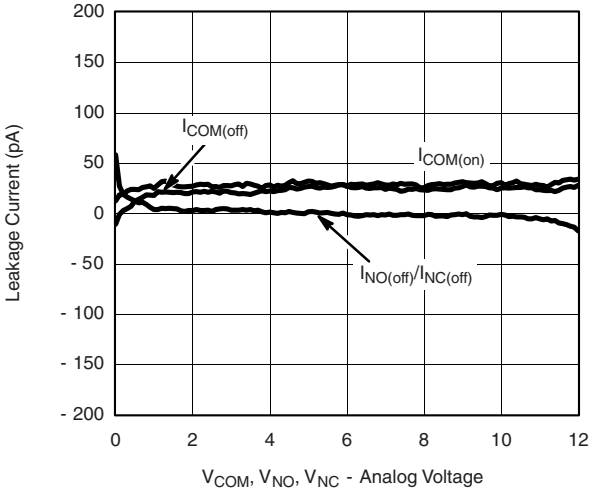
R_{ON} vs. V_{COM} and Single Supply Voltage



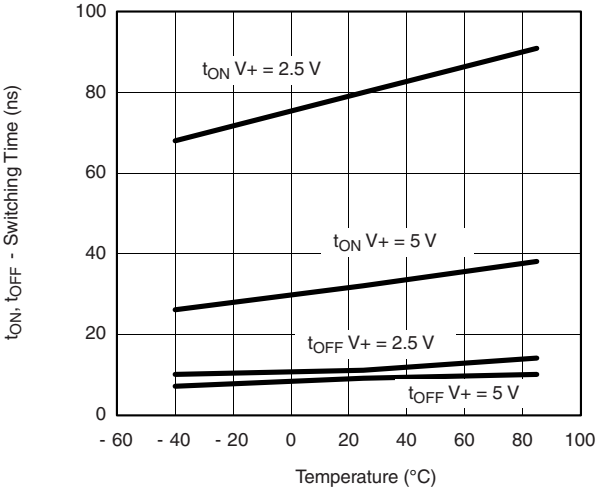
R_{ON} vs. Analog Voltage and Temperature



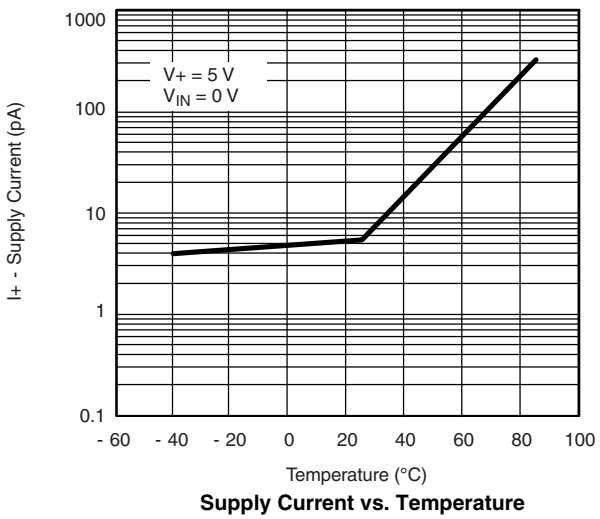
Leakage Current vs. Temperature



Leakage Current vs. Analog Voltage

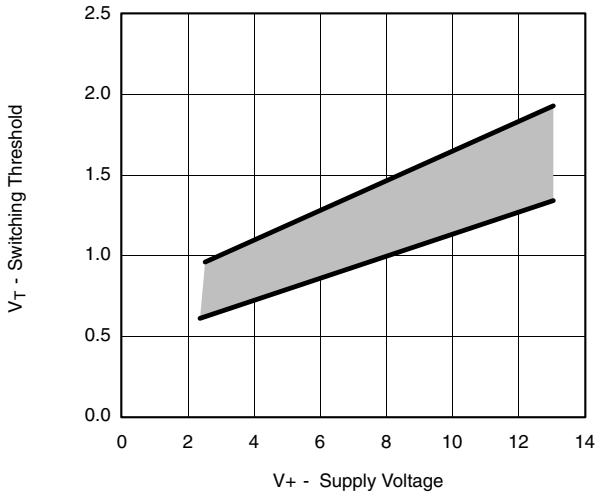


Switching Time vs. Temperature

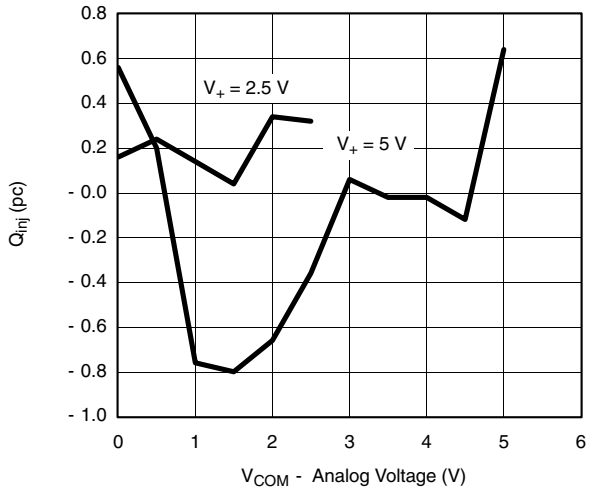


Supply Current vs. Temperature

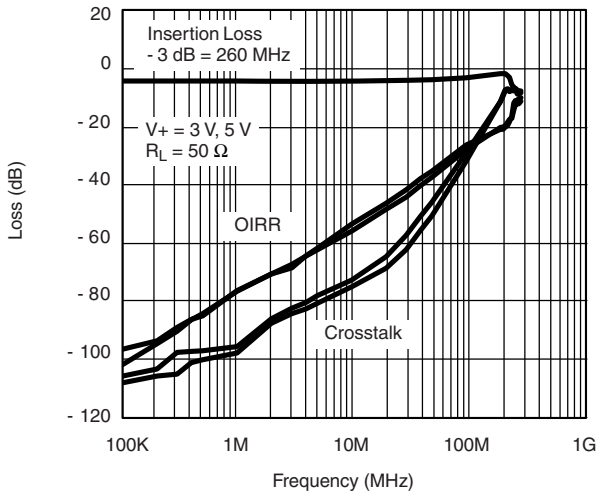
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



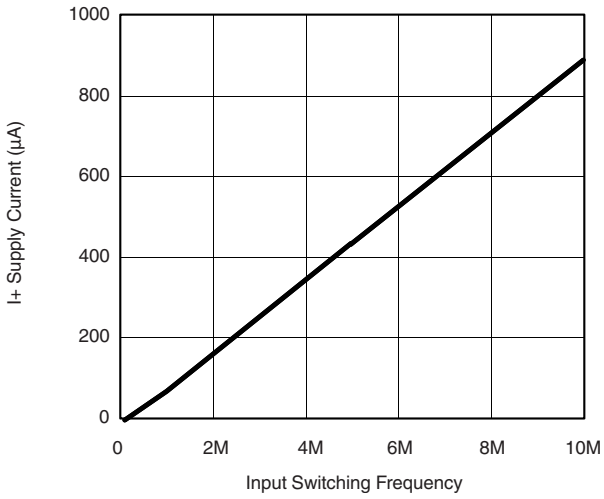
Switching Threshold vs. Supply Voltage



Charge Injection at Source

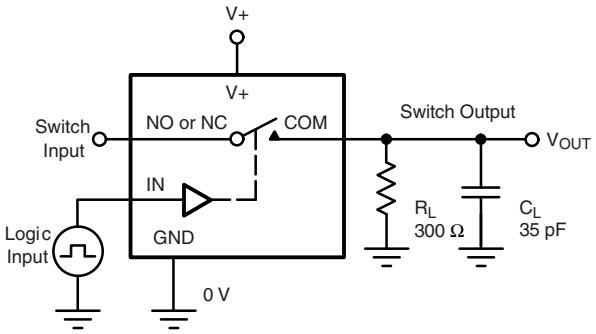


Insertion Loss, Off Isolation and Crosstalk vs. Frequency



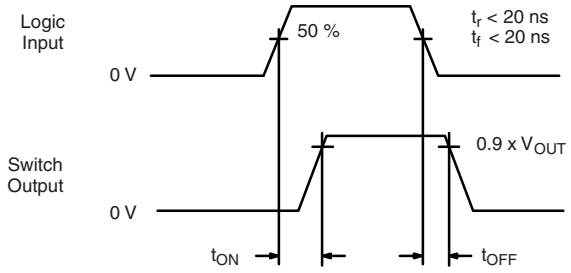
Supply Current vs. Input Switching Frequency

TEST CIRCUITS



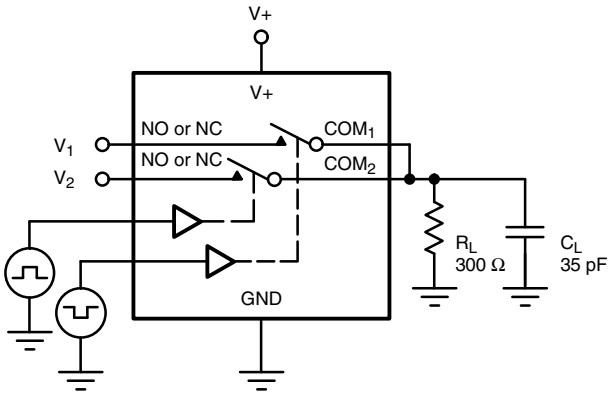
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

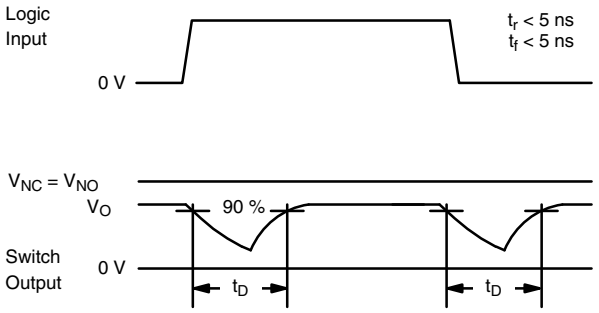
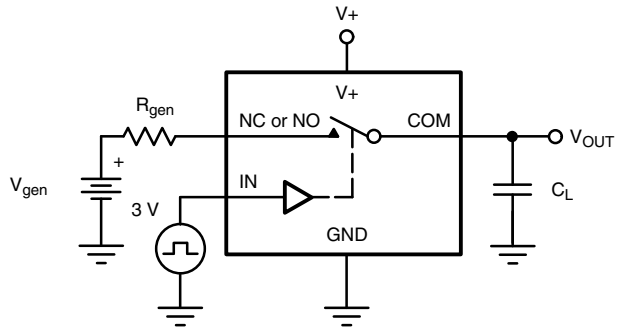
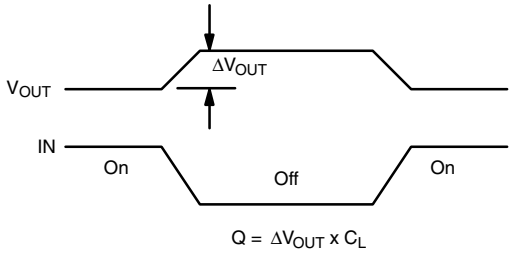


Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

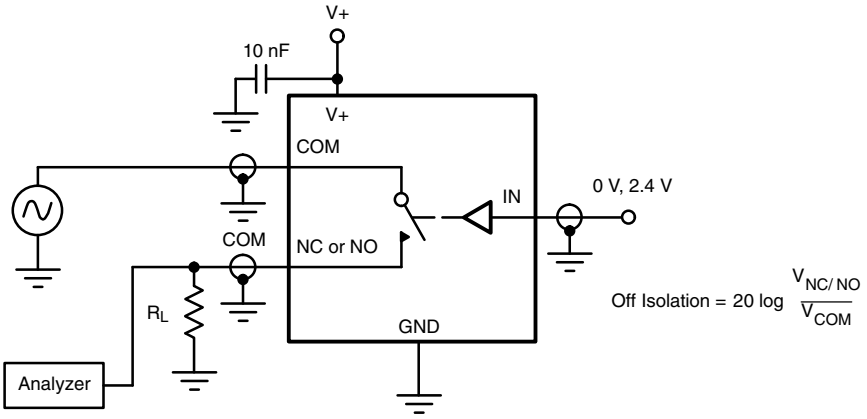


Figure 4. Off-Isolation

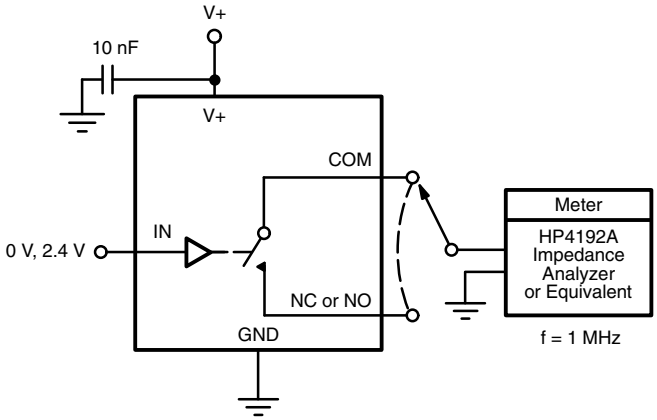
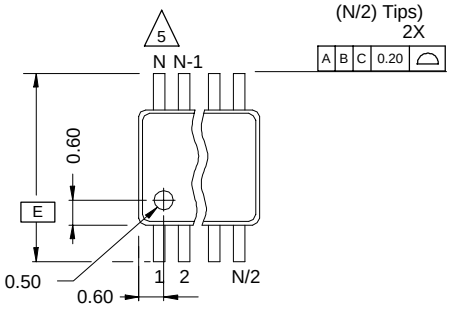


Figure 5. Channel Off/On Capacitance

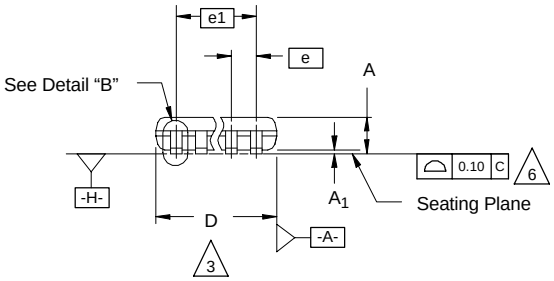
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72311.

MSOP: 8-LEADS

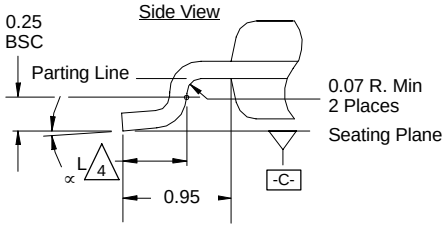
JEDEC Part Number: MO-187, (Variation AA and BA)



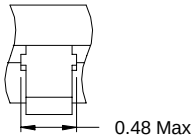
Top View



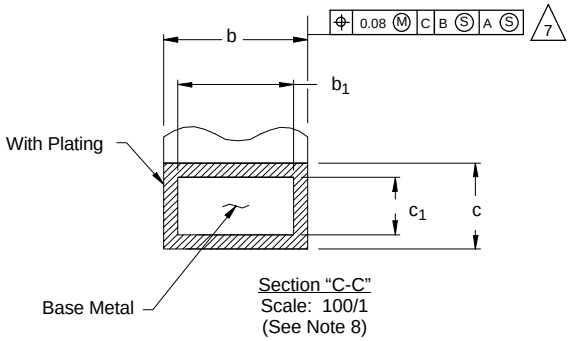
Side View



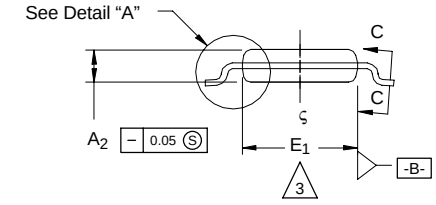
Detail "A"
(Scale: 30/1)



Detail "B"
(Scale: 30/1)
Dambar Protrusion



Section "C-C"
Scale: 100/1
(See Note 8)



End View

NOTES:

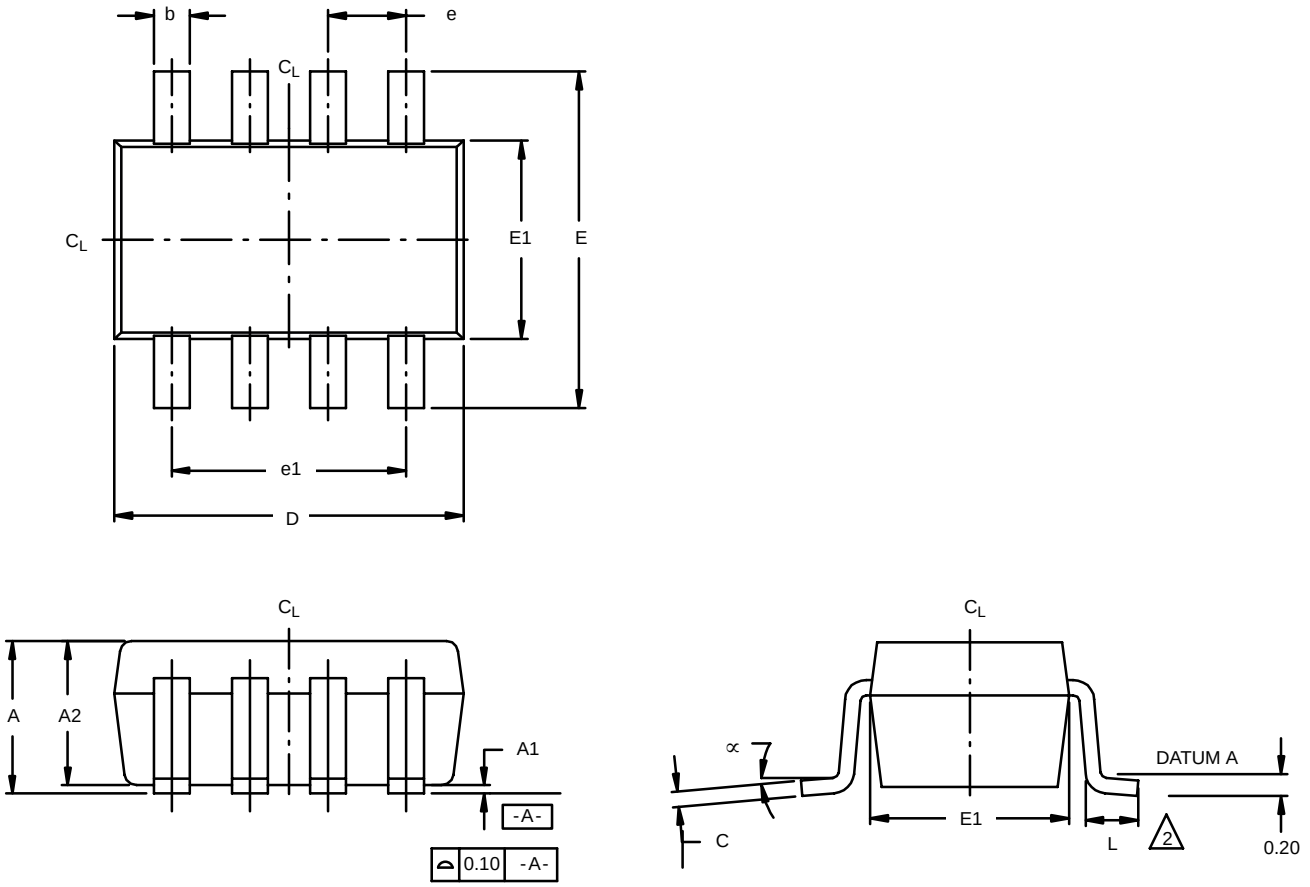
1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "E_1" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 8L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	-	-	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.25	-	0.38	8
b_1	0.25	0.30	0.33	8
c	0.13	-	0.23	
c_1	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E_1	2.90	3.00	3.10	3
e	0.65 BSC			
e_1	1.95 BSC			
L	0.40	0.55	0.70	4
N	8			5
∝	0°	4°	6°	

ECN: T-02080—Rev. C, 15-Jul-02
DWG: 5867

SOT-23 : 8-LEAD



NOTES:

1. All dimensions are in millimeters.
2. Foot length measured at intercept point between Datum A and lead surface.
3. Package outline exclusive of mold flash and metal burr.
4. Package outline inclusive of solder plating.
5. No molding flash allowed on the top and bottom lead surface.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	1.27	1.45	0.035	0.05	0.057
A1	0.00	0.0762	0.15	0.000	0.003	0.006
A2	0.90	1.20	1.30	0.035	0.047	0.051
b	0.22	0.30	0.38	0.009	0.012	0.015
C	0.09	0.152	0.20	0.004	0.006	0.008
D	2.80	2.9	3.00	0.11	0.114	0.118
E	2.60	2.8	23.00	0.102	0.11	0.118
E1	1.50	1.65	1.75	0.059	0.065	0.069
e	0.65 REF			0.026 REF		
e1	1.95 REF			0.077 REF		
L	0.35	0.45	0.55	0.014	0.018	0.022
∝	0°	4°	8°	0°	4°	8°

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DWG: 5895

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