

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC7W00F, TC7W00FU, TC7W00FK

## DUAL 2-INPUT NAND GATE

The TC7W00 is a high speed C<sup>2</sup>MOS 2-INPUT NAND GATE fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the C<sup>2</sup>MOS low power dissipation.

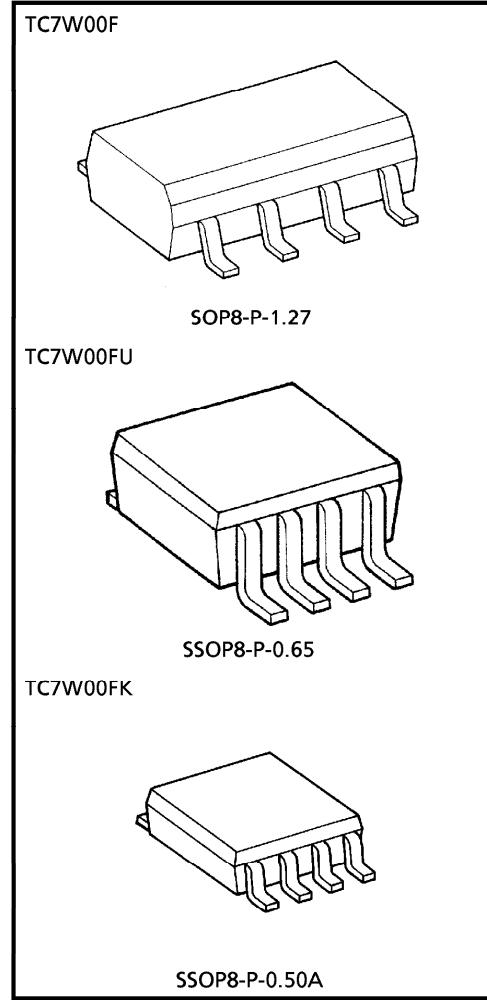
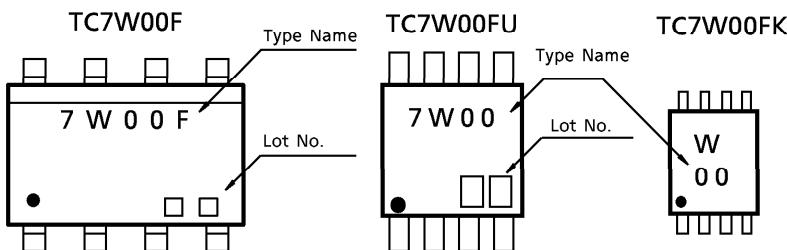
The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### FEATURES

- High Speed .....  $t_{pd} = 6\text{ns}$  (Typ.) at  $V_{CC} = 5\text{V}$
- Low Power Dissipation .....  $I_{CC} = 1\mu\text{A}$  (Max.) at  $T_a = 25^\circ\text{C}$
- High Noise Immunity .....  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ...  $|I_{OH}| = |I_{OL}| = 4\text{mA}$  (Min.)
- Balanced Propagation Delays .....  $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range ...  $V_{CC}(\text{opr}) = 2\text{~}6\text{V}$

### MARKING

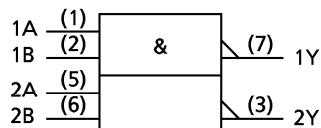


Weight  
 SOP8-P-1.27 : 0.05g (Typ.)  
 SSOP8-P-0.65 : 0.02g (Typ.)  
 SSOP8-P-0.50A : 0.01g (Typ.)

MAXIMUM RATINGS ( $T_a = 25^\circ\text{C}$ )

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	$V_{CC}$	$-0.5 \sim 7$	V
DC Input Voltage	$V_{IN}$	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ / Ground Current	$I_{CC}$	$\pm 25$	mA
Power Dissipation	$P_D$	300 (FM8, SM8) 200 (US8)	mW
Storage Temperature	$T_{stg}$	$-65 \sim 150$	$^\circ\text{C}$
Lead Temperature (10s)	$T_L$	260	$^\circ\text{C}$

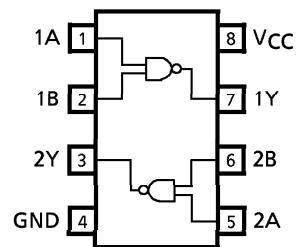
## LOGIC DIAGRAM



## TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

## PIN ASSIGNMENT (TOP VIEW)



## RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}$	2~6	V
Input Voltage	$V_{IN}$	$0 \sim V_{CC}$	V
Output Voltage	$V_{OUT}$	$0 \sim V_{CC}$	V
Operating Temperature	$T_{opr}$	$-40 \sim 85$	$^\circ\text{C}$
Input Rise and Fall Time	$t_r, t_f$	0~1000 ( $V_{CC} = 2.0\text{V}$ ) 0~ 500 ( $V_{CC} = 4.5\text{V}$ ) 0~ 400 ( $V_{CC} = 6.0\text{V}$ )	ns

## DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITION	V <sub>CC</sub>	Ta = 25°C			Ta = - 40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V <sub>IH</sub>	—	2.0 4.5 6.0	1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	V	
Low-Level Input Voltage	V <sub>IL</sub>	—	2.0 4.5 6.0	— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = - 20 $\mu$ A	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	
			I <sub>OH</sub> = - 4mA I <sub>OH</sub> = - 5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	V
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub>	I <sub>OL</sub> = 20 $\mu$ A	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	
			I <sub>OL</sub> = 4mA I <sub>OL</sub> = 5.2mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	V
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	—	—	± 0.1	—	± 1.0	—	$\mu$ A
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	—	—	1.0	—	10.0		

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 15pF, V<sub>CC</sub> = 5V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			MIN.	TYP.	MAX.	
Output Transition Time	t <sub>TLH</sub> t <sub>THL</sub>	—	—	4	8	ns
Propagation Delay Time	t <sub>pLH</sub> t <sub>pHL</sub>	—	—	6	12	ns

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$ )

CHARACTERISTIC	SYMBOL	TEST CONDITION	$V_{CC}$	Ta = 25°C			Ta = - 40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	$t_{TLH}$ $t_{THL}$	—	2.0	—	25	75	—	95	ns
			4.5	—	7	15	—	19	
			6.0	—	6	13	—	16	
Propagation Delay Time	$t_{PLH}$ $t_{PHL}$	—	2.0	—	27	75	—	95	ns
			4.5	—	9	15	—	19	
			6.0	—	8	13	—	16	
Input Capacitance	$C_{IN}$	—	—	—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{PD}$	(Note 1)	—	—	20	—	—	—	

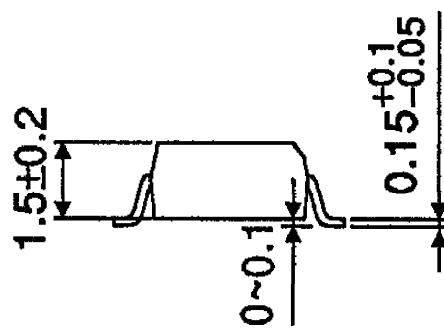
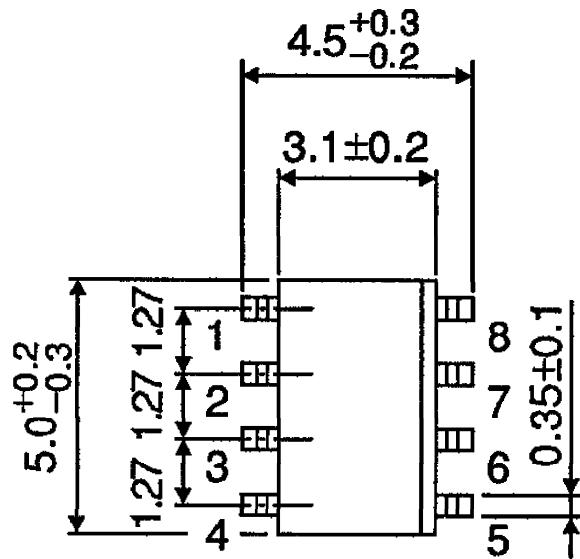
(Note 1)  $C_{PD}$  is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder.

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per gate)}$$

**PACKAGE DIMENSIONS**  
SOP8-P-1.27

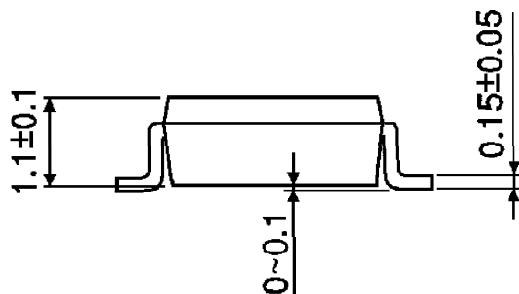
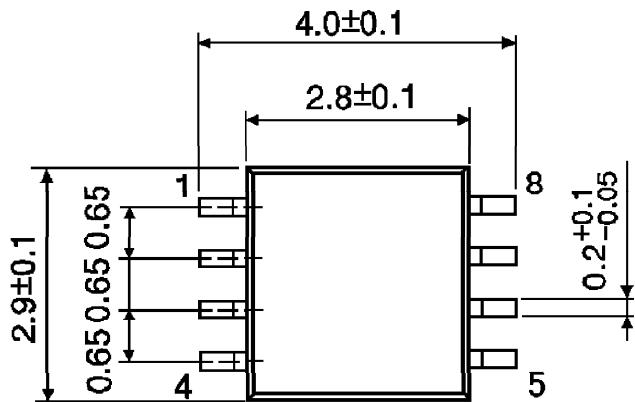
Unit : mm



Weight : 0.05g (Typ.)

**PACKAGE DIMENSIONS**  
SSOP8-P-0.65

Unit : mm

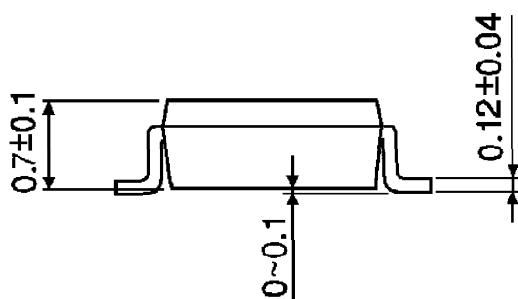
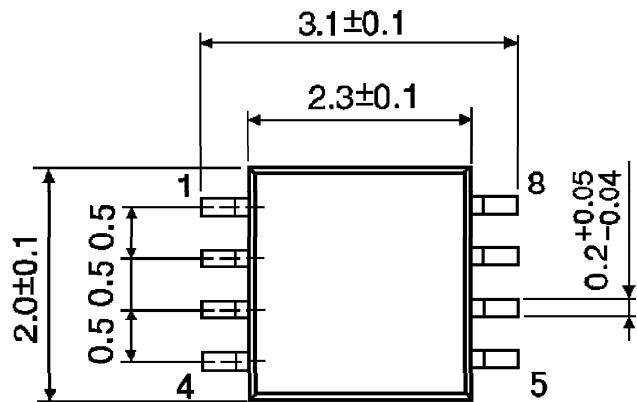


Weight : 0.02g (Typ.)

## PACKAGE DIMENSIONS

### SSOP8-P-0.50A

Unit : mm



Weight : 0.01g (Typ.)

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000707EBA

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