



CYPRESS

CY7C331

Asynchronous Registered EPLD

Features

- Twelve I/O macrocells each having:
 - One state flip-flop with an XOR sum-of-products input
 - One feedback flip-flop with input coming from the I/O pin
 - Independent (product term) set, reset, and clock inputs on all registers
 - Asynchronous bypass capability on all registers under product term control ($r = s = 1$)
 - Global or local output enable on three-state I/O
 - Feedback from either register to the array
- 192 product terms with variable distribution to macrocells
- 13 inputs, 12 feedback I/O pins, plus 6 shared I/O macrocell feedbacks for a total of 31 true and complementary inputs
- High speed: 20 ns maximum t_{PD}
- Security bit
- Space-saving 28-pin slim-line DIP package; also available in 28-pin PLCC

Low power

- 90 mA typical I_{CC} quiescent
- 180 mA I_{CC} maximum
- UV-erasable and reprogrammable
- Programming and operation 100% testable

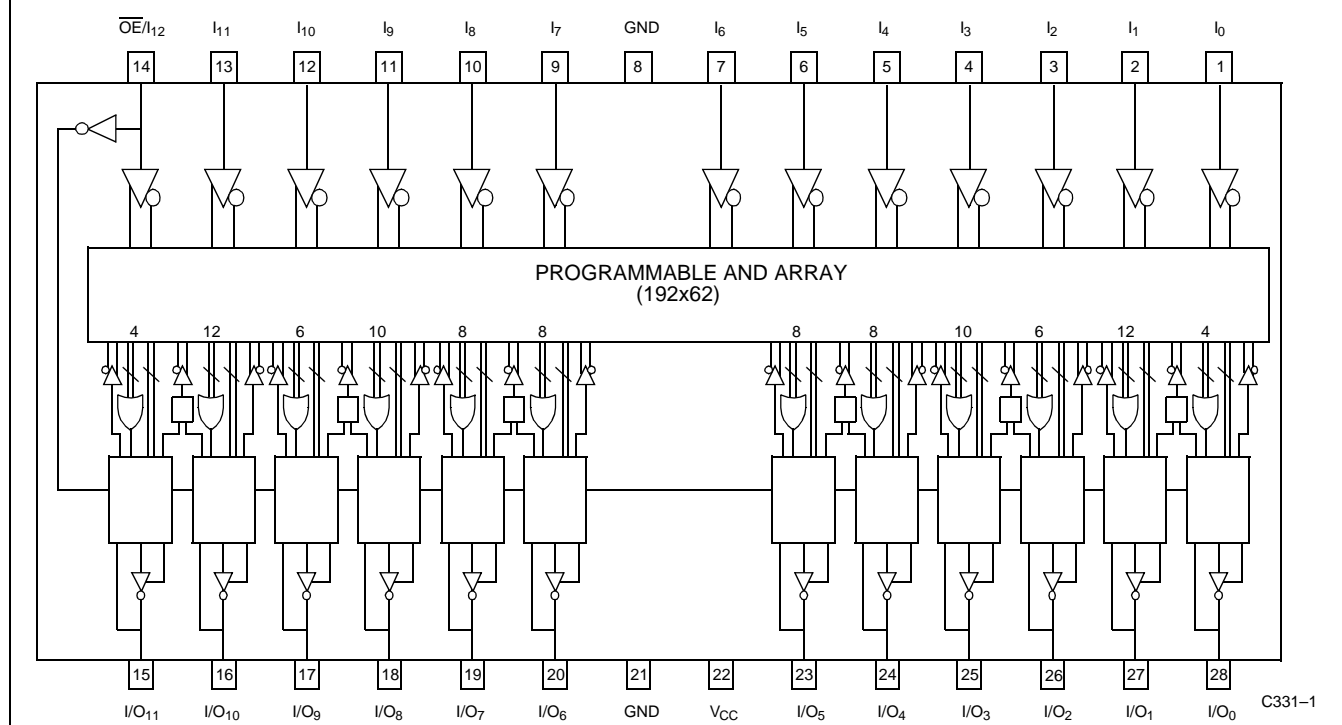
Functional Description

The CY7C331 is the most versatile PLD available for asynchronous designs. Central resources include twelve full D-type flip-flops with separate set, reset, and clock capability. For increased utility, XOR gates are provided at the D-inputs and the product term allocation per flip-flop is variably distributed.

I/O Resources

Pins 1 through 7 and 9 through 14 serve as array inputs; pin 14 may also be used as a global output enable for the I/O macrocell three-state outputs. Pins 15 through 20 and 23 through 28 are connected to I/O macrocells and may be managed as inputs or outputs depending on the configuration and the macrocell OE terms.

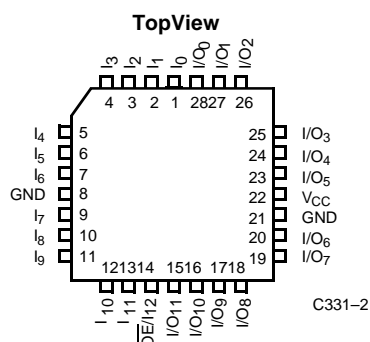
Logic Block Diagram



Selection Guide

| Generic Part Number | I_{CC1} (mA) | | t_{PD} (ns) | | t_S (ns) | | t_{CO} (ns) | |
|---------------------|----------------|-----|---------------|-----|------------|-----|---------------|-----|
| | Com'I | Mil | Com'I | Mil | Com'I | Mil | Com'I | Mil |
| CY7C331-20 | 130 | | 20 | | 12 | | 20 | |
| CY7C331-25 | 120 | 160 | 25 | 25 | 12 | 15 | 25 | 25 |
| CY7C331-30 | | 150 | | 30 | | 15 | | 30 |
| CY7C331-40 | | 150 | | 40 | | 20 | | 40 |

Pin Configuration



I/O Resources (continued)

It should be noted that there are two ground connections (pins 8 and 21) which, together with V_{CC} (pin 22) are located centrally on the package. The reason for this placement and dual-ground structure is to minimize the ground-loop noise when the outputs are driving simultaneously into a heavy capacitive load.

The CY7C331 has twelve I/O macrocells (see *Figure 1*). Each macrocell has two D-type flip-flops. One is fed from the array, and one from the I/O pin. For each flip-flop there are three dedicated product terms driving the R, S, and clock inputs, respectively. Each macrocell has one input to the array and for each pair of macrocells there is one shared input to the array. The macrocell input to the array may be configured to come from the 'Q' output of either flip-flop.

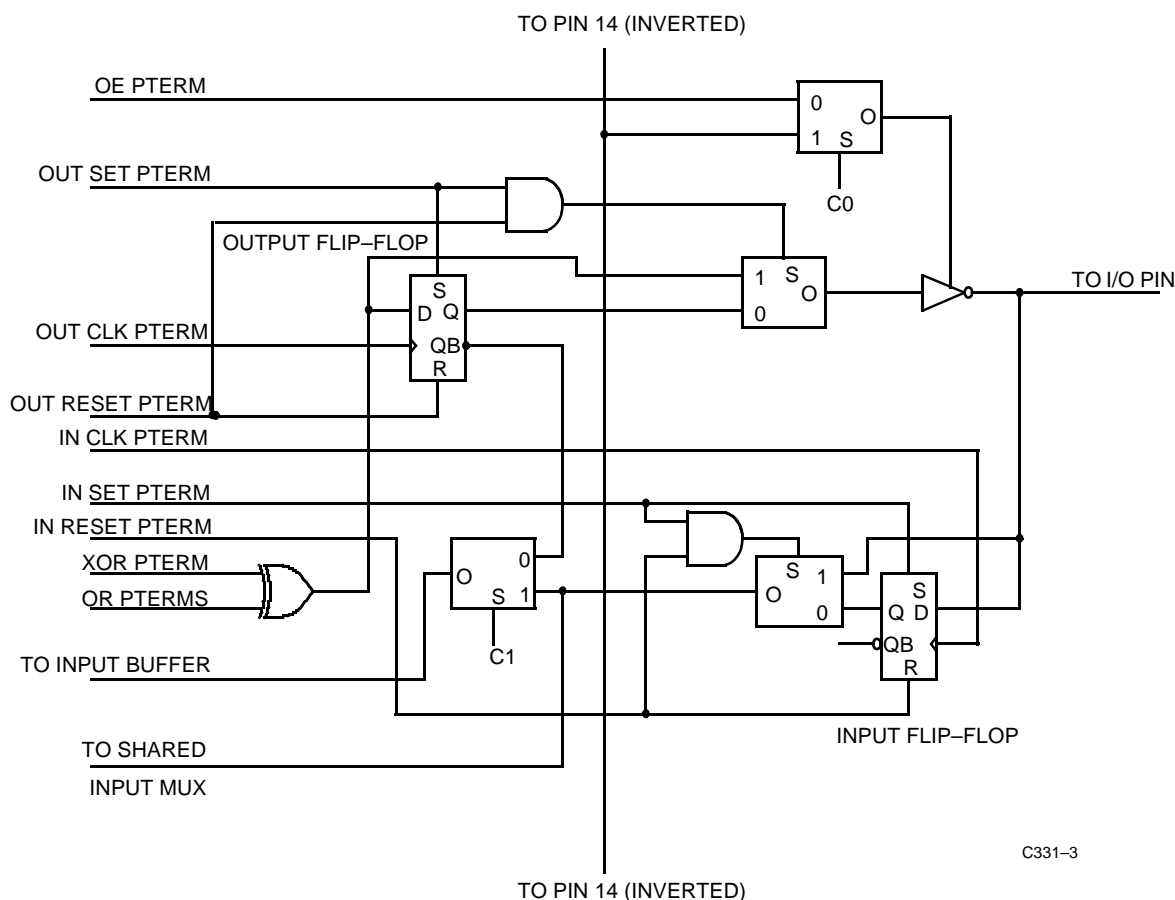


Figure 1. I/O Macrocell

I/O Resources (continued)

The D-type flip-flop that is fed from the array (i.e., the state flip-flop) has a logical XOR function on its input that combines a single product term with a sum (OR) of a number of product terms. The single product term is used to set the polarity of the output or to implement toggling (by including the current output in the product term).

The R and S inputs to the flip-flops override the current setting of the 'Q' output. The S input sets 'Q' true and the R input resets 'Q' (sets it false). If both R and S are asserted (true) at once, then the output will follow the input ('Q' = 'D') (see *Table 1*).

Table 1. RS Truth Table

| R | S | Q |
|---|---|---|
| 1 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 1 | D |

Shared Input Multiplexer

The input associated with each pair of macrocells may be configured by the shared input multiplexer to come from either macrocell; the 'Q' output of the flip-flop coming from the I/O pin is used as the input signal source (see *Figure 2*).

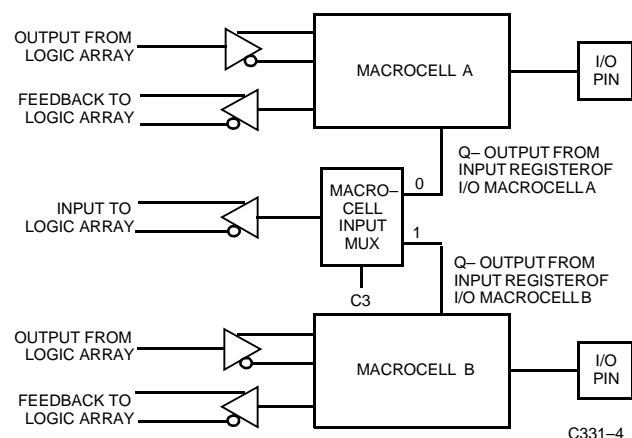
Product Term Distribution

The product terms are distributed to the macrocells such that 32 product terms are distributed between two adjacent macrocells.

The pairing of macrocells is the same as it is for the shared inputs. Eight of the product terms are used in each macrocell for set, reset, clock, output enable, and the upper part of the XOR gate. This leaves 16 product terms per pair of macrocells to be divided between the sum-of-products inputs to the two state registers. The following table shows the I/O pin pairing for shared inputs, and the product term (PT) allocation to macrocells associated with the I/O pins (see *Table 2*).

Table 2. . Product Term Distribution

| Macrocell | Pin Number | Product Terms |
|-----------|------------|---------------|
| 0 | 28 | 4 |
| 1 | 27 | 12 |
| 2 | 26 | 6 |
| 3 | 25 | 10 |
| 4 | 24 | 8 |
| 5 | 23 | 8 |
| 6 | 20 | 8 |
| 7 | 19 | 8 |
| 8 | 18 | 10 |
| 9 | 17 | 6 |
| 10 | 16 | 12 |
| 11 | 15 | 4 |


Figure 2. Shared Input Multiplexer

The CY7C331 is configured by three arrays of configuration bits (C0, C1, C2). For each macrocell, there is one C0 bit and one C1 bit. For each pair of macrocells there is one C2 bit.

There are twelve C0 bits, one for each macrocell. If C0 is programmed for a macrocell, then the three-state enable (OE) will be controlled by pin 14 (the global OE). If C0 is not programmed, then the OE product term for that macrocell will be used.

There are twelve C1 bits, one for each macrocell. The C1 bit selects inputs for the product term (PT) array from either the state register (if the bit is unprogrammed) or the input register (if the bit is programmed).

There are six C2 bits, providing one C2 bit for each pair of macrocells. The C2 bit controls the shared input multiplexer; if the C2 bit is not programmed, then the input to the product term array comes from the upper macrocell (A). If the C2 bit is programmed, then the input comes from the lower macrocell (B).

The timing diagrams for the CY7C331 cover state register, input register, and various combinational delays. Since internal clocks are the outputs of product terms, all timing is from the transition of the inputs causing the clock transition.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential
(Pin 28 to Pin 8 or 21)..... -0.5V to +7.0V

DC Input Voltage..... -3.0V to +7.0V

Output Current into Outputs (LOW) 12 mA

Static Discharge Voltage >1500V
(per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

DC Programming Voltage..... 13.0 V

Operating Range

| Range | Ambient Temperature | V _{CC} |
|-------------------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Military ^[1] | -55°C to +125°C | 5V ± 10% |

Electrical Characteristics Over the Operating Range^[2]

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|------------------|---|--|--------------|------|------|
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -3.2 mA (Com'l), I _{OH} = -2 mA (Mil) | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 12 mA (Com'l), I _{OL} = 8 mA (Mil) | | 0.5 | V |
| V _{IH} | Input HIGH Voltage | Guaranteed HIGH Input, all Inputs ^[3] | 2.2 | | V |
| V _{IL} | Input LOW Voltage | Guaranteed LOW Input, all Inputs ^[3] | | 0.8 | V |
| I _{IX} | Input Leakage Current | V _{SS} < V _{IN} < V _{CC} , V _{CC} = Max. | -10 | +10 | μA |
| I _{OZ} | Output Leakage Current | V _{SS} < V _{OUT} < V _{CC} , V _{CC} = Max. | -40 | +40 | μA |
| I _{SC} | Output Short Circuit Current ^[4] | V _{CC} = Max., V _{OUT} = 0.5V ^[5] | -30 | -90 | mA |
| I _{CC1} | Standby Power Supply Current | V _{CC} = Max., V _{IN} = GND, Outputs Open | Com'l -20 | 130 | mA |
| | | | Com'l -25 | 120 | |
| | | | Mil -25 | 160 | mA |
| | | | Mil -30, -40 | 150 | |
| I _{CC2} | Power Supply Current at Frequency ^[4, 6] | V _{CC} = Max., Outputs Disabled (in High Z State) Device Operating at f _{MAX} External (f _{MAX1}) | Com'l | 180 | mA |
| | | | Mil | 200 | |

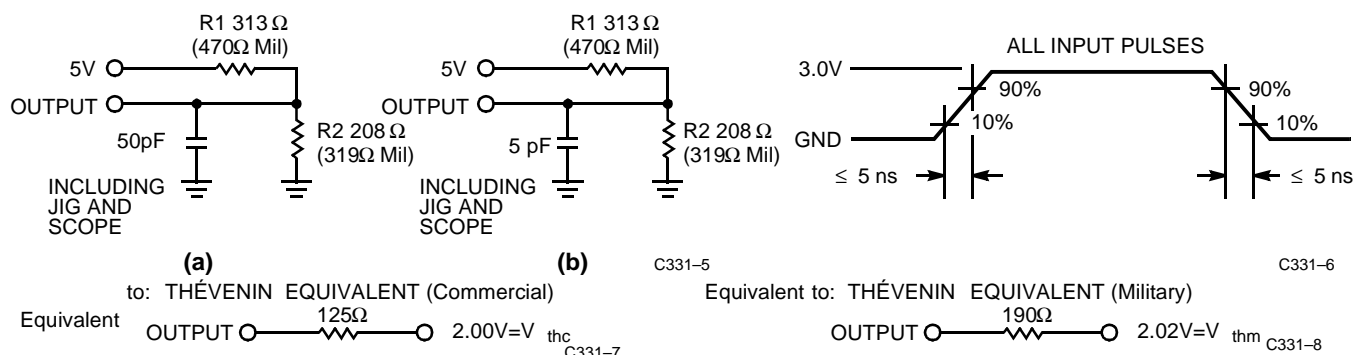
Capacitance^[4]

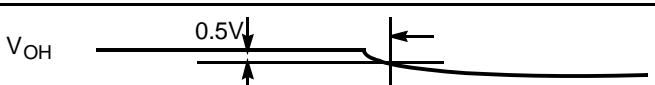
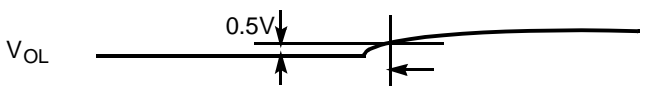
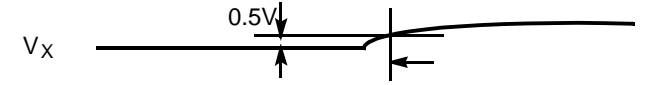
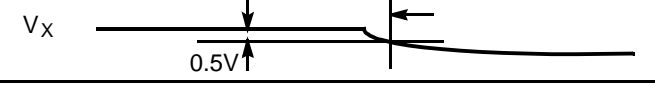
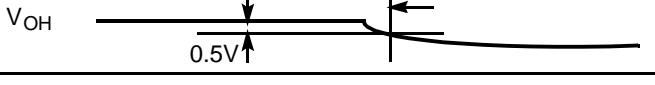
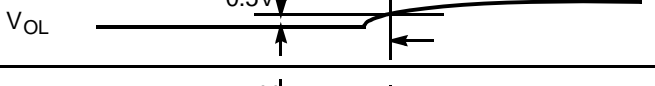
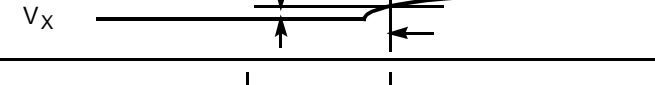
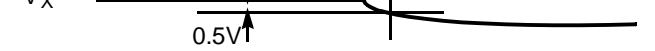
| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|--------------------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 2.0V at f = 1 MHz | 10 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 2.0V at f = 1 MHz | 10 | pF |

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
4. Tested initially and after any design or process changes that may affect these parameters.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
6. Because these input signals are controlled by product terms, active input polarity may be of either polarity. Internal active input polarity has been shown for clarity.

AC Test Loads and Waveforms



| Parameter | V _X | Output Waveform—Measurement Level |
|----------------------|------------------|---|
| t _{PXZ} (-) | 1.5V |  C331-9 |
| t _{PXZ} (+) | 2.6V |  C331-10 |
| t _{PZX} (+) | V _{thc} |  C331-11 |
| t _{PZX} (-) | V _{thc} |  C331-12 |
| t _{ER} (-) | 1.5V |  C331-13 |
| t _{ER} (+) | 2.6V |  C331-14 |
| t _{EA} (+) | V _{thc} |  C331-15 |
| t _{EA} (-) | V _{thc} |  C331-16 |

(c) Test Waveforms and Measurement Levels

Switching Characteristics Over the Operating Range^[2]

| Parameter | Description | Commercial | | | | Unit |
|------------------|--|------------|------|------|------|------|
| | | −20 | | −25 | | |
| | | Min. | Max. | Min. | Max. | |
| t _{PD} | Input to Output Propagation Delay ^[7] | | 20 | | 25 | ns |
| t _{ICO} | Input Register Clock to Output Delay ^[8] | | 35 | | 40 | ns |
| t _{IOH} | Output Data Stable Time from Input Clock ^[8] | 5 | | 5 | | ns |
| t _{IS} | Input or Feedback Set-Up Time to Input Register Clock ^[8] | 2 | | 2 | | ns |
| t _{IH} | Input Register Hold Time from Input Clock ^[8] | 11 | | 13 | | ns |
| t _{IAR} | Input to Input Register Asynchronous Reset Delay ^[8] | | 35 | | 40 | ns |

Switching Characteristics Over the Operating Range^[2] (continued)

| Parameter | Description | Commercial | | | | Unit |
|---------------------------------------|--|------------|------|------|------|------|
| | | –20 | | –25 | | |
| | | Min. | Max. | Min. | Max. | |
| t _{IRW} | Input Register Reset Width ^[4, 8] | 35 | | 40 | | ns |
| t _{IRR} | Input Register Reset Recovery Time ^[4, 8] | 35 | | 40 | | ns |
| t _{IAS} | Input to Input Register Asynchronous Set Delay ^[8] | | 35 | | 40 | ns |
| t _{ISW} | Input Register Set Width ^[4, 8] | 35 | | 40 | | ns |
| t _{ISR} | Input Register Set Recovery Time ^[4, 8] | 35 | | 40 | | ns |
| t _{WH} | Input and Output Clock Width HIGH ^[8, 9, 10] | 12 | | 15 | | ns |
| t _{WL} | Input and Output Clock Width LOW ^[8, 9, 10] | 12 | | 15 | | ns |
| f _{MAX1} | Maximum Frequency with Feedback in Input Registered Mode (1/(t _{ICO} + t _{IS})) ^[11] | 27.0 | | 23.8 | | MHz |
| f _{MAX2} | Maximum Frequency Data Path in Input Registered Mode (Lowest of 1/t _{ICO} , 1/(t _{WH} + t _{WL}), or 1/(t _{IS} + t _{IH})) ^[8] | 28.5 | | 25.0 | | MHz |
| t _{IOH} –t _{IH} 33X | Output Data Stable from Input Clock Minus Input Register Input Hold Time for 7C335 ^[12, 13] | 0 | | 0 | | ns |
| t _{CO} | Output Register Clock to Output Delay ^[9] | | 20 | | 25 | ns |
| t _{OH} | Output Data Stable Time from Output Clock ^[9] | 3 | | 3 | | ns |
| t _S | Output Register Input Set-Up Time to Output Clock ^[9] | 12 | | 12 | | ns |
| t _H | Output Register Input Hold Time from Output Clock ^[9] | 8 | | 8 | | ns |
| t _{OAR} | Input to Output Register Asynchronous Reset Delay ^[9] | | 20 | | 25 | ns |
| t _{ORW} | Output Register Reset Width ^[9] | 20 | | 25 | | ns |
| t _{ORR} | Output Register Reset Recovery Time ^[9] | 20 | | 25 | | ns |
| t _{OAS} | Input to Output Register Asynchronous Set Delay ^[9] | | 20 | | 25 | ns |
| t _{OSW} | Output Register Set Width ^[9] | 20 | | 25 | | ns |
| t _{OSR} | Output Register Set Recovery Time ^[9] | 20 | | 25 | | ns |
| t _{EA} | Input to Output Enable Delay ^[14, 15] | | 25 | | 25 | ns |
| t _{ER} | Input to Output Disable Delay ^[14, 15] | | 25 | | 25 | ns |
| t _{PZX} | Pin 14 to Output Enable Delay ^[14, 15] | | 20 | | 20 | ns |
| t _{PXZ} | Pin 14 to Output Disable Delay ^[14, 15] | | 20 | | 20 | ns |
| f _{MAX3} | Maximum Frequency with Feedback in Output Registered Mode (1/(t _{CO} + t _S)) ^[16, 17] | 31.2 | | 27.0 | | MHz |
| f _{MAX4} | Maximum Frequency Data Path in Output Registered Mode (Lowest of 1/t _{CO} , 1/(t _{WH} + t _{WL}), or 1/(t _S + t _H)) ^[9] | 41.6 | | 33.3 | | MHz |
| t _{OH} –t _{IH} 33X | Output Data Stable from Output Clock Minus Input Register Input Hold Time for 7C335 ^[13, 18] | 0 | | 0 | | ns |
| f _{MAX5} | Maximum Frequency Pipelined Mode ^[10, 17] | 35.0 | | 30.0 | | MHz |

Notes:

7. Refer to Figure 3, configuration 1.
8. Refer to Figure 3, configuration 2.
9. Refer to Figure 3, configuration 3.
10. Refer to Figure 3, configuration 6.
11. Refer to Figure 3, configuration 7.
12. Refer to Figure 3, configuration 9.
13. This specification is intended to guarantee interface compatibility of the other members of the CY7C330 family with the CY7C331. This specification is met for the devices noted operating at the same ambient temperature and at the same power supply voltage. These parameters are tested periodically by sampling of production product.
14. Part (a) of AC Test Loads and Waveforms used for all parameters except t_{PZX} , t_{PXZ} , t_{PZX} , and t_{PXZ} , which use part (b). Part (c) shows the test waveforms and measurement levels.
15. Refer to Figure 3, configuration 4.
16. Refer to Figure 3, configuration 8.
17. This specification is intended to guarantee that a state machine configuration created with internal or external feedback can be operated with output register and input register clocks controlled by the same source. These parameters are tested by periodic sampling of production product.

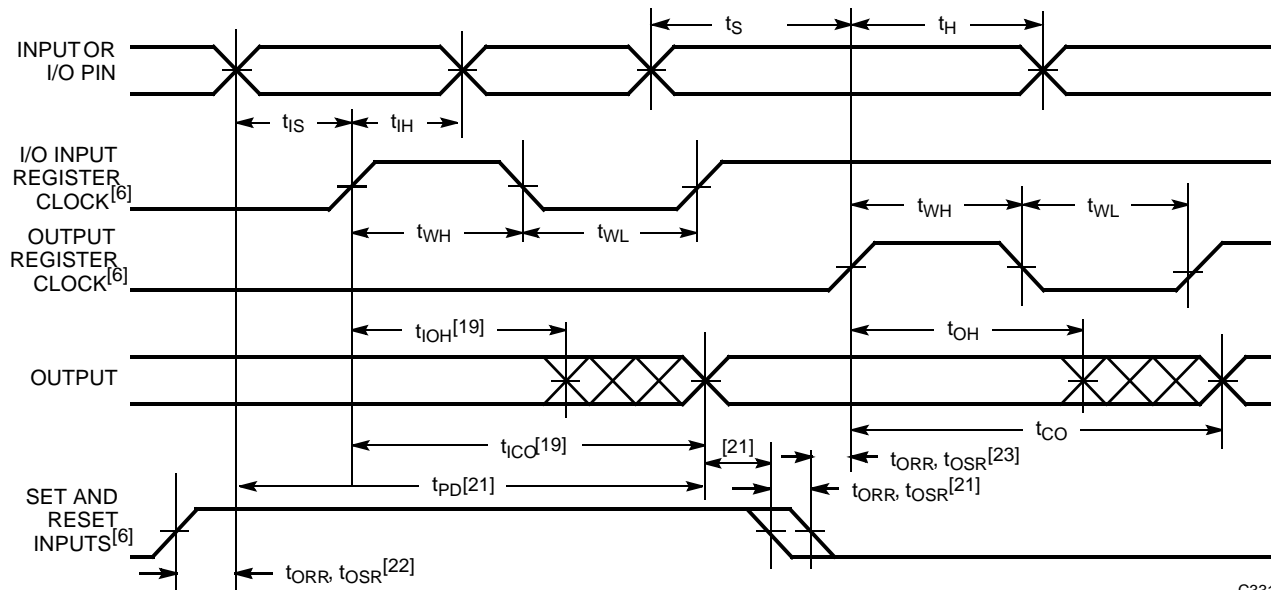
Switching Characteristics Over the Operating Range^[2] (continued)

| Parameter | Description | Military | | | | | | Unit |
|---------------------------------------|--|----------|------|------|------|------|------|------|
| | | [20] −25 | | −30 | | −40 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{PD} | Input to Output Propagation Delay ^[7] | | 25 | | 30 | | 40 | ns |
| t _{ICO} | Input Register Clock to Output Delay ^[4, 8] | | 45 | | 50 | | 65 | ns |
| t _{IOH} | Output Data Stable Time from Input Clock ^[4, 8] | 5 | | 5 | | 5 | | ns |
| t _{IS} | Input or Feedback Set-Up Time to Input Register Clock ^[8] | 5 | | 5 | | 5 | | ns |
| t _{IH} | Input Register Hold Time from Input Clock ^[4, 8] | 13 | | 15 | | 20 | | ns |
| t _{IAR} | Input to Input Register Asynchronous Reset Delay ^[4, 8] | | 45 | | 50 | | 65 | ns |
| t _{IRW} | Input Register Reset Width ^[8] | 45 | | 50 | | 65 | | ns |
| t _{IRR} | Input Register Reset Recovery Time ^[8] | 45 | | 50 | | 65 | | ns |
| t _{IAS} | Input to Input Register Asynchronous Set Delay ^[8] | | 45 | | 50 | | 65 | ns |
| t _{ISW} | Input Register Set Width ^[8] | 45 | | 50 | | 65 | | ns |
| t _{ISR} | Input Register Set Recovery Time ^[8] | 45 | | 50 | | 65 | | ns |
| t _{WH} | Input and Output Clock Width High ^[8, 9, 10] | 15 | | 20 | | 25 | | ns |
| t _{WL} | Input and Output Clock Width Low ^[8, 9, 10] | 15 | | 20 | | 25 | | ns |
| f _{MAX1} | Maximum frequency with Feedback in Input Registered Mode (1/(t _{ICO} + t _{IS})) ^[11] | 20.0 | | 18.1 | | 14.2 | | MHz |
| f _{MAX2} | Maximum frequency Data Path in Input Registered Mode (Lowest of 1/t _{ICO} , 1/(t _{WH} + t _{WL}), or 1/(t _{IS} + t _{IH})) ^[8] | 22.2 | | 20.0 | | 15.3 | | MHz |
| t _{IOH} −t _{IH} 33X | Output Data Stable from Input Clock Minus Input Register Input Hold Time for 7C335 ^[12, 13] | 0 | | 0 | | 0 | | ns |
| t _{CO} | Output Register Clock to Output Delay ^[9] | | 25 | | 30 | | 40 | ns |
| t _{OH} | Output Data Stable Time from Output Clock ^[9] | 3 | | 3 | | 3 | | ns |
| t _S | Output Register Input Set-Up Time to Output Clock ^[9] | 15 | | 15 | | 20 | | ns |
| t _H | Output Register Input Hold Time from Output Clock ^[9] | 10 | | 10 | | 12 | | ns |
| t _{OAR} | Input to Output Register Asynchronous Reset Delay ^[9] | | 25 | | 30 | | 40 | ns |
| t _{ORW} | Output Register Reset Width ^[9] | 25 | | 30 | | 40 | | ns |
| t _{ORR} | Output Register Reset Recovery Time ^[9] | 25 | | 30 | | 40 | | ns |
| t _{OAS} | Input to Output Register Asynchronous Set Delay ^[9] | | 25 | | 30 | | 40 | ns |
| t _{OSW} | Output Register Set Width ^[9] | 25 | | 30 | | 40 | | ns |
| t _{OSR} | Output Register Set Recovery Time ^[9] | 25 | | 30 | | 40 | | ns |
| t _{EA} | Input to Output Enable Delay ^[14, 15] | | 25 | | 30 | | 40 | ns |
| t _{ER} | Input to Output Disable Delay ^[14, 15] | | 25 | | 30 | | 40 | ns |
| t _{PZX} | Pin 14 to Output Enable Delay ^[14, 15] | | 20 | | 25 | | 35 | ns |
| t _{PXZ} | Pin 14 to Output Disable Delay ^[14, 15] | | 20 | | 25 | | 35 | ns |
| f _{MAX3} | Maximum Frequency with Feedback in Output Registered Mode)1/(t _{CO} + t _S)) ^[16, 17] | 25.0 | | 22.2 | | 16.6 | | MHz |
| f _{MAX4} | Maximum Frequency Data Path in Output Registered Mode (Lowest of 1/t _{CO} , 1/(t _{WH} + t _{WL}), or 1/(t _S + t _H)) ^[9] | 33.3 | | 25.0 | | 20.0 | | MHz |
| t _{OH} −t _{IH} 33X | Output Data Stable from Output Clock Minus Input Register Input Hold Time for 7C335 ^[13, 18] | 0 | | 0 | | 0 | | ns |
| f _{MAX5} | Maximum Frequency Pipelined Mode ^[10, 17] | 28.0 | | 23.5 | | 18.5 | | MHz |

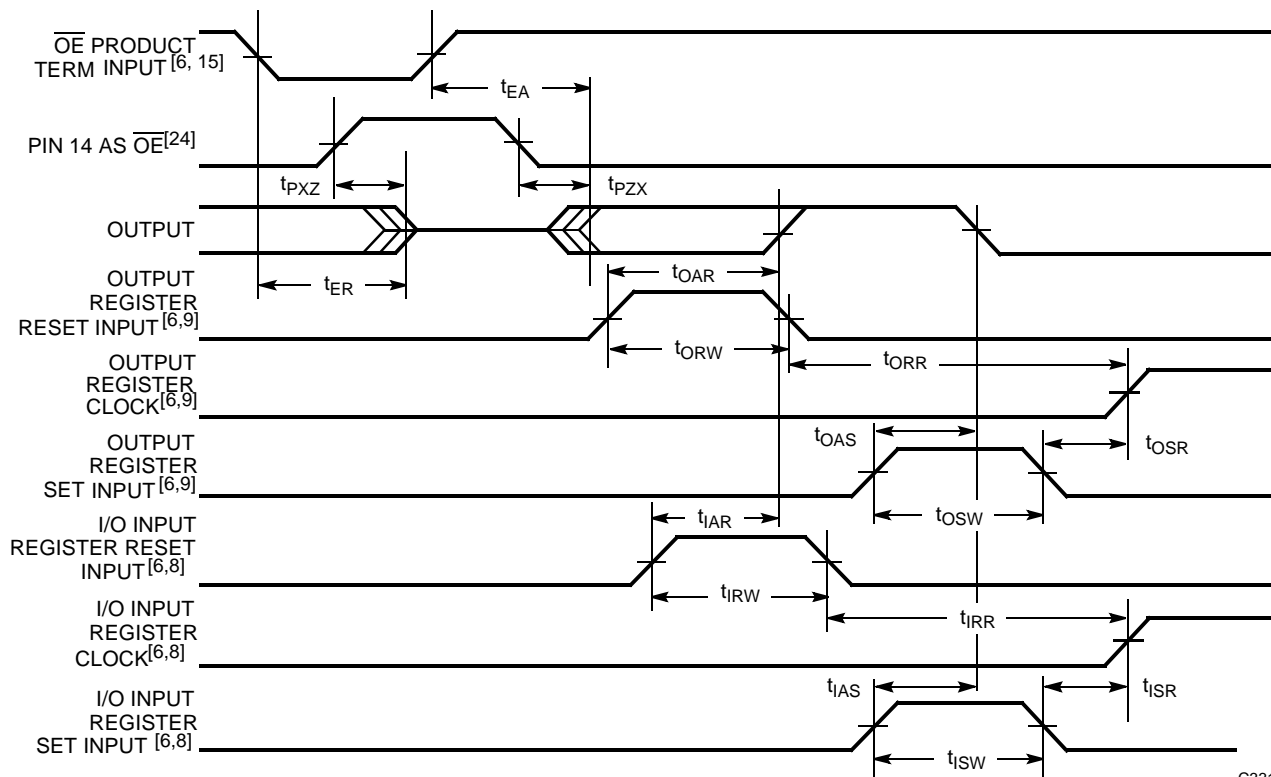
Note:

18. Refer to Figure 3, configuration 10.

Switching Waveforms



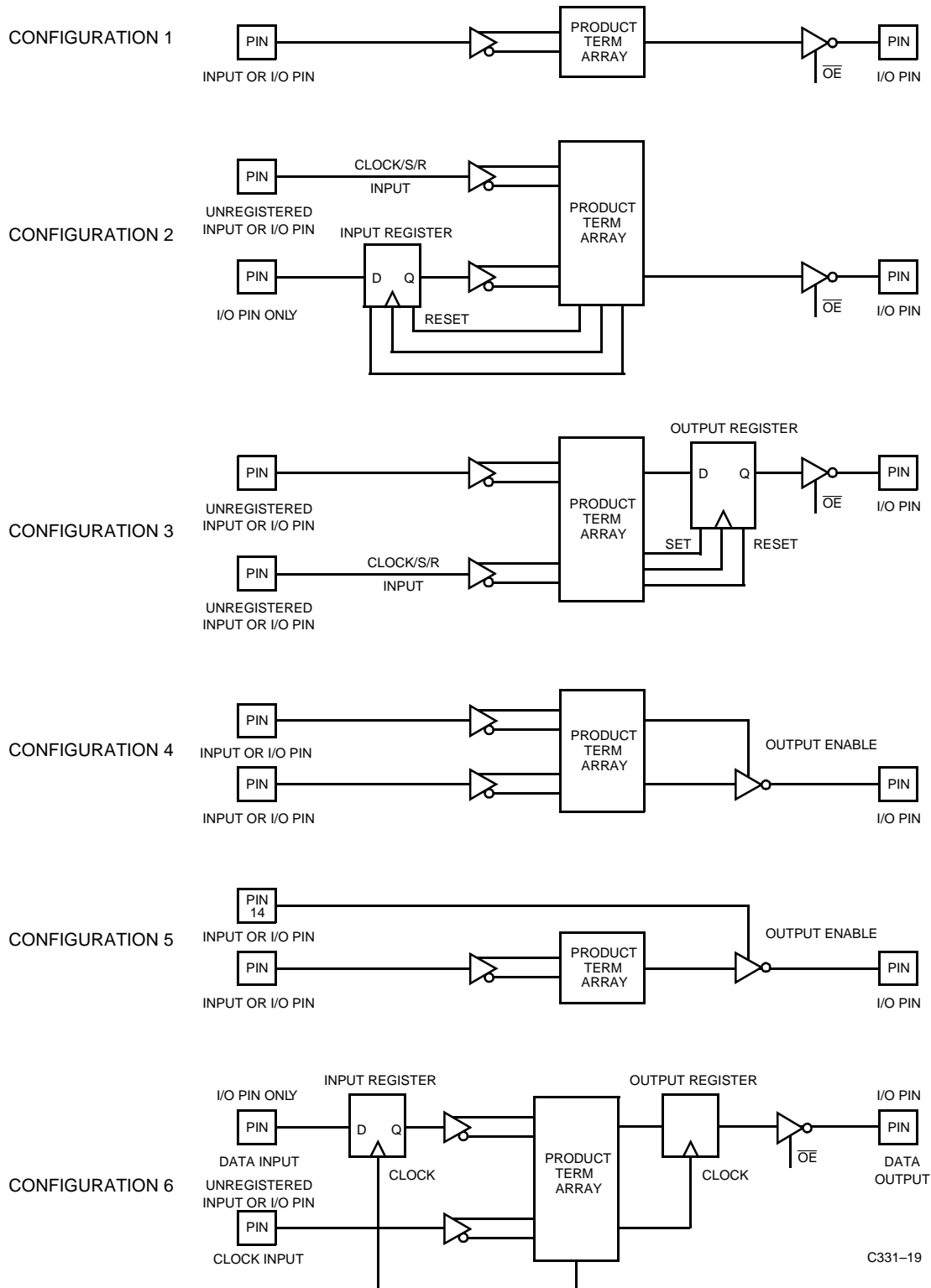
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C331-18

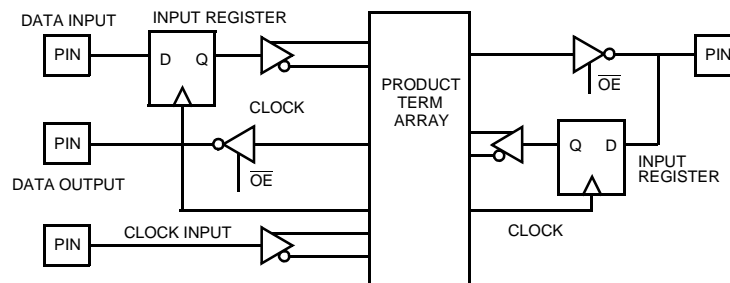
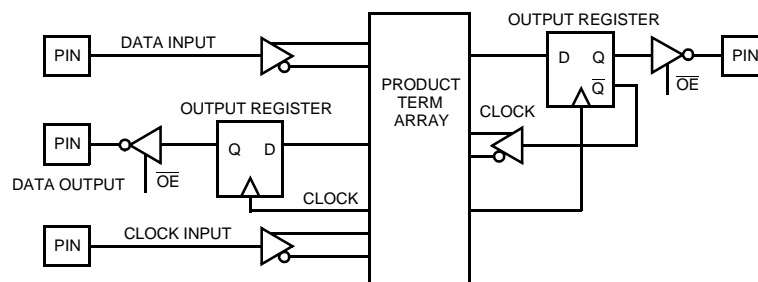
Notes:

19. Output register is set in Transparent mode. Output register set and reset inputs are in a HIGH state.
20. Dedicated input or input register set in Transparent mode. Input register set and reset inputs are in a HIGH state.
21. Combinatorial Mode. Reset and set inputs of the input and output registers should remain in a HIGH state at least until the output responds at t_{PD} . When returning set and reset inputs to a LOW state, one of these signals should go LOW a minimum of t_{OSR} (set input) or t_{ORR} (reset input) prior to the other. This guarantees predictable register states upon exit from Combinatorial mode.
22. When entering the Combinatorial mode, input and output register set and reset inputs must be stable in a HIGH state a minimum of t_{ISR} or t_{IRR} and t_{OSR} or t_{ORR} respectively prior to application of logic input signals.
23. When returning to the input and/or output Registered mode, register set and reset inputs must be stable in a LOW state a minimum of t_{ISR} or t_{IRR} and t_{OSR} or t_{ORR} respectively prior to the application of the register clock input.
24. Refer to Figure 3, configuration 5.

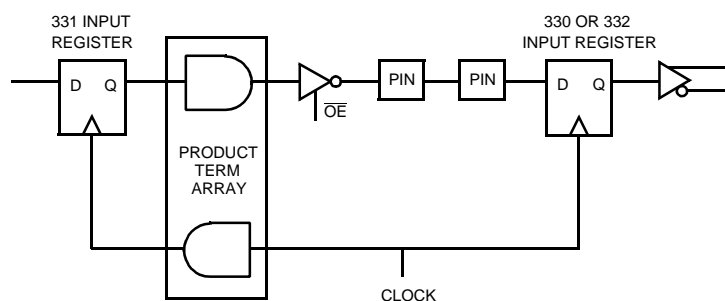
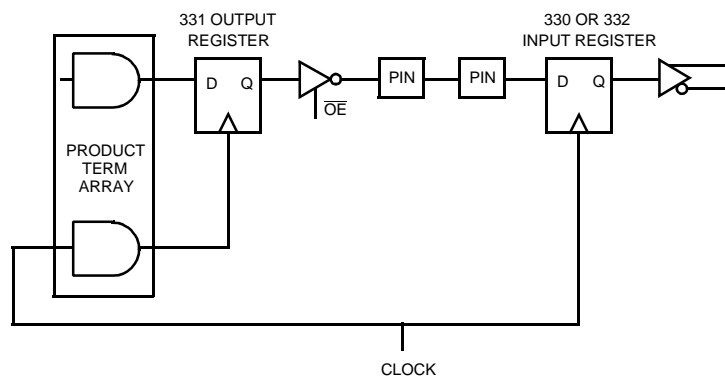


C331-19

Figure 3. Timing Configurations

CONFIGURATION 7

CONFIGURATION 8


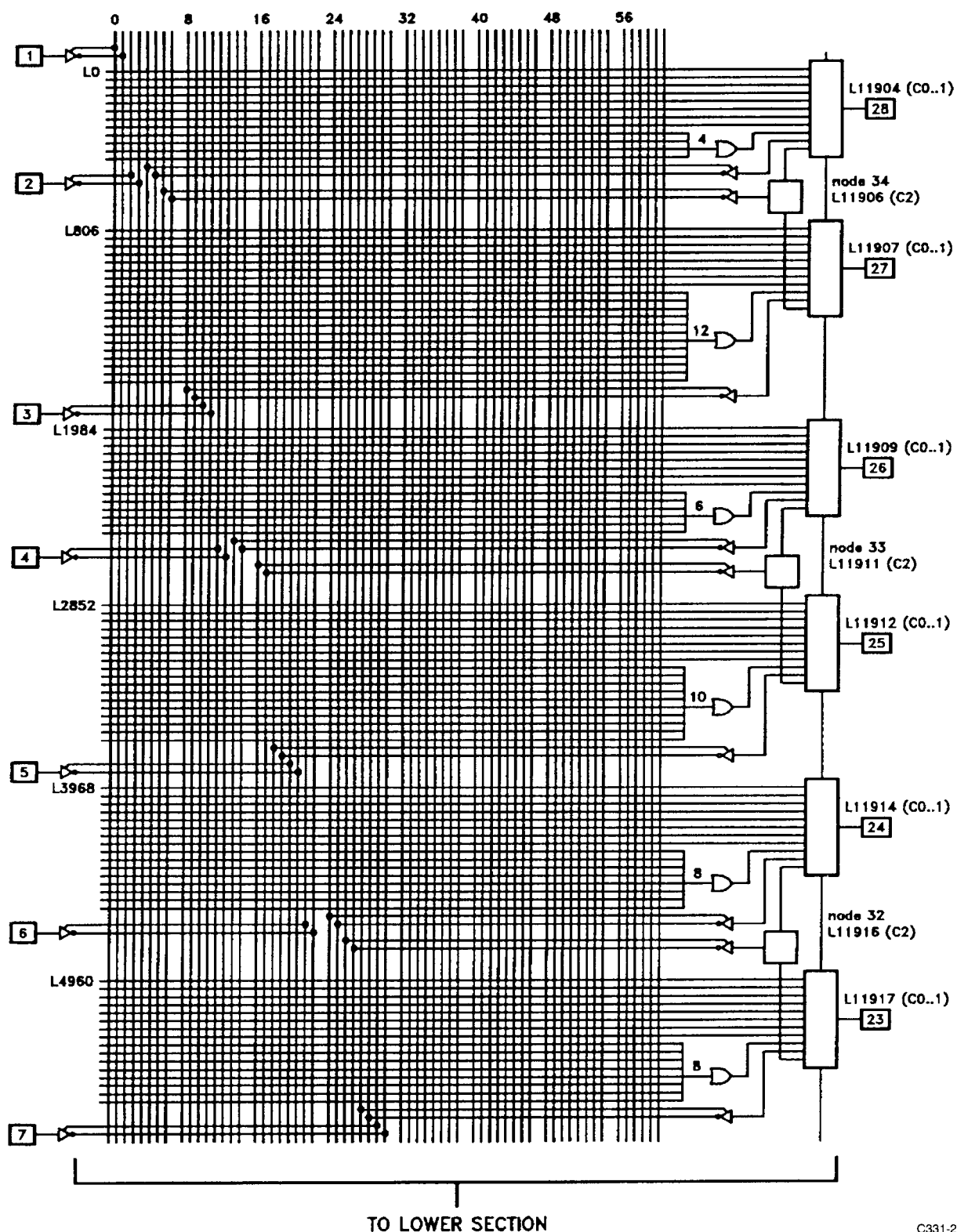
C331-20

CONFIGURATION 9

CONFIGURATION 10


C331-21

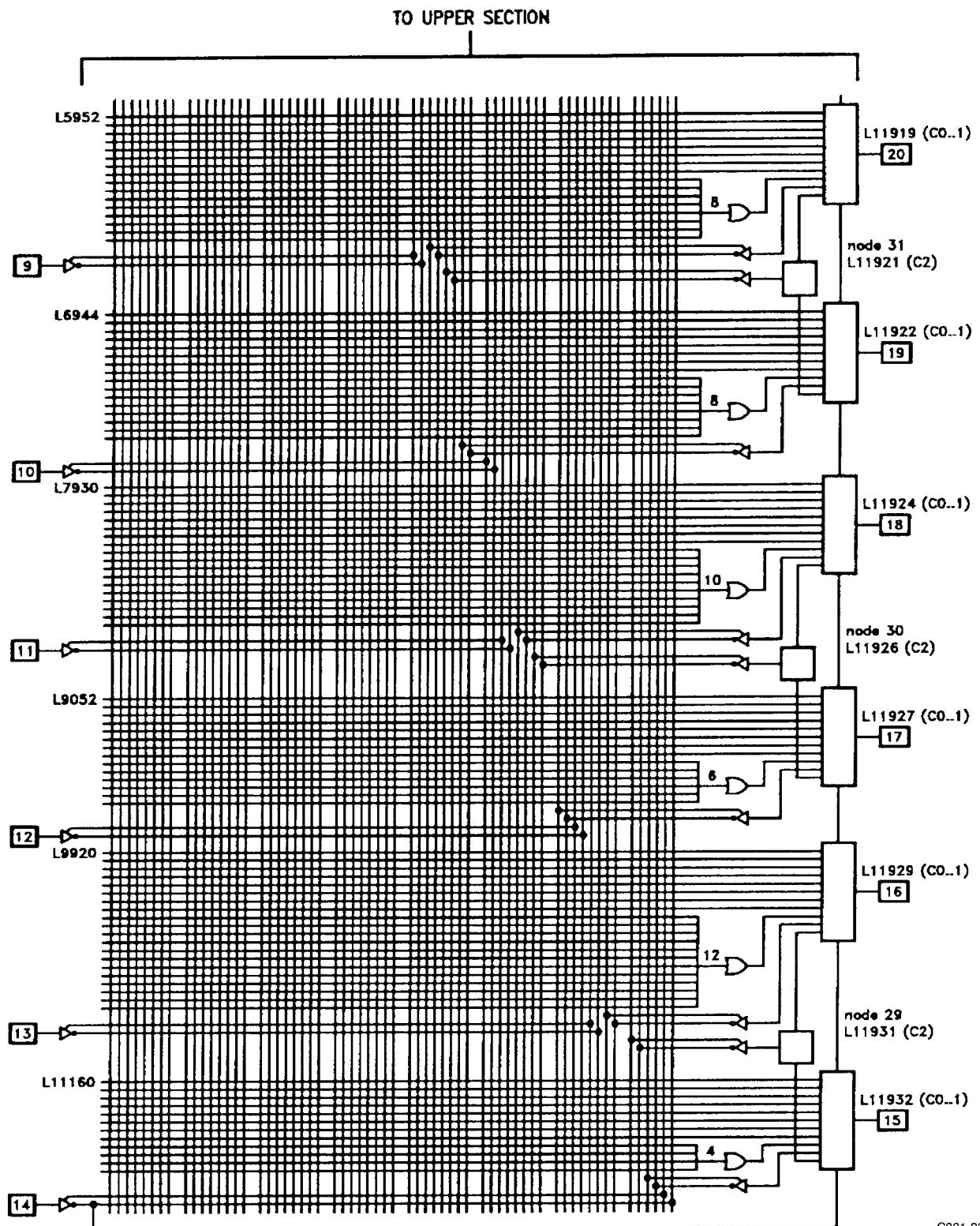
Figure 3. Timing Configurations (continued)

CY7C331 Logic Diagram (Upper Half)



C331-22

CY7C331 Logic Diagram (Lower Half)



C331-23

Ordering Information

| I_{CC1} (mA) | t_{PD} (ns) | t_S (ns) | t_{CO} (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|-------------------|------------------|---------------|------------------|---------------|--------------|---------------------------------------|-----------------|
| 130 | 20 | 12 | 20 | CY7C331-20HC | H64 | 28-Pin Windowed Leaded Chip Carrier | Commercial |
| | | | | CY7C331-20JC | J64 | 28-Lead Plastic Leaded Chip Carrier | |
| | | | | CY7C331-20PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | | | | CY7C331-20WC | W22 | 28-Lead (300-Mil) Windowed CerDIP | |
| 160 | 25 | 15 | 25 | CY7C331-25DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | | | | CY7C331-25HMB | H64 | 28-Pin Windowed Leaded Chip Carrier | |
| | | | | CY7C331-25LMB | L64 | 28-Square Leadless Chip Carrier | |
| | | | | CY7C331-25QMB | Q64 | 28-Pin Windowed Leadless Chip Carrier | |
| | | | | CY7C331-25TMB | T74 | 28-Lead Windowed Cerpack | |
| | | | | CY7C331-25WMB | W22 | 28-Lead (300-Mil) Windowed CerDIP | |
| 120 | 25 | 12 | 25 | CY7C331-25HC | H64 | 28-Pin Windowed Leaded Chip Carrier | Commercial |
| | | | | CY7C331-25JC | J64 | 28-Lead Plastic Leaded Chip Carrier | |
| | | | | CY7C331-25PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | | | | CY7C331-25WC | W22 | 28-Lead (300-Mil) Windowed CerDIP | |
| 150 | 30 | 15 | 30 | CY7C331-30DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | | | | CY7C331-30HMB | H64 | 28-Pin Windowed Leaded Chip Carrier | |
| | | | | CY7C331-30LMB | L64 | 28-Square Leadless Chip Carrier | |
| | | | | CY7C331-30QMB | Q64 | 28-Pin Windowed Leadless Chip Carrier | |
| | | | | CY7C331-30TMB | T74 | 28-Lead Windowed Cerpack | |
| | | | | CY7C331-30WMB | W22 | 28-Lead (300-Mil) Windowed CerDIP | |
| 150 | 40 | 20 | 40 | CY7C331-40DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | | | | CY7C331-40HMB | H64 | 28-Pin Windowed Leaded Chip Carrier | |
| | | | | CY7C331-40LMB | L64 | 28-Square Leadless Chip Carrier | |
| | | | | CY7C331-40QMB | Q64 | 28-Pin Windowed Leadless Chip Carrier | |
| | | | | CY7C331-40TMB | T74 | 28-Lead Windowed Cerpack | |
| | | | | CY7C331-40WMB | W22 | 28-Lead (300-Mil) Windowed CerDIP | |

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

| Parameter | Subgroups |
|-----------|-----------|
| V_{OH} | 1, 2, 3 |
| V_{OL} | 1, 2, 3 |
| V_{IH} | 1, 2, 3 |
| V_{IL} | 1, 2, 3 |
| I_{IX} | 1, 2, 3 |
| I_{OZ} | 1, 2, 3 |
| I_{CC1} | 1, 2, 3 |

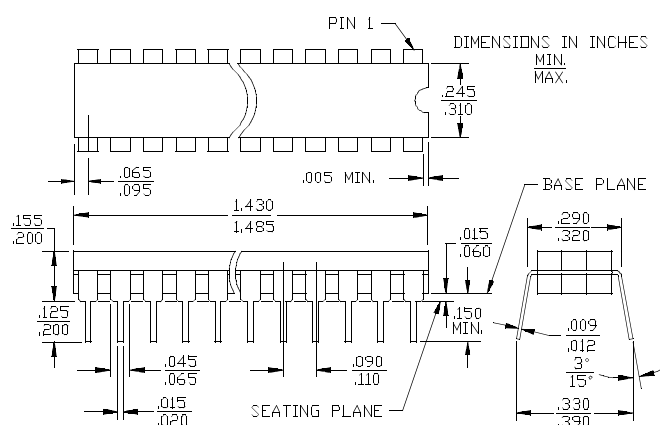
Switching Characteristics

| Parameter | Subgroups |
|-----------|-----------|
| t_{IS} | 9, 10, 11 |
| t_{IH} | 9, 10, 11 |
| t_{WH} | 9, 10, 11 |
| t_{WL} | 9, 10, 11 |
| t_{CO} | 9, 10, 11 |
| t_{PD} | 9, 10, 11 |
| t_{IAR} | 9, 10, 11 |
| t_{IAS} | 9, 10, 11 |
| t_{PXZ} | 9, 10, 11 |
| t_{PZX} | 9, 10, 11 |
| t_{ER} | 9, 10, 11 |
| t_{EA} | 9, 10, 11 |
| t_S | 9, 10, 11 |
| t_H | 9, 10, 11 |

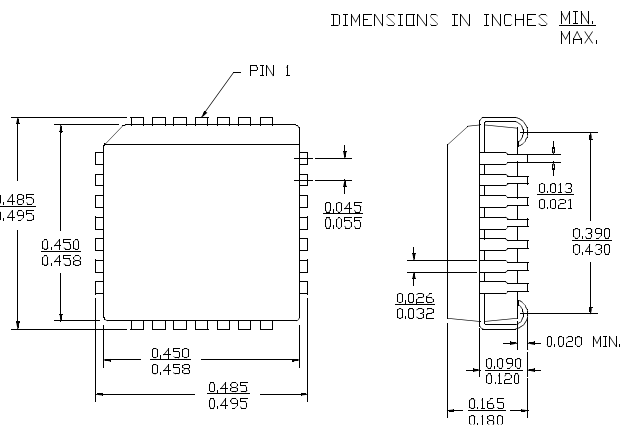
Package Diagrams

28-Lead (300-Mil) CerDIP D22

MIL-STD-1835 D-15 Config. A

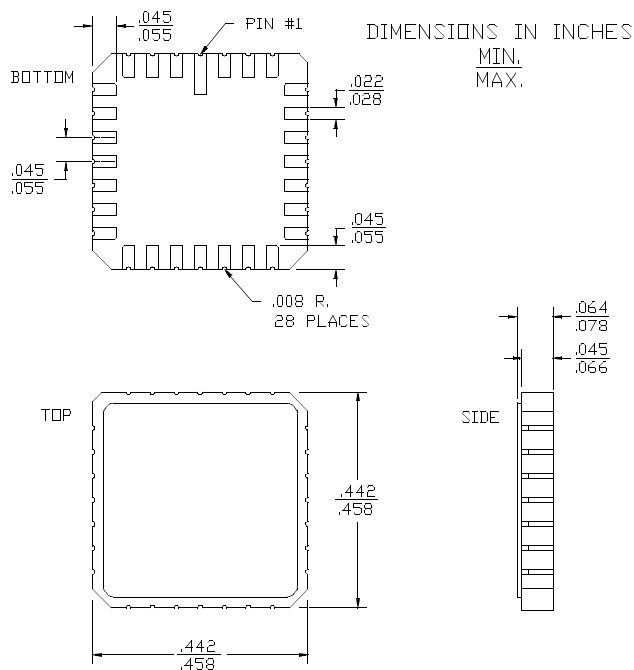


28-Lead Plastic Leaded Chip Carrier J64



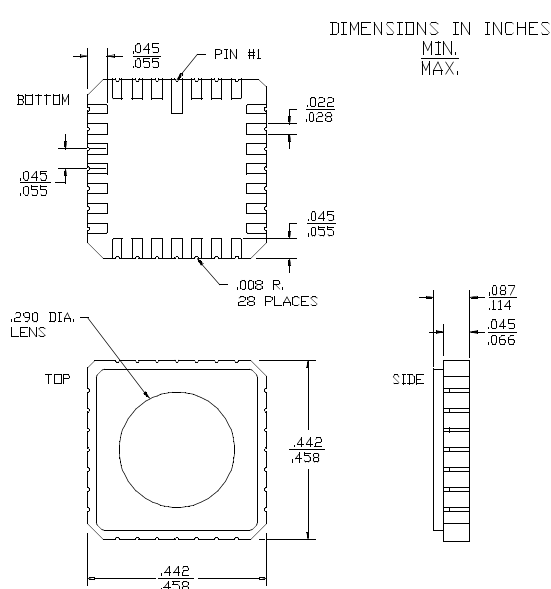
28-Square Leadless Chip Carrier L64

MIL-STD-1835 C-4



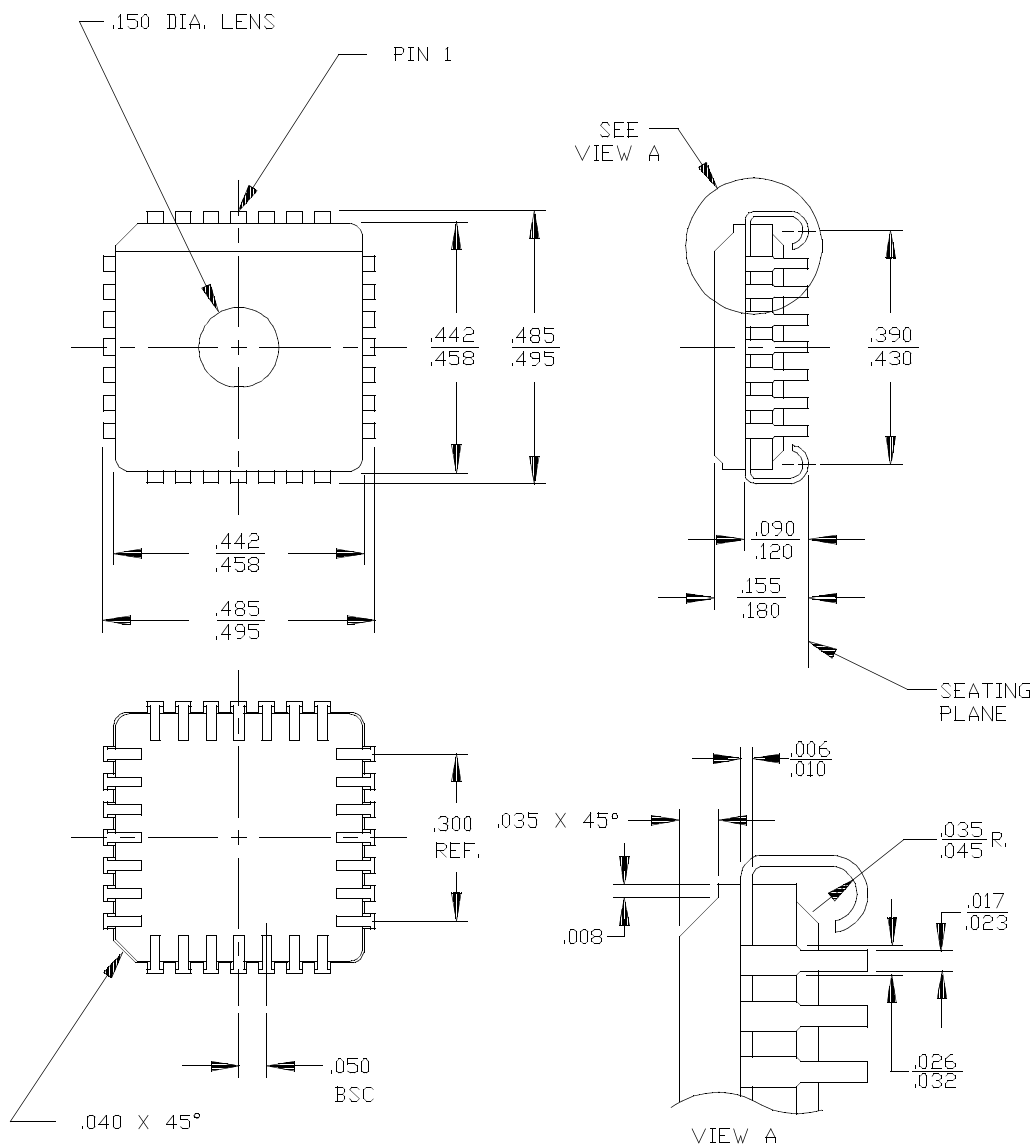
28-Pin Windowed Leadless Chip Carrier Q64

MIL-STD-1835 C-4



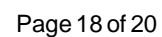
Package Diagrams (continued)

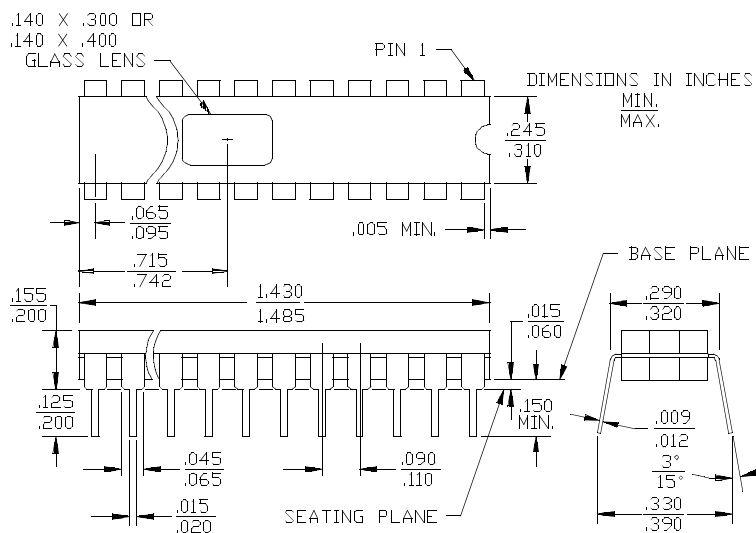
28-Pin Windowed Leaded Chip Carrier





28-Lead (300-Mil) Molded DIP P21



Package Diagrams (continued)
28-Lead (300-Mil) Windowed CerDIP W22
MIL-STD-1835 D- 15Config.A


| Document Title: CY7C331 Asynchronous Registered EPLD Document Number: 38-03011 | | | | |
|---|----------------|-------------------|------------------------|---|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 106293 | 04/20/01 | SZV | Change from Spec number: 38-00066 to 38-03011 |