TEXAS INSTRUMENTS

TVP5040

NTSC/PAL Digital Video Decoder With Macrovision™ Detection

Data Manual

May 2001

MSDS Multimedia

SLAS257D

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1 Introduction

The TVP5040 is a high-quality single-chip digital video decoder that converts base-band analog National Television System Committee (NTSC) and phase alternating line (PAL) video into digital component video. Both composite and S-video inputs are supported. The TVP5040 includes two 10-bit A/D converters with 2x sampling. Sampling is square-pixel or ITU-R BT.601 (27 MHz) and is line-locked for correct pixel alignment. The output formats can be 8-bit, 10-bit, 16-bit, or 20-bit 4:2:2, and 8-bit or 10-bit ITU-R BT.656 with embedded synchronization. The TVP5040 utilizes Texas Instruments patented technology for locking to weak, noisy, or unstable signals, and a chroma frequency control output is generated for synchronizing downstream video encoders.

Complementary three-line adaptive (2-H delay) comb filtering is available for both the luma and chroma data paths to reduce both cross-luma and cross-chroma artifacts; a chroma trap filter is also available. Video characteristics including hue, contrast, and saturation may be programmed using one of five supported host port interfaces; I^2C, three parallel host interface (PHI) modes, and VIP. The TVP5040 generates synchronization, blanking, field, lock and clock signals, in addition to digital video outputs.

The TVP5040 includes methods for advanced vertical blanking interval (VBI) data retrieval. The VBI data processor slices, parses, and performs error checking on teletext data in several formats. A built-in FIFO stores up to 14 lines of teletext data, and with proper host port synchronization full-screen teletext retrieval is possible. The VBI data processor also retrieves closed-caption data. The TVP5040 can also pass through double-sampled raw composite data for host-based software VBI processing.

The main blocks of the TVP5040 include:

- Analog processors and A/D converters
- Y/C separation
- Chrominance processor
- Luminance processor
- Clock/timing processor and power-down control
- Output formatter
- Host port interface
- VBI data processor
- Macrovision™ detection

1.1 Features

- Accepts NTSC (M) and PAL (B, D, G, H, I, M, N) composite video, S-video
- Four analog video inputs for up to four composite inputs or two S-video inputs
- Two fully differential CMOS analog preprocessing channels with clamping and automatic gain control (AGC) for best S/N performance
- Dual high-speed 2x over-sampling 10-bit A/D converters
- Patented architecture for locking to weak, noisy, or unstable signals
- Single 14.31818-MHz reference crystal for all standards
- Line-locked clock and sampling at square-pixel or 27-MHz rates
- Programmable output data rates:
  - 12.2727 MHz square-pixel (NTSC)
  - 14.7500 MHz square-pixel (PAL)
  - 13.5 MHz ITU-R BT.601 (NTSC and PAL)
- Optional automatic switching between PAL and NTSC standards

- This device requires microcode to be downloaded in order to operate (see Note)
- Complementary 3-line (2-H delay) adaptive comb filters for both cross-luminance and cross-chrominance noise reduction
- Subcarrier genlock output for synchronizing color subcarrier of external encoder
- Standard programmable video output formats:
  - 16-bit 4:2:2 YCbCr
  - 20-bit 4:2:2 YCbCr
  - 8-bit 4:2:2 YCbCr
  - 10-bit 4:2:2 YCbCr
  - ITU-R BT.656 8-bit 4:2:2 with embedded syncs
  - ITU-R BT.656 10-bit 4:2:2 with embedded syncs
- Advanced programmable video output formats:
  - 2x oversampled raw VBI data during active video
  - Sliced VBI data as ancillary data in video stream
- Teletext (NABTS, WST) and closed-caption decode with FIFO
- Macrovision copy protection detection
- Supports ITU-R BT.601 standard
- Programmable host port options including I^2C, three parallel host interface (PHI) modes, and VIP 2.0
- Brightness, contrast, saturation, and hue control through host port
- 5-V tolerant digital I/O ports
- 80-pin TQFP package

1.2 Applications

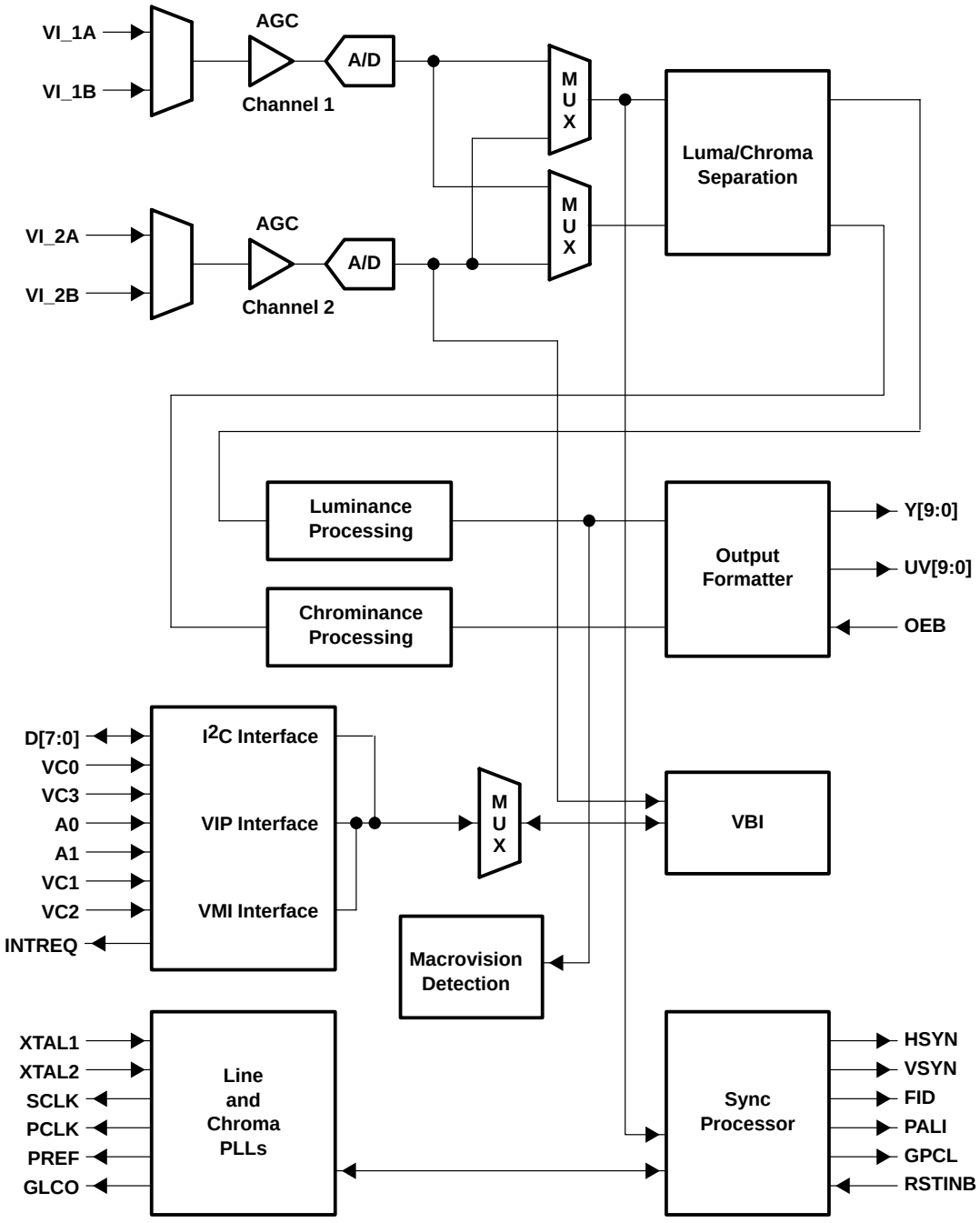
- Digital image processing
- Video conferencing
- Multimedia
- Digital video
- Desktop video
- Video capture
- Video editing
- Intercast and teletext applications
- Security applications

1.3 Related Products

- TVP5031 NTSC/PAL Digital Video Decoder, Literature Number SLAS267B
- TVP6000 NTSC/PAL Digital Video Encoder, Literature Number SLAS184

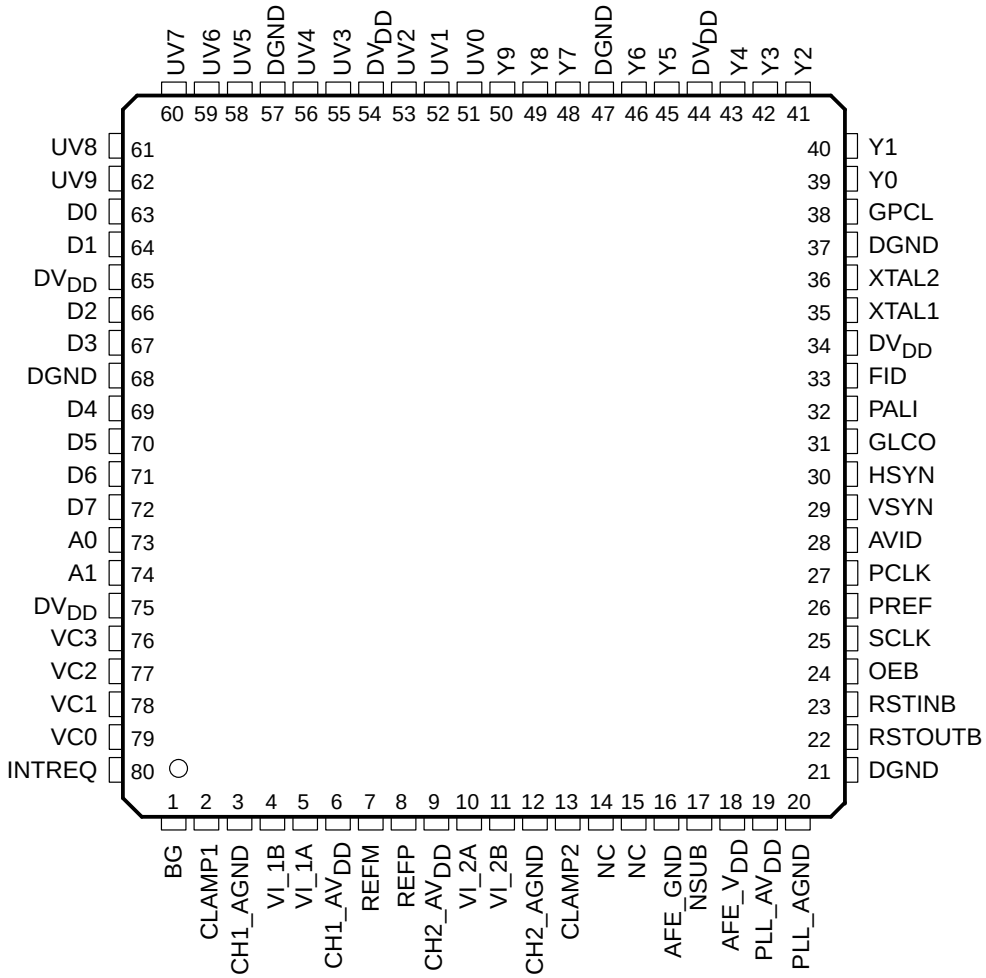
NOTE:
To obtain the device software from the TI Web site, click on the development tools link from the TVP5040 product page.

1.4 Functional Block Diagram



1.5 Terminal Assignments

TQFP PACKAGE
(TOP VIEW)



1.6 Ordering Information

DEVICE:	TVP5040CPFP
PFP:	Plastic flat-pack with PowerPAD™

NOTE: PowerPAD package requires special board layout considerations. Please see Texas Instruments Literature Number SLMA004 for more information.

PowerPAD is a trademark of Texas Instruments.

1.7 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
Analog Video			
VI–1A VI–1B VI–2A VI–2B	5 4 10 11	I	Analog video inputs. Up to four composite inputs or two S-video inputs or a combination of the two. The inputs must be ac-coupled. The recommended coupling is 0.1 μF.
Clock Signals			
PCLK	27	O	Pixel clock output. The frequency is 12.2727 MHz for square-pixel NTSC, 14.75 MHz for square-pixel PAL, and 13.5 MHz for ITU-R.BT.601 sampling modes.
PREF	26	I/O	Clock phase reference signal. This signal qualifies clock edges when SCLK is used to clock data that is changing at the pixel clock rate.
SCLK	25	O	System clock output with twice the frequency of the pixel clock (PCLK).
XTAL1 XTAL2	35 36	I	External clock reference. The user may connect XTAL1 to a TTL-compatible oscillator or to one terminal of a crystal oscillator. The user may connect XTAL2 to the other terminal of the crystal oscillator or not connect XTAL2 at all. One single 14.31818-MHz crystal or oscillator is needed for square pixel sampling and ITU-R BT.601 sampling.
Digital Video			
UV[9:0]	62, 61, 60, 59, 58, 56, 55, 53, 52, 51	I/O	10-bit digital chrominance outputs. These terminals may also be configured to output the data from the channel 2 A/D converter. A vendor modifiable subsystem ID may be initialized by configuring the UV[9:0] terminals with pullup/pulldown resistors. Terminals UV[7:0] are used to set the lower byte of the subsystem ID, and terminals UV[9:8] are used to set the bit 9 and bit 8. During reset, UV[9:0] terminals are used to set the VIP device configuration registers.
Y[9:0]	50, 49, 48, 46, 45, 43, 42, 41, 40, 39	I/O	10-bit digital luminance outputs, or 10-bit multiplexed luminance and chrominance outputs. These terminals may also be configured to output the data from the channel 1 A/D converter. A vendor modifiable subsystem ID may be initialized by configuring the Y[9:0] terminals with pullup/pulldown resistors. Terminals Y[7:0] are used to set the upper byte of the subsystem ID, and terminals Y[9:8] are used to set the bit 11 and bit 10. During reset, Y[9:0] terminals are used to set the VIP device configuration registers.
HOST PORT-Bus			
A[1:0]	74, 73	I	PHI mode: PHI address port. VIP mode: During reset A[1:0] terminals are input and are used to set the VIP device configuration registers. A[1:0] are used to set bits 13 and 12 of the subsystem device ID. Pull up on each terminal during reset will set a 1 to the corresponding bit . Leaving the terminal undriven or pulldown on the terminal during the reset will set a 0. The internal weak pulldown remains on after reset.
D[7:0]	72, 71, 70, 69, 67, 66, 64, 63	I/O	PHI mode: PHI data port-bit [7:0] VIP mode: During reset, D[7:0] terminals are input and are used to set the VIP device configuration registers. D[7:0] are used to set the lower byte of the subsystem device ID. Pull up on each terminal during reset will set a 1 to the corresponding bit . Leaving the terminal undriven or pulldown on the terminal during the reset will set a 0. The internal weak pulldown remains on after reset.
INTREQ	80	I/O	PHI mode: Interrupt request (INTREQ) Pullup is required if configured as open drain. I^2C mode: Interrupt request (INTREQ) Pullup is required if configured as open drain. VIP mode: Interrupt request (VIRQ) No internal weak pulldown. 10 KΩ pullup resistor is required.
VC0	79	I/O	PHI mode: PHI port data acknowledgement or ready signal **(**DTACK**)** I^2C mode: Serial clock (SCL) Pullup is required. VIP mode**:** Hardware address bit 0 (HAD[0])
VC1	78	I/O	PHI mode: PHI port read-write or write (RW/WR) I^2C mode: Serial data (SDA) Pullup is required. VIP mode**:** Hardware address bit 1 HAD[1] 10-KΩ pullup resistor is required.
VC2	77	I/O	PHI mode: PHI port data strobe or read signal (DS/RD) VIP mode**:** Hardware control (HCTL) 10-KΩ pullup resistor is required.
VC3	76	I	PHI mode: PHI port chip select (VC) I^2C mode: Slave address select (I^2CA) VIP mode**:** VIPCLK

1.7 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
Miscellaneous Signals			
RSTOUTB	22	O	Reset output, active low
RSTINB	23	I	Reset input, active low
OEB	24	I/O	Output enable for Y and UV terminals. Output enable is also controllable via the host port. When this terminal is a logic 1, it forces Y and UV output terminals to high impedance states (active low).
GLCO	31	I/O	This serial output carries color PLL information. A slave device can decode the information to allow chroma frequency control to the TVP5040. Data is transmitted at the SCLK rate. Additionally, this terminal, in conjunction with PALI and FID, is used to determine the host port mode configuration during initial power up.
GPCL	38	I/O	General-purpose control logic. This terminal has three functions: 1) General-purpose output. In this mode the state of GPCL is directly programmed via the host port. 2) Vertical blank output. In this mode the GPCL terminal is used to indicate the vertical blanking interval of the output video. The beginning and end times of this signal are programmable via the host port control. 3) Sync lock control input. In this mode when GPCL is high, the output clock frequencies and the sync timing are forced to nominal values.
CLAMP1, CLAMP2	2, 13	O	Clamp voltage outputs. Connect a 0.1-μF decoupling capacitor from each terminal to analog ground
NC	14, 15		No connection
BG	1	O	Connect a 1-μF capacitor from this terminal to CH1_AGND – CH2_AGND
Power Supplies			
AFE_V_{DD}	18		Analog supply. Connect to 3.3-V analog supply
AFE_GND	16		Analog ground
CH1_AGND CH2_AGND	3 12		Analog grounds
CH1_AV_{DD} CH2_AV_{DD}	6 9		Analog supply. Connect to 3.3-V analog supply.
DGND	21, 37, 47, 57, 68		Digital grounds
PLL_AGND	20		PLL ground. Connect to analog ground.
PLL_AV_{DD}	19		Pll supply. Connect to 3.3-V analog supply.
DV_{DD}	34, 44, 54, 65, 75		Digital supply. Connect to 3.3 V.
NSUB	17		Susbstrate ground. Connect to analog ground.
REFP	8	O	A/D reference supply. Connect a 4.7-μF capacitor from each terminal to analog ground. Connect a 1-μF capacitor across REFM and REFP terminals.
REFM	7	O	
Sync Signals			
AVID	28	I/O	Active video indicator. This signal is high during the horizontal active time of the video output on the Y and UV terminals. AVID continues to toggle during vertical blanking intervals. This terminal may be placed in a high-impedance state. During reset, AVID is an input, used to program the behavior of Y[9:0], UV[9:0], HSYN, VSYN, AVID, and FID immediately after the completion of reset. If AVID is pulled up during reset, Y[9:0], UV[9:0], HSYN, VSYN, AVID, PALI, and FID actively drive after reset. If AVID is pulled down during reset, Y[9:0], UV[9:0], HSYN, VSYN, AVID, PALI, and FID remain in high-impedance state after reset.
FID	33	I/O	Odd/even field indicator or vertical lock indicator. For odd/even indicator, a logic 1 indicates the odd field. For vertical lock indicator, a logic 1 indicates the internal vertical PLL is in a locked state. Additionally, this terminal in conjunction with GLCO and PALI is used to determine the host port configuration during initial power up and reset.

1.7 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
Sync Signals (Continued)			
HSYN	30	O	Horizontal sync signal with respect to the digital video data output. The rising edge time is programmable via the host port.
PALI	32	I/O	PAL line indicator or horizontal lock indicator. For PAL line indicator, a logic 1 indicates a noninverted line, and a logic 0 indicates an inverted line. For horizontal lock indicator, a logic 1 indicates the internal horizontal PLL is in a locked state. This terminal is an input terminal during reset and is used in conjunction with GLCO and FID to select the mode of the host interface. During reset, this terminal can be pulled up to set a 1, or pulled down to set a 0.
VSYN	29	O	Vertical sync signal with respect to the digital video data output.

1.8 Strapping Terminals Description

All of the following terminals have reset strapping options. The states of these terminals are sampled during reset to configure TVP5040 for various modes of operation. These terminals are temporarily turned into inputs with weak internal pulldown (approximately 40-KΩ resistor) during reset and return to their normal operation after reset. Each of the following terminals can be pulled up with a 10-KΩ resistor to set a 1 to the corresponding bit or be left undriven during reset, relying on the internal pulldown resistor to pull the terminal low to set a 0 to the corresponding bit.

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
UV[7:0]	60, 59, 58, 56 55, 53, 52, 51	Lower byte of VIP subsystem vendor ID (VIP register 004)
Y[7:0]	48, 46, 45, 43, 42, 41, 40, 39	Upper byte of VIP subsystem vendor ID (VIP register 005)
D[7:0]	72, 71, 70, 69, 67, 66, 64, 63,	Lower byte of VIP subsystem device ID (VIP register 006)
UV[9:8]	62, 61	Bits 1 and 0 of the upper byte of VIP subsystem device ID (VIP register 007)
Y[9:8]	50, 49	Bits 3 and 2 of the upper byte of VIP subsystem device ID (VIP register 007)
HSYN	30	Bit 4 of the upper byte of VIP subsystem device ID (VIP register 007)
VSYN	29	Bit 5 of the upper byte of VIP subsystem device ID (VIP register 007)
A[1:0]	74, 73	Bits 7 and 6 of the upper byte of VIP subsystem device ID (VIP register 007)
AVID	28	Y, U/V output enable (bit 4) and HSYN, VSYN, AVID, FID, and PALI output enable (bit 3) of miscellaneous control (register 03)
PREF	26	Clock enable bit (bit 0) of miscellaneous control (register 03)
FID	33	Host interface mode (see Table 2-2)
PALI	32	Host interface mode (see Table 2-2)
GLCO	31	Host interface mode (see Table 2-2)

2 Functional Description

2.1 Analog Video Processing and A/D Converters

Figure 2–1 shows a functional diagram of the analog video preprocessors and A/D converters. This block provides the analog interface to all the video inputs. It accepts up to four inputs and performs source selection, video clamping, video amplification, analog-to-digital conversion, and fine gain and offset adjustments to center the digitized video signal.

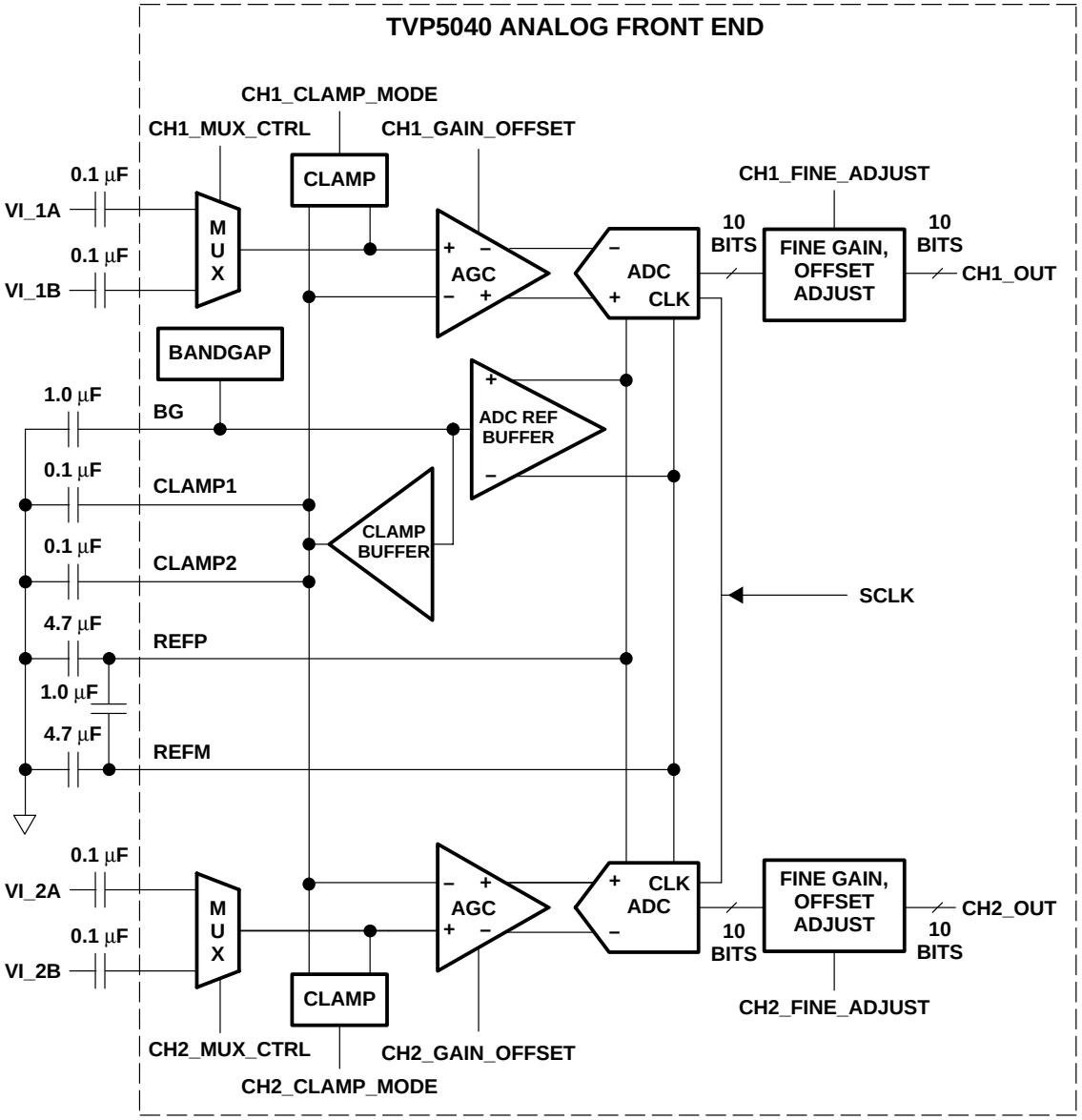


Figure 2–1. Analog Video Processors and A/D Converters

2.1.1 Video Input Selection

The TVP5040 has two analog channels that accept four video inputs ac-coupled through 0.1-μF capacitors. The internal video multiplexers can be configured via the host port. The four analog video inputs may be connected as follows:

- Four selectable individual composite video inputs
- One S-video input and two composite video inputs
- Two S-video inputs

2.1.2 Analog Input Clamping and Automatic Gain Control Circuits

An internal clamping circuit restores the ac-coupled video signal to a fixed dc level. The clamping circuit provides line-by-line restoration of the video sync level to a fixed dc reference voltage. Two modes of clamping are provided: coarse and fine. In coarse mode, the most negative portion of the input signal (typically the sync tip) is clamped to a fixed dc level. Fine clamp mode may be enabled to prevent spurious level shifting caused by noise more negative than the sync tip on the input signal. If fine clamp mode is selected, clamping is only enabled during the sync period. S-video requires fine clamp mode on the chroma channel for proper operation. External capacitors of 0.1-μF on terminal CLAMP1 and CLAMP2 are required to store and filter the clamp voltage.

The input video signal amplitude may vary significantly from the nominal level of 1 V_{pp}. An automatic gain control circuit (AGC) adjusts the signal amplitude to utilize the maximum range of the A/D converter without clipping. The AGC adjusts gain to achieve desired sync amplitude. Some nonstandard video signals contain peak white levels that saturate the A/D converter. In these cases, AGC automatically cuts back gain to avoid clipping.

In the digital data path, scaling is applied to the A/D output data to reach CCIR601 Y, Cr, and Cb levels. This scaling introduces distortion if digitized sync tip and back porch levels are not precise. The fine gain and offset adjustment block precisely controls the sync tip and back porch levels to achieve best linearity performance.

2.1.3 A/D Converters

The TVP5040 contains two 10-bit 2x oversampling A/D converters that digitize the analog video inputs. As the inputs are digitized at greater than two times the Nyquist sampling rate, only simple external antialiasing low pass filters are needed to prevent out-of-band frequencies. The A/D converter reference voltages on terminals REFP and REFM require an external capacitor network for filtering, as shown in Figure 2–1.

2.2 Digital Processing

Figure 2–2 is a block diagram of the TVP5040 digital video decoder processing. This block receives digitized composite or S-video signals from the A/D converters. It performs Y/C separation, Y, and U/V signal enhancements. It also generates horizontal and vertical syncs. The Y and U/V digital outputs may be programmed into various formats: 20-bit, 16-bit, 10-bit, or 8-bit 4:2:2, and 10-bit or 8-bit ITU-R BT.656 parallel interface standard. This block also retrieves VBI data and stores it in a FIFO. The data from the FIFO can be read either through the host port or output as ancillary data on the video port. This block also detects pseudosync pulses, AGC pulses and color striping in copy protected material in accordance with Macrovision specification.

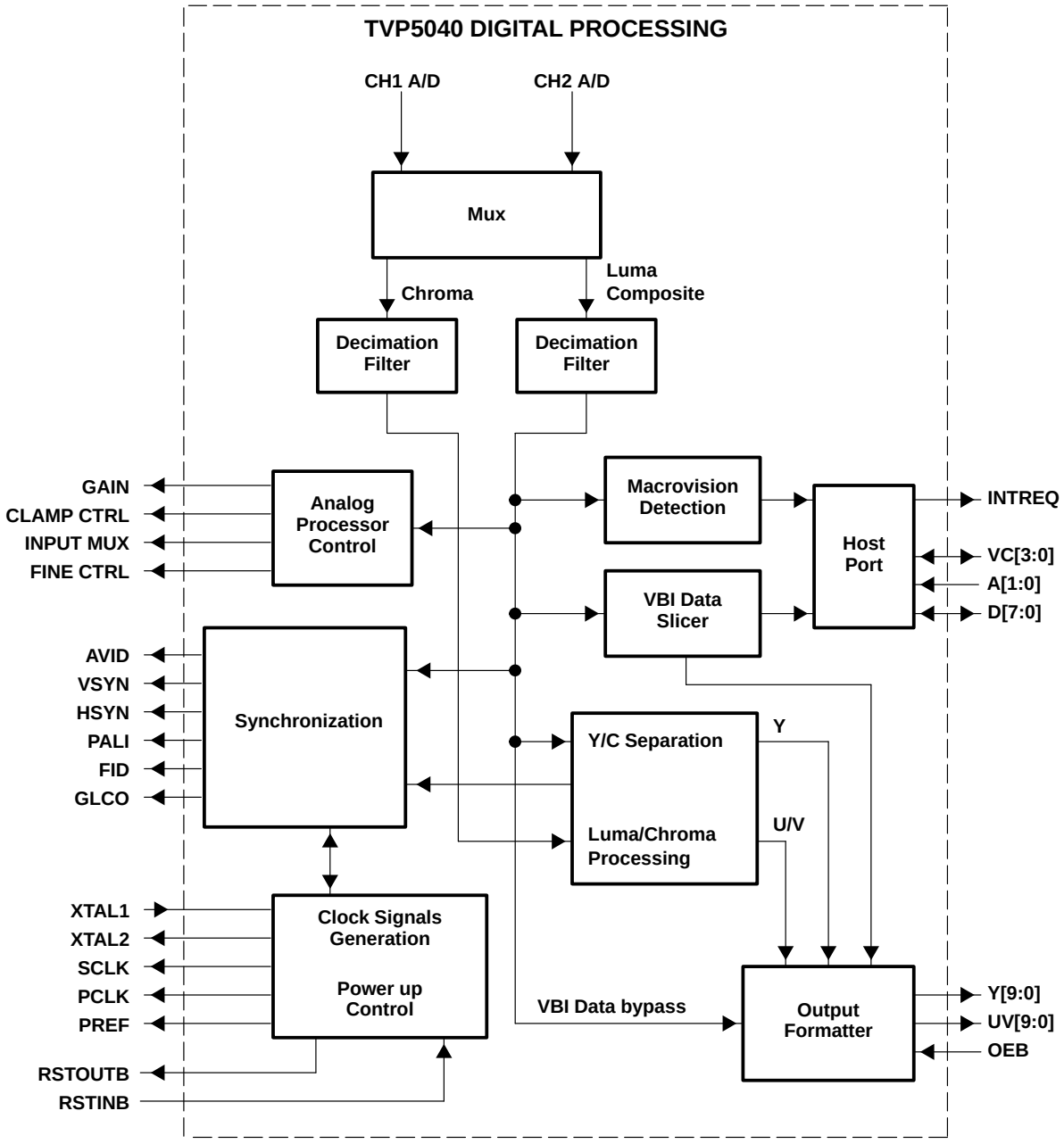


Figure 2–2. Digital Video Signal Processing Block Diagram

2.2.1 Digital Input Selection

The digital processing block takes digitized composite or S-video from the two internal A/D converters running at 2x PCLK rate. The data from the A/D converters are appropriately multiplexed as shown in Figure 2–3 for downstream separation and processing of luma and chroma.

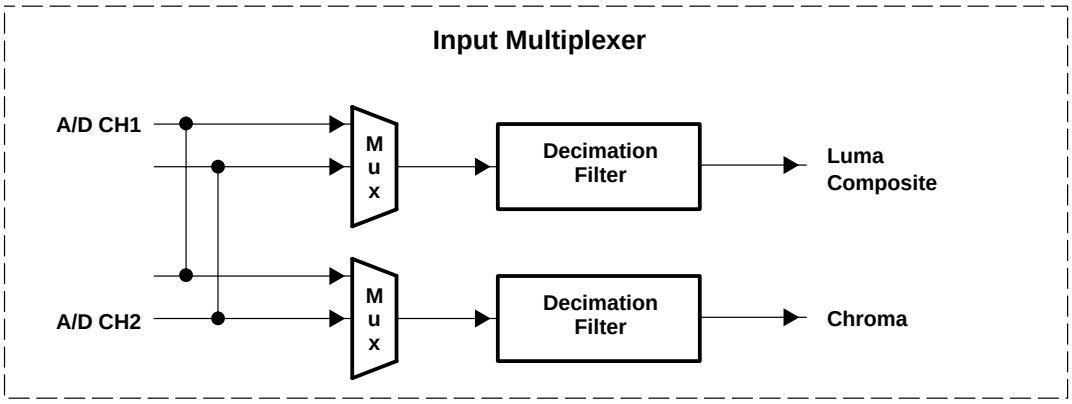


Figure 2–3. Digital Input Multiplexer

2.2.2 Decimation Filter

Digitized composite or S-video at 2x PCLK rate first passes through two decimation filters that reduce the data rate from 2x to 1x PCLK. The decimation filter is a half-band filter whose frequency response is shown in Figure 2–4. For applications that can not tolerate high frequency roll off, the decimation filters can be bypassed via host port. The 2x oversampling and decimation filtering can effectively increase the overall signal-to-noise ratio by 3 dB. This advantage is lost if the decimation filter is bypassed.

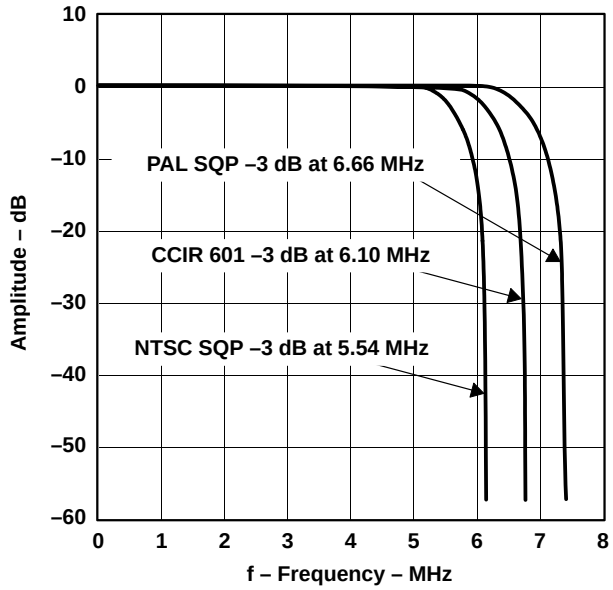


Figure 2–4. Decimation Filter Frequency Response

2.2.3 Y/C Separation

Figure 2–5 illustrates the luminance/chrominance (Y/C) separation process in the TVP5040. 10-bit composite video is multiplied by subcarrier signals in the quadrature demodulator to generate color difference signals U and V. The U and V are then run into low-pass filter to achieve the desired bandwidth. An adaptive 3-line comb filter separates UV from Y based on the unique property of color phase shifts from line to line. The chroma is remodulated through a quadrature modulator and subtracted from line-delayed composite video to generate luma. This form of Y/C separation is completely complementary, thus there is no loss of information. However in some applications, it is desirable to limit the U/V bandwidth to avoid crosstalk. In that case, notch filters can be turned on. To accommodate some viewing preferences, a peaking filter is also available in the luma path. The Y/C separation is bypassed for S-video input. Contrast, brightness, hue, and saturation are programmable via the host port.

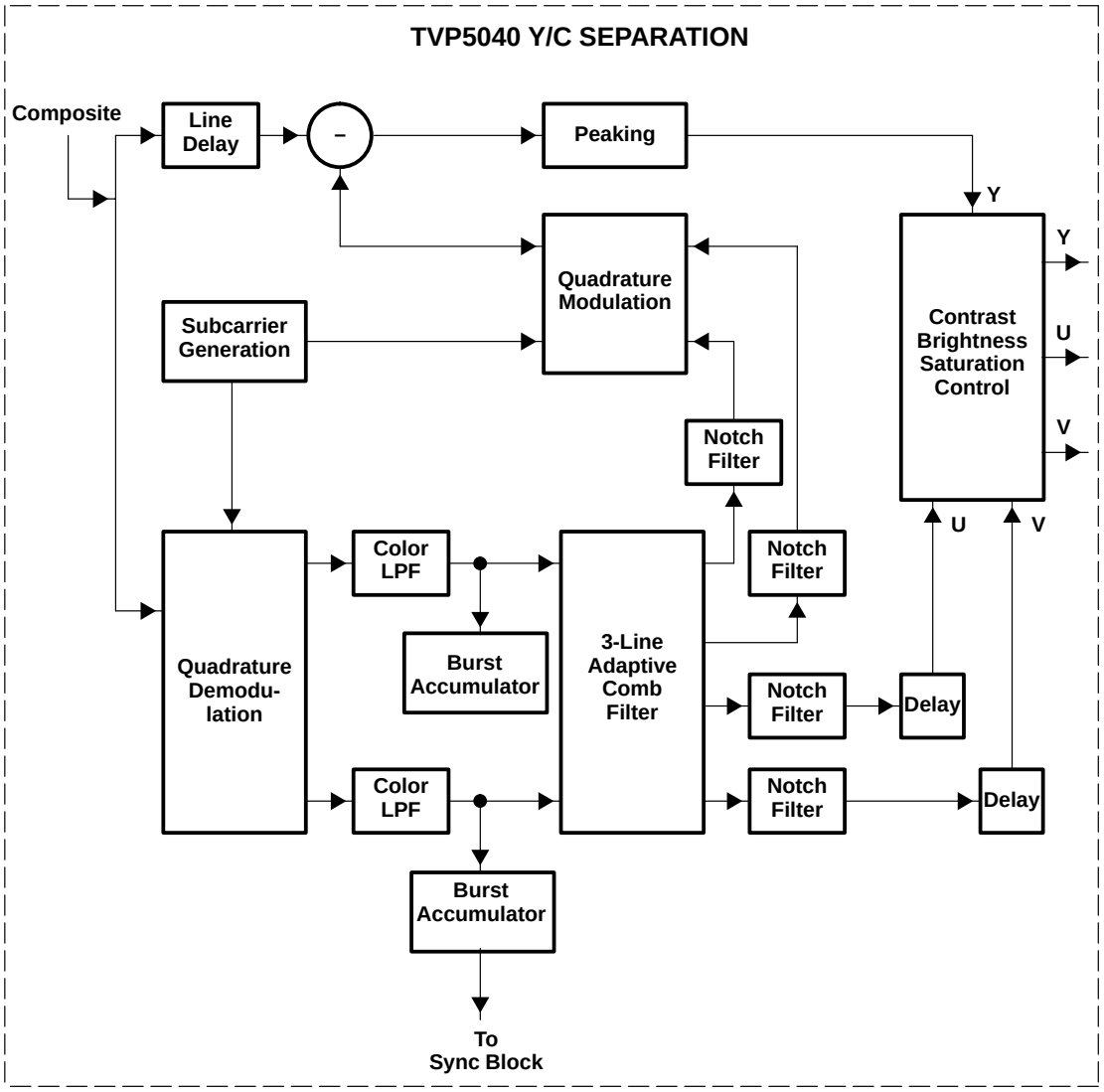


Figure 2–5. Y/C Separation Block Diagram

2.2.3.1 Color Low-Pass Filter

Color low-pass filter frequency responses are shown in Figures 2–6 to 2–9. High filter bandwidth preserves sharp color transitions and produces crisp color boundaries. However, for nonstandard video sources that have asymmetrical U and V side bands, it is desirable to limit the filter bandwidth to avoid UV crosstalk. Color low-pass filter bandwidth is programmable by enabling one of the three notch filters.

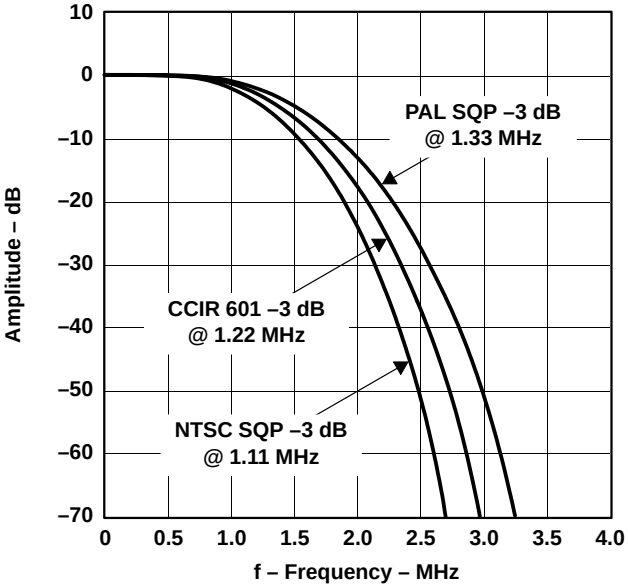


Figure 2–6. Color Low-Pass Filter Frequency Response

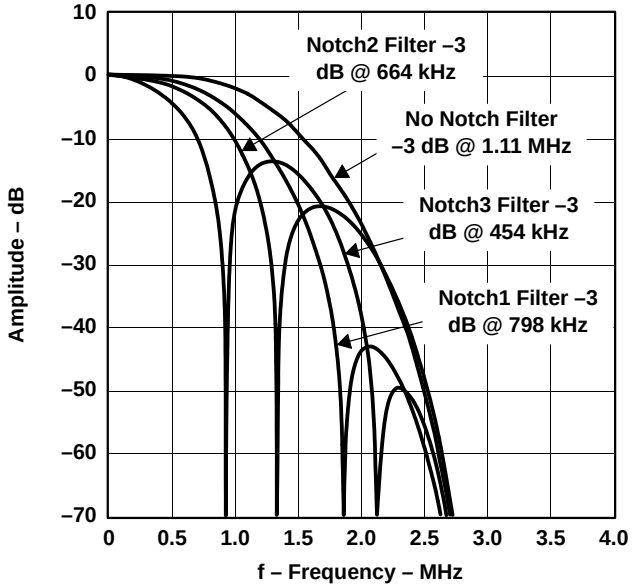


Figure 2–7. Color Low-Pass Filter With Notch Filter Frequency Response (NTSC And PAL-M Square Pixel Sampling)

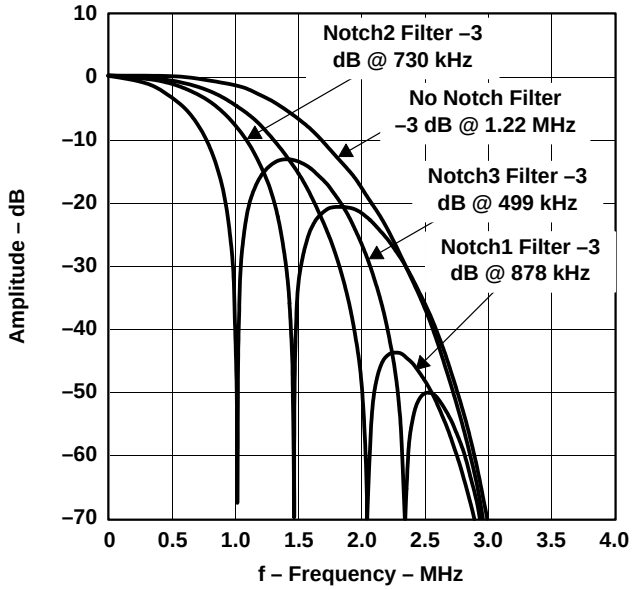


Figure 2–8. Color Low-Pass Filter With Notch Filter Characteristics (13.5 MHz Sampling)

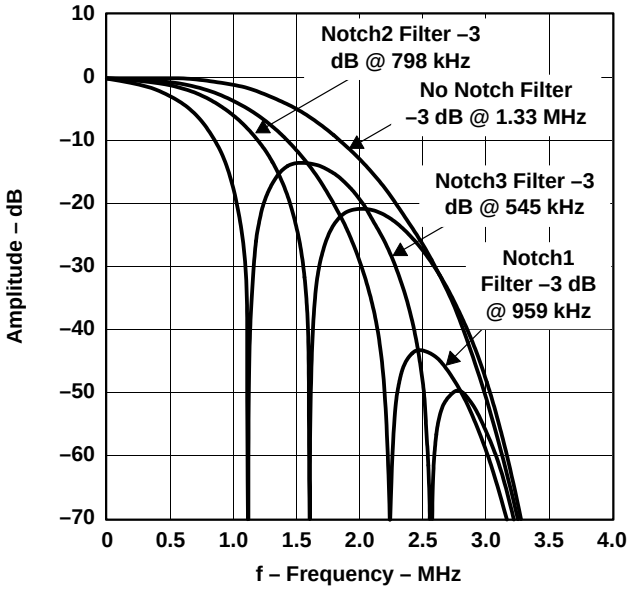


Figure 2–9. Color Low-Pass Filter With Notch Filter Frequency Response (PAL Square Pixel Sampling)

2.2.3.2 Adaptive Comb Filter

Y/C separation may be done using adaptive 3-line (2-H delay), fixed 3-line, fixed 2-line comb filters, or a chroma trap filter as shown in Figure 2–10. Adaptive comb filtering is available for both luminance and chrominance. The adaptive comb filter algorithm computes the vertical and horizontal contours of color based on a block of 3×3 pixels. If there is a sharp color transition, comb filtering is applied to the two lines that have fewer color changes. If there is no color transition, 3-line comb filtering is used with a choice of filter coefficients [1/4, 1/2, 1/4] or [1/2, 0, 1/2] programmable via the host port. Characteristics of 2-line and 3-line comb filters are shown in Figure 2–11. The filter frequency plots show that both 2-line and 3-line (with filter coefficients [1/4,1/2,1/4]) comb filters have zeros at 1/2 of the horizontal line frequency to separate the interleaved Y/C spectrum in NTSC. The 3-line comb filter has less cross-luma and cross-chroma noise due to slightly sharper filter cut off. The 3-line comb filter with filter coefficients[1/2, 0, 1/2] has two zeros at 1/4 and 3/4 of the horizontal line frequency. This should be used for PAL only because of its 90 degrees U/V phase shifting from line to line. The comb filter can be selectively bypassed in the luma or chroma path. If the comb filter is bypassed in the luma path, then chroma trap filters are used which are shown in Figures 2–12 to 2–14. TI's patented adaptive comb filter algorithm reduces artifacts such as hanging dots at color boundary and detects and properly handles false colors in high frequency luminance images such as a multiburst pattern or circle pattern. Adaptive comb filtering is the recommended mode of operation.

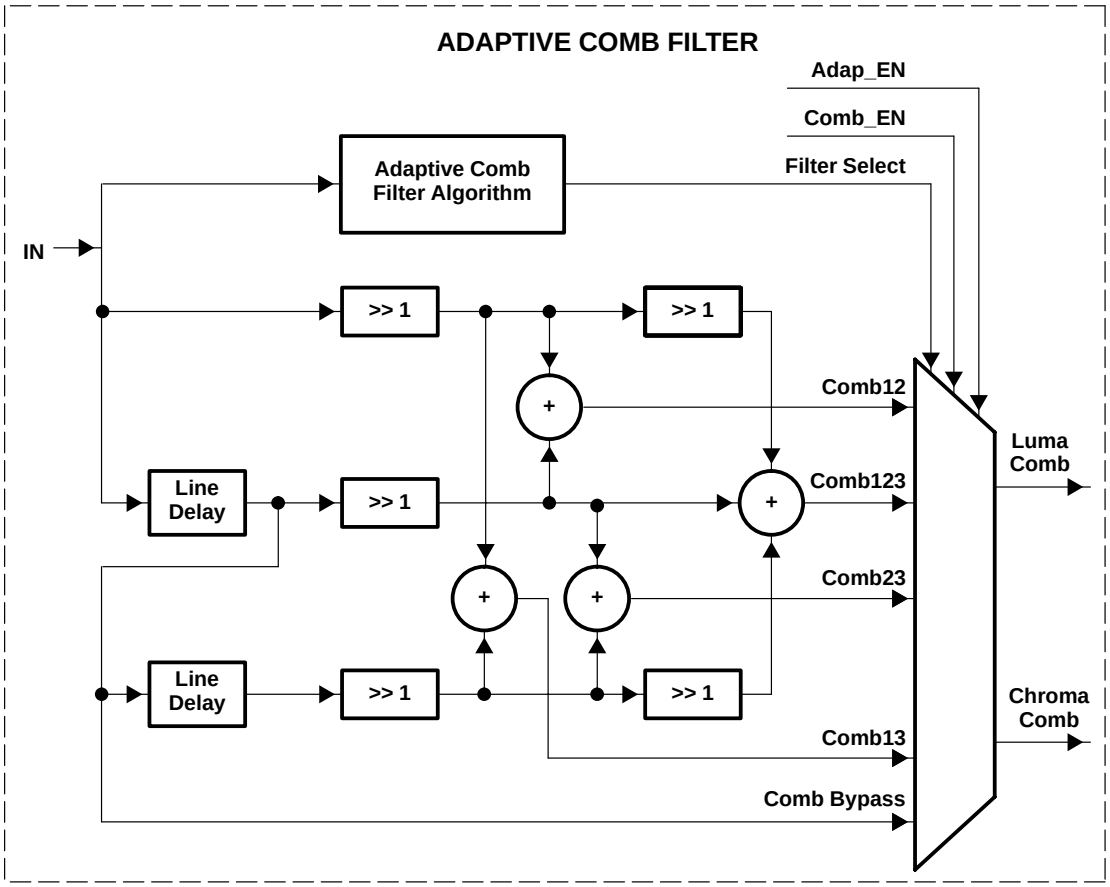


Figure 2–10. 3-Line Adaptive Comb Filtering

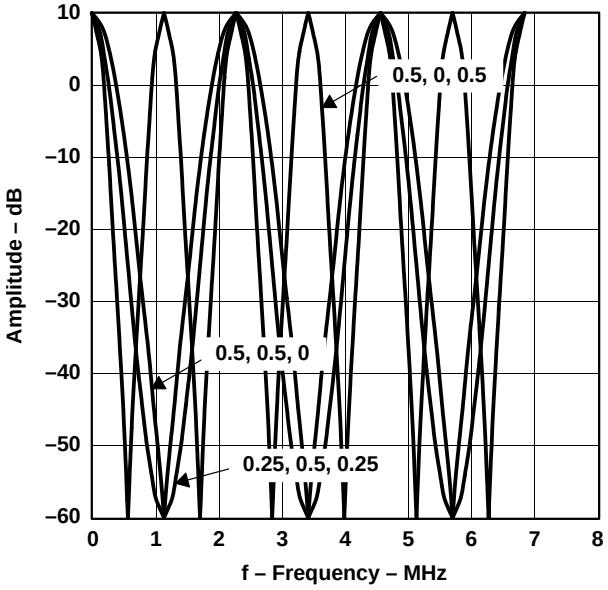


Figure 2–11. Comb Filters Frequency Response

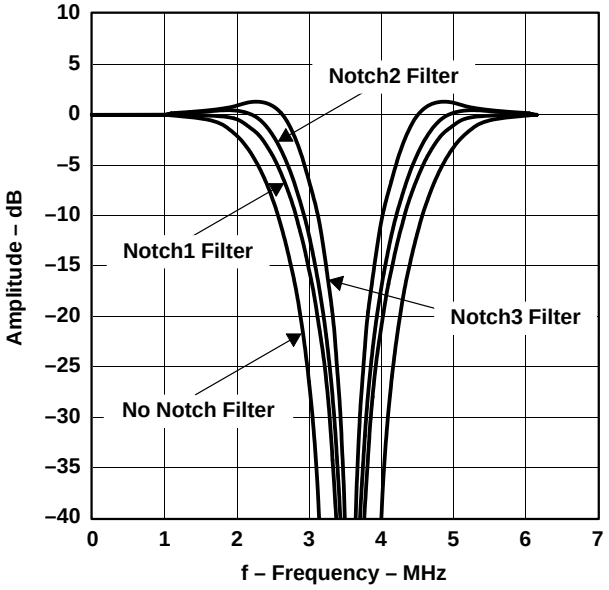


Figure 2–12. Chroma Trap Filter Frequency Response (NTSC Square Pixel Sampling)

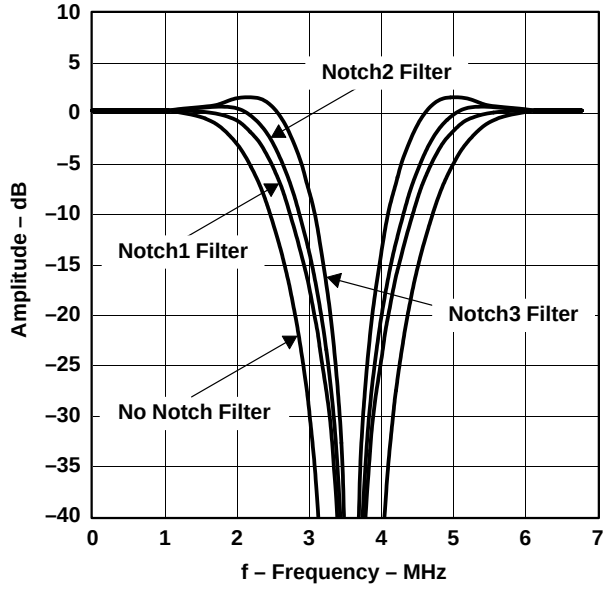


Figure 2–13. Chroma Trap Filter Frequency Response (13.5 MHz Sampling)

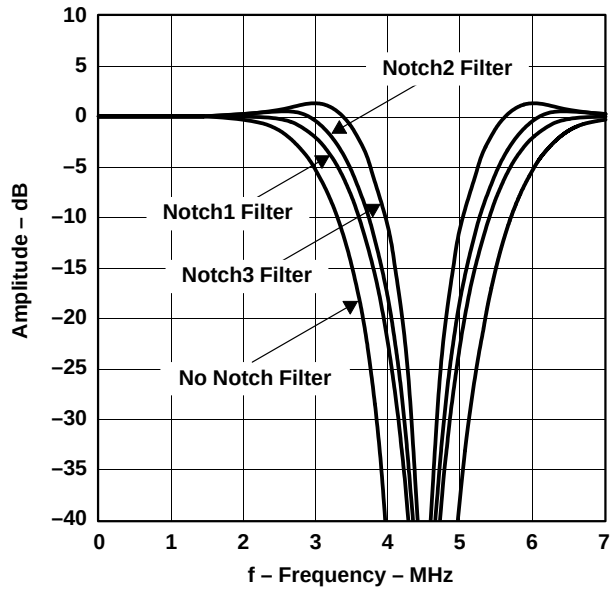


Figure 2–14. Chroma Trap Filter Frequency Response (PAL Square Pixel Sampling)

2.2.4 Luminance Processing

The digitized composite video signal passes through either a luminance comb filter or a chroma trap filter, either of which removes chrominance information from the composite signal to generate a luminance signal. The luminance signal is then fed to the input of a peaking circuit. Figure 2–15 illustrates the basic functions of the luminance data path. High frequency components of the luminance signal are enhanced by a peaking filter (edge-enhancer). Figure 2–16, Figure 2–17, and Figure 2–18 show the characteristics of the peaking filter at four different gain settings programmable via the host port.

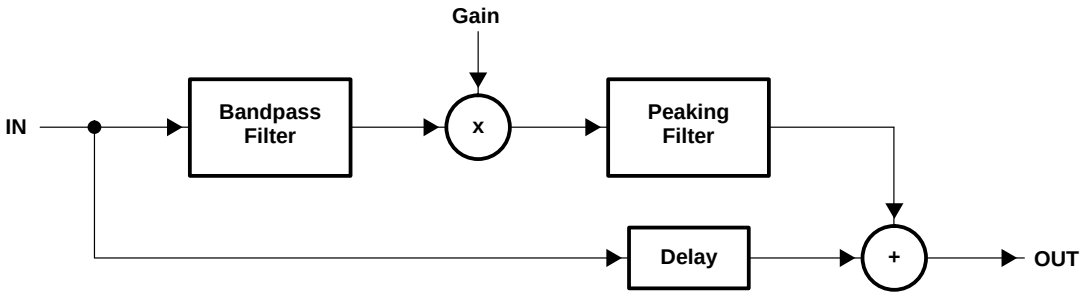


Figure 2–15. Luminance Edge-Enhancer Peaking Block Diagram

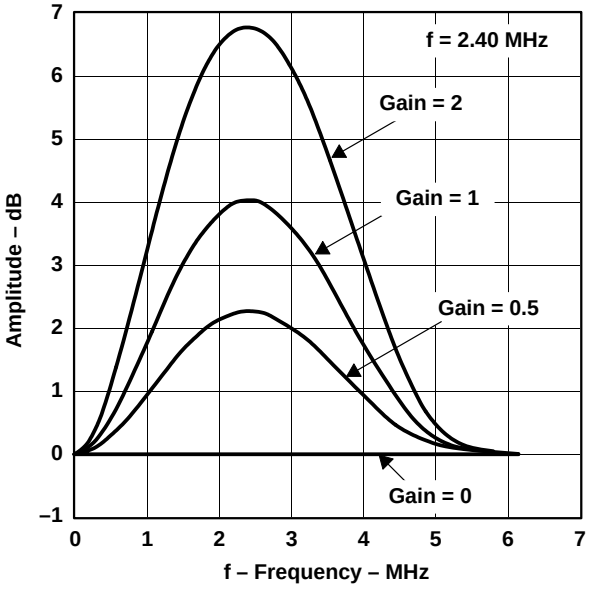


Figure 2–16. Peaking Filter Response, NTSC and PAL-M Square Pixel Sampling

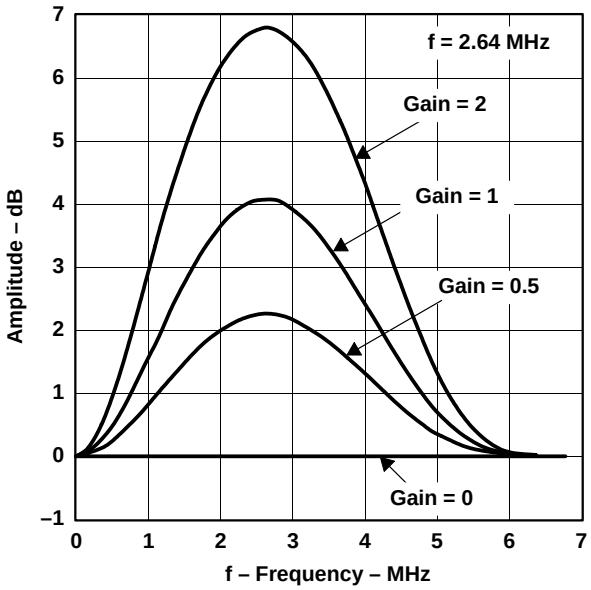


Figure 2–17. Peaking Filter Response, 13.5 MHz Sampling Rate

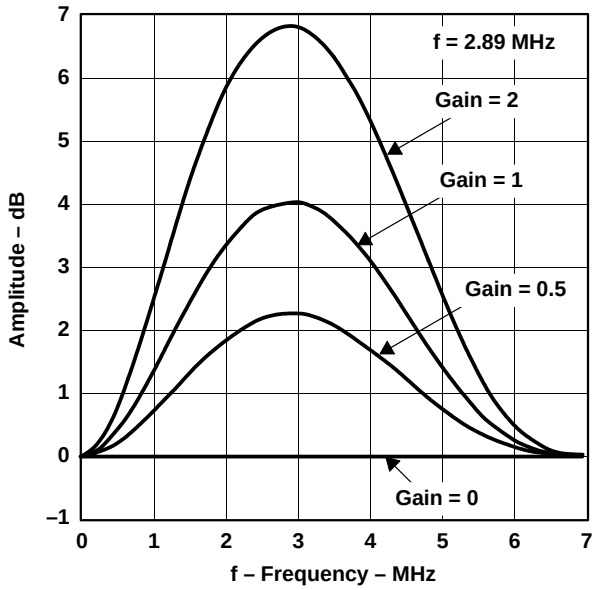


Figure 2–18. Peaking Filter Response, PAL Square Pixel

2.2.5 Chrominance Processing

A quadrature demodulator extracts U and V components from the composite signal. The U/V signals then pass through the gain control stage for chroma saturation adjustment. A comb filter is applied to both U and V to eliminate cross-chrominance noise. Hue control is achieved with phase shift of the digitally controlled oscillator. An automatic color killer (ACK) circuit is also included in this block. The ACK will suppress the chroma processing when the color burst of the video signal is weak or not present.

2.2.6 Clock Circuits

An internal line-locked PLL generates the system and pixel clocks. Figure 2–19 shows a simplified clock circuit diagram. The digital control oscillator (DCO) generates the reference signal for the horizontal PLL. A 14.318-MHz clock is required to drive the DCO. This may be input to the TVP5040 at TTL level on the XTAL1 terminal, or a crystal of 14.318 MHz fundamental resonant frequency may be connected across terminals XTAL1 and XTAL2. Figure 2–20 shows the reference clock configurations. For the example crystal circuit shown in Figure 2–20 (a parallel-resonant crystal with 14.31818 MHz fundamental frequency), the external capacitors must have the following relationship:

$$C_{L1} = C_{L2} = 2C_L - C_{(stray)}$$

where $C_{(stray)}$ is the terminal capacitance with respect to ground. Note that with the crystal oscillator, an external 4.53-KΩ resistor is required across XTAL1 and XTAL2 terminals.

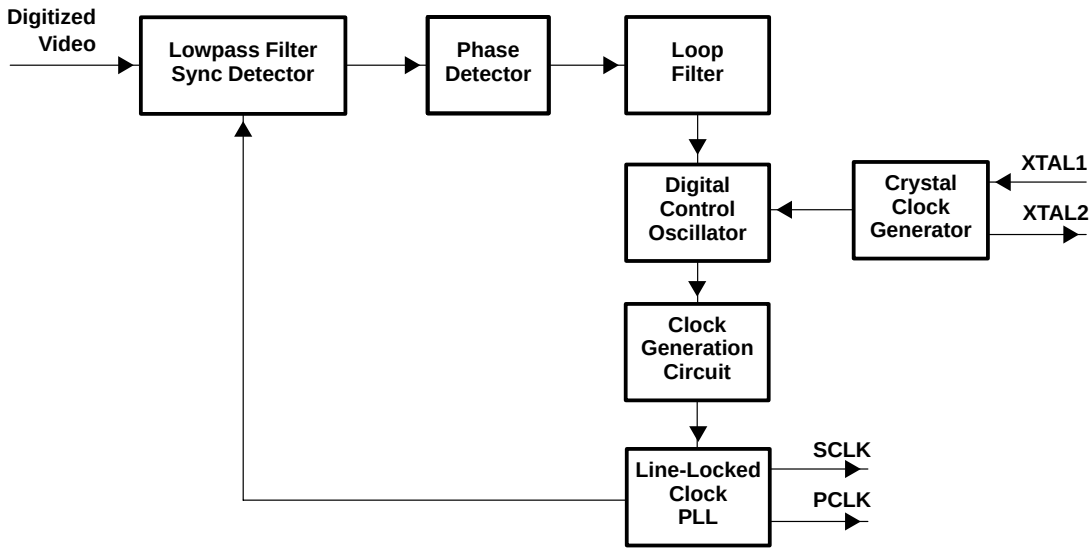


Figure 2–19. Clock Circuit Diagram

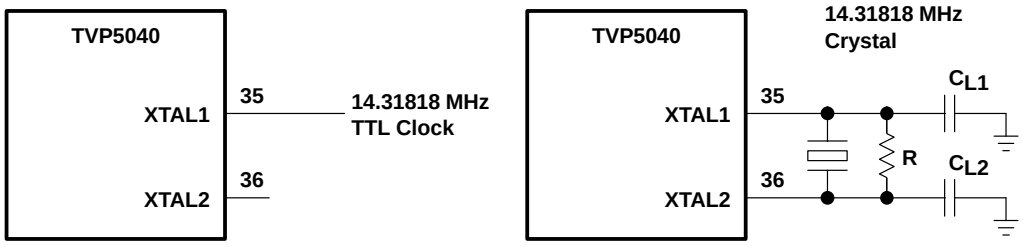


Figure 2–20. Example Reference Clock Configurations

The TVP5040 generates three signals PCLK, SCLK, and PREF used for clocking data. PCLK, the pixel clock, can be used for clocking data in the 20-bit and 16-bit 4:2:2 output formats. SCLK is twice the PCLK frequency and may be used for clocking data in the 10-bit and 8-bit 4:2:2 as well as in ITU-R BT.656 formats. PREF is used as a clock qualifier with SCLK to clock data in the 20-bit and 16-bit 4:2:2 formats.

2.3 Genlock Control

The frequency control word of the internal color subcarrier digital control oscillator (DCO) and the sub-carrier phase reset bit are transmitted via the GLCO terminal. The frequency control word is a 23-bit binary number. The frequency of the DCO can be calculated from the following equation:

$$F_{dco} = \frac{F_{ctrl}}{2^{23}} \times F_{sclk}$$

where F_{dco} is the frequency of the DCO, F_{ctrl} is the 23-bit DCO frequency control and F_{sclk} is the frequency of the SCLK.

The last bit (bit 0) of the DCO frequency control is always 0.

A write of 1 to bit 4 of the chrominance control register at the host port sub-address 1Ah causes the sub-carrier DTO phase reset bit to be sent on the next scan line on GLCO. The active low reset bit occurs 7 SCLKs after the transmission of the last bit of DCO frequency control. Upon the transmission of the reset bit, the phase of the TVP5040 internal subcarrier DCO is reset to zero.

A genlocking slave device can be connected to the GLCO terminal and use the information on GLCO to synchronize its internal color phase DCO to achieve clean line and color lock.

Figure 2–21 shows the timing of GLCO.

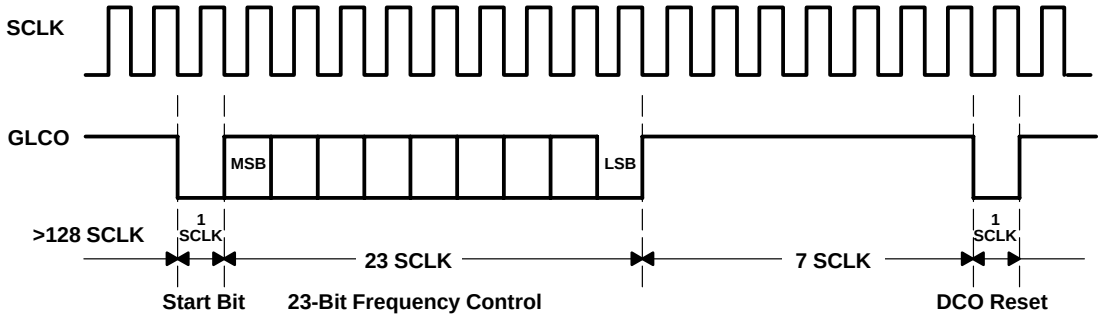


Figure 2–21. GLCO Timing

2.4 Video Output Format

The TVP5040 supports both square-pixel and ITU-R BT.601 sampling formats and multiple Y-UV output formats:

- 20-bit 4:2:2
- 16-bit 4:2:2
- 10-bit 4:2:2
- 8-bit 4:2:2
- 10-bit ITU-R BT.656
- 8-bit ITU-R BT.656

2.4.1 Sampling Frequencies and Patterns

The sampling frequencies that control the number of pixels per line differ depending on the video format and standards. Table 2–1 shows a summary of the sampling frequencies. The TVP5040 outputs data in the 4:2:2 sampling pattern. Every second sample is both a luminance and chrominance sample. The remainder are luminance-only samples.

Table 2–1. Summary of Line Frequencies, Data Rates, and Pixel Counts

STANDARDS	HORIZONTAL LINE RATE (kHz)	PIXELS PER LINE	ACTIVE PIXELS PER LINE	PCLK FREQUENCY (MHz)	SCLK FREQUENCY (MHz)
NTSC, square-pixel	15.73426	780	640	12.2727	24.54
NTSC, ITU-R BT.601	15.73426	858	720	13.50	27.00
PAL(B,D,G,H,I), square-pixel	15.625	944	768	14.75	29.50
PAL(B,D,G,H,I),ITU-R BT.601	15.625	864	720	13.50	27.00
PAL(M),square-pixel	15.73426	780	640	12.2727	24.54
PAL(M),ITU-R BT.601	15.73426	858	720	13.50	27.00
PAL(Combination-N), square-pixel	15.625	944	768	14.75	29.50
PAL(Combination-N), ITU-R BT.601	15.625	864	720	13.50	27.00

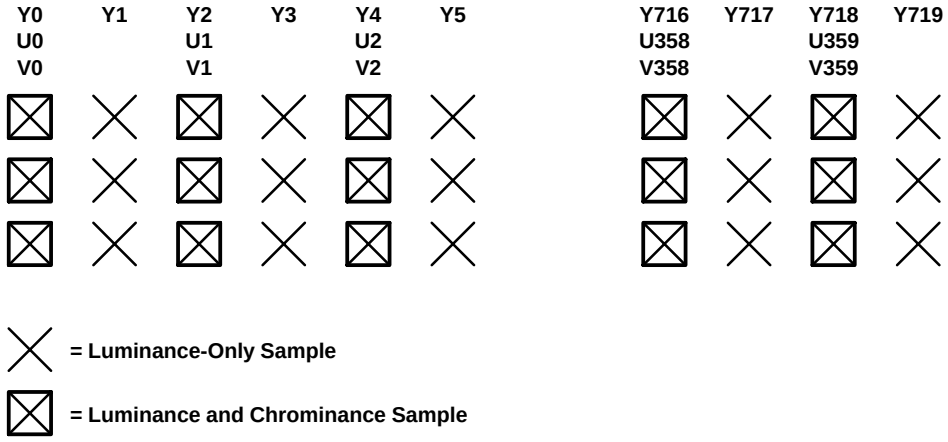


Figure 2–22. 4:2:2 Sampling

2.4.2 Video Port 20-Bit and 16-Bit 4:2:2 Output Format Timing

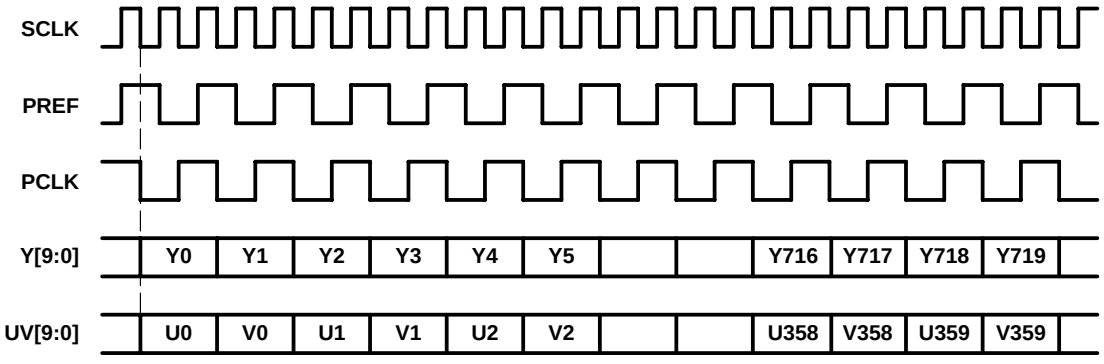
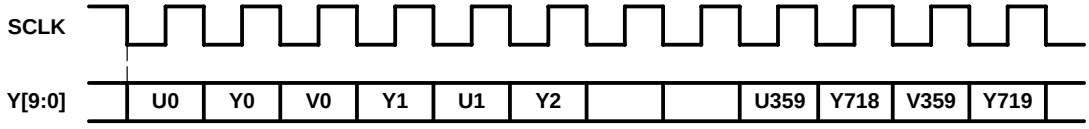


Figure 2–23. 20-Bit 4:2:2 Output Format

2.4.3 Video Port 10-Bit and 8-Bit 4:2:2 and ITU-R BT.656 Output Format Timing



UV[9:0] **HIGH**

Numbering shown is for 13.5-MHz sampling

Figure 2–24. 20-Bit 4:2:2 Output Format

2.5 Synchronization Signals

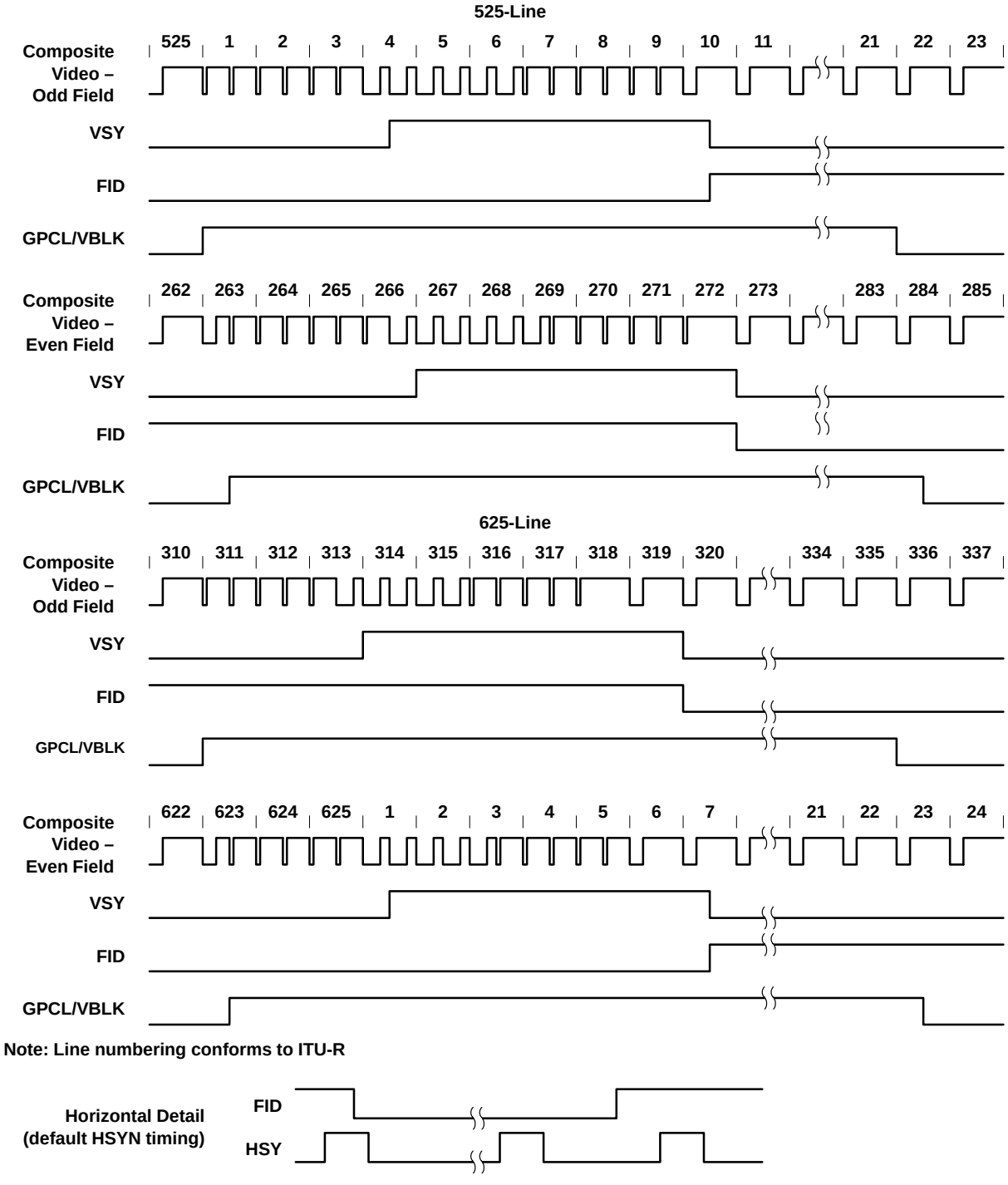


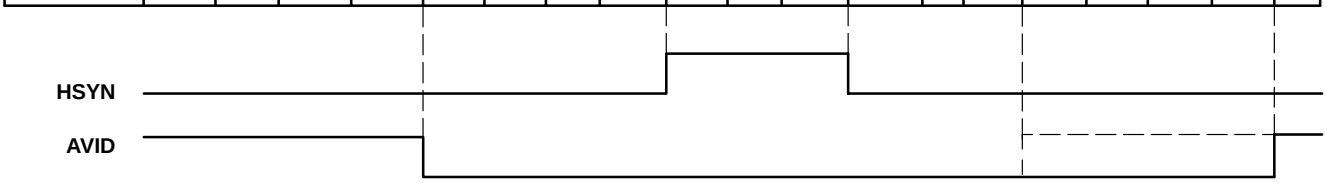
Figure 2–25. Vertical Synchronization Signals

10-bit 4:2:2 timing with 2x pixel clock (SCLK) reference. ITU-R BT.656 timing also shown.

NTSC 601	1436	1437	1438	1439	1440	1441	…	1471	1472	…	1599	1600	⋯	1711	1712	1713	1714	1715	0
PAL 601	1436	1437	1438	1439	1440	1441	…	1463	1464	…	1591	1592	⋯	1723	1724	1725	1726	1727	0
ITU 656 Datastream	Cb 359	Y 718	Cr 359	Y 719	FF	00	…	10	80	…	10	80	⋯	10	FF	00	00	XX	Cb 0

NTSC sqp	1276	1277	1278	1279	1280	1281	…	1323	1324	…	1451	1452	⋯	1555	1556	1557	1558	1559	0
ITU 656 Datastream	Cb 319	Y 638	Cr 319	Y 639	FF	00	…	10	80	…	10	80	⋯	10	FF	00	00	XX	Cb 0

PAL sqp	1532	1533	1534	1535	1536	1537	…	1579	1580	…	1707	1708	⋯	1883	1884	1885	1886	1887	0
ITU 656 Datastream	Cb 383	Y 766	Cr 383	Y 767	FF	00	…	10	80	…	10	80	⋯	10	FF	00	00	XX	Cb 0



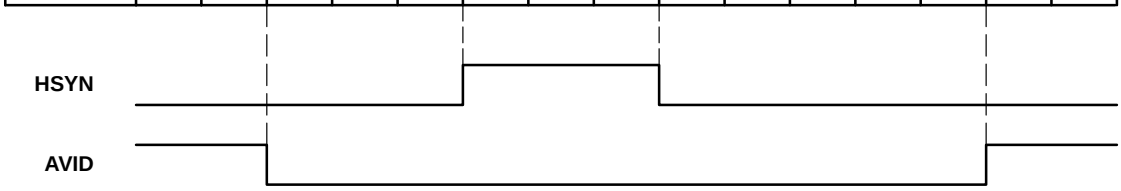
Note: AVID rising edge occurs 4 SCLK cycles early when in ITU656 output mode

(A)

The HSYN timing shown is valid when HSYN start (register 16) is set to its default value of 80h.

20-bit 4:2:2 timing with 1x pixel clock (PCLK) reference.

NTSC 601	718	719	720	…	735	736	…	799	800	…	855	856	857	0	1
PAL 601	718	719	720	…	731	732	…	795	796	…	861	862	863	0	1
NTSC sqp	638	639	640	…	661	662	…	725	726	…	777	778	779	0	1
PAL sqp	766	767	768	…	789	790	…	853	854	…	941	942	943	0	1



(B)

The HSYN timing shown is valid when HSYN start (register 16) is set to its default value of 80h.

Figure 2–26. Horizontal Synchronization Signals

2.6 Host Interface

The host interface is used to initialize the internal microprocessor, to read and write status registers, and to access sliced VBI data. The interface modes supported by TVP5040 are I^{2}C, three parallel interface modes, and VIP mode. The host interface is configured at power up and at reset using the GLCO, PALI, and FID terminals shown in Table 2–2.

Table 2–2. Host Port Select

TERMINALS	GLCO	PALI	FID
	2	**1**	**0**
I^{2}C	0	0	1
VIP	0	1	0
Parallel A	1	0	1
Parallel B	1	1	0
Parallel C	1	1	1

2.7 I^{2}C Host Interface

The TVP5040 host interface is configured for I^{2}C operation by attaching external pullup and pulldown resistors to the GLCO, PALI, and FID terminals. The following is the combination of resistors required to select I^{2}C host mode (1 is pullup and 0 is pulldown).

	GLCO	PALI	FID
I^{2}C Host Port Enabled	0	0	1

2.7.1 I^{2}C Host Port Select

The I^{2}C standard consists of two signals, serial input/output data (VC1) line and input/output clock line (VC0), which carry information between the devices connected to the bus. A third signal (VC3) is used for slave address selection. Although the I^{2}C system can be multimastered, the TVP5040 functions as a slave device only.

Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pullup resistor. When the bus is free, both lines are high.

The slave address select terminal (VC3) enables the use of two TVP5040 devices tied to the same I^{2}C bus.

Table 2–3 summarizes the terminal functions of the I^{2}C-mode host interface.

Table 2–3. I^{2}C Host Port Terminal Description

SIGNAL	TYPE	DESCRIPTION
VC3 (I2CA)	I	Slave address selection
VC0 (SCL)	I/O (open drain)	Input/output clock line
VC1 (SDA)	I/O (open drain)	Input/output data line

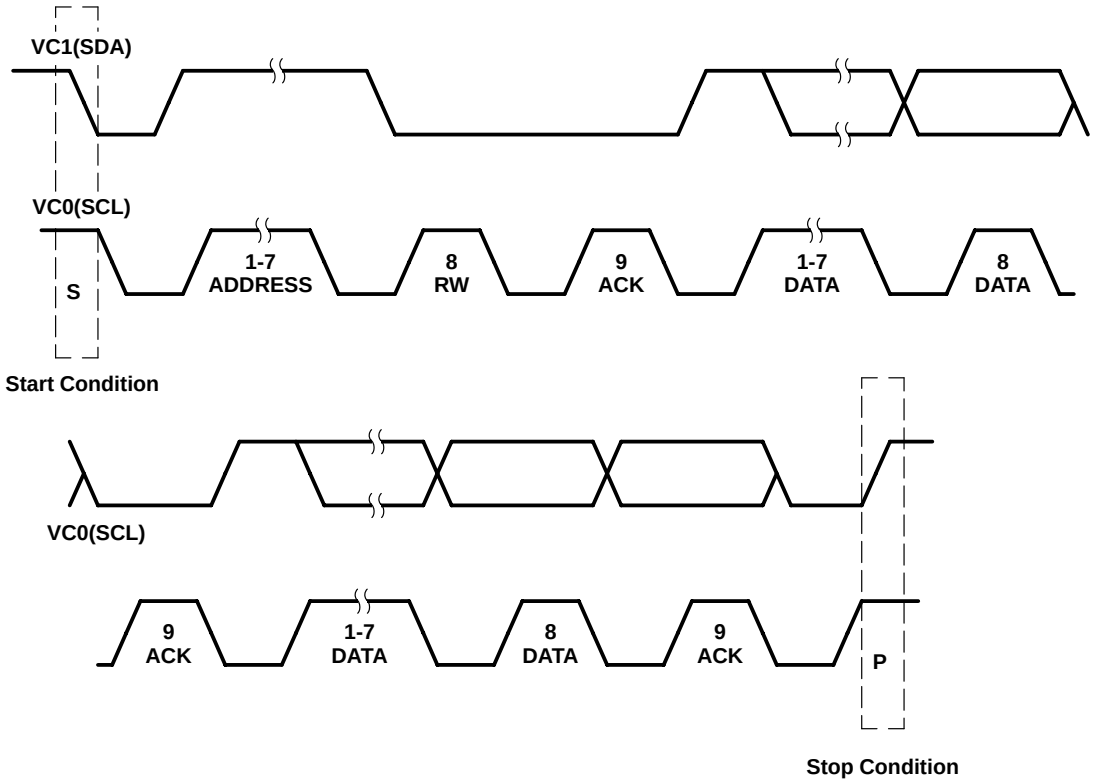


Figure 2–27. I²C Data Transfer

The data transfer rate on the bus is up to 400 kbits/s. The number of interfaces connected to the bus is dependent on the bus capacitance limit of 400 pF. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change with the clock signal on the SCL line being low.

- If multiple bytes are transferred during one read or write operation, the internal subaddress is automatically incremented.
- A high to low transition on the SDA line while the SCL is high indicates a start condition.
- A low to high transition on the SDA line while the SCL is high indicates a stop condition.
- Acknowledge (SDA low)
- Not-Acknowledge (SDA high)

Every byte placed on the SDA line must be 8-bits long. The number of bytes that can be transferred is unrestricted. Each byte must be followed by an acknowledge bit. If the slave can not receive another complete byte of data until it has performed another function, it can hold the clock line (SCL) low to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases the clock line (SCL).

The data transfer with acknowledgement is obligatory. The acknowledge related clock pulse is generated by the master. The master releases the SDA line high during the acknowledge clock pulse. The slave must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

When a slave does not acknowledge the slave address, the data line must be left high by the slave. The master can then generate a stop condition to abort the transfer.

If a slave does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line high and the master generates the stop condition.

If a master-receiver is involved in a transfer, it must signal the end of the data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a stop or repeated start condition.

2.7.2 I²C Write Operation

The data transfers occur utilizing the following illustrated formats.

An I²C master initiates a write operation to TVP5040 by generating a start condition followed by TVP5040s I²C address 101110X , the X in the TVP5040 address is 0 when VC3 terminal is tied low and is 1 when VC3 terminal is tied high, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the TVP5040, the master presents the subaddress of the register, or the first of a block of registers it wants to write, followed by one or more bytes of data, MSB first. The TVP5040 acknowledges each byte after completion of each transfer. The I²C master terminates the write operation by generating a stop condition.

STEP 1	**0**
I²C Start (master)	S

STEP 2	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C General address (master)	1	0	1	1	1	0	X	0

STEP 3	**9**
I²C Acknowledge (slave)	A

STEP 4	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Write register address (master)	addr	addr	addr	addr	addr	addr	addr	addr

STEP 5	**9**
I²C Acknowledge (slave)	A

STEP 6	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Write data (master)	Data	Data	Data	Data	Data	Data	Data	Data

STEP 7†	**9**
I²C Acknowledge (slave)	A

STEP 8	**0**
I²C Stop (master)	P

† Repeat steps 6 and 7 until all data has been written.

2.7.3 I²C Read Operation

The read operation consists of two phases. The first phase is the address phase. In this phase, an I²C master initiates a write operation to the TVP5040 by generating a start condition followed by the TVP5040s I²C address 101110X, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledge from the TVP5040, the master presents the subaddress of the register, or the first of a block of registers it wants to read. After the cycle is acknowledged, the master terminates the cycle immediately by generating a stop condition. The second phase is the data phase. In this phase, a I2C master initiates a read operation to TVP5040 by generating a start condition followed by the TVP5040s I²C address 101110X, in MSB first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from TVP5040, the I²C master receives one or more bytes of data from the TVP5040. The I²C master acknowledges the transfer at the end of each byte. After the last data byte desired has been transferred from the TVP5040 to the master, the master generates a not acknowledge followed by a stop.

2.7.3.1 Read Phase 1:

STEP 1	**0**
I2C Start (master)	S

STEP 2	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C General address (master)	1	0	1	1	1	0	X	0

STEP 3	**9**
I2C Acknowledge (slave)	A

STEP 4	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C Read register address (master)	addr	addr	addr	addr	addr	addr	addr	addr

STEP 5	**9**
I2C Acknowledge (slave)	A

STEP 6	**0**
I2C Stop (master)	P

2.7.3.2 Read Phase 2:

STEP 7	**0**
I2C Start (master)	S

STEP 8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C General address (master)	1	0	1	1	1	0	X	1

STEP 9	**9**
I2C Acknowledge (slave)	A

STEP 10	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C Read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

STEP 11†	**8**
I2C Acknowledge (master)	A

STEP 12	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C Read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

STEP 13	**9**
I2C Not acknowledge (master)	$\overline{A}$

STEP 14	**0**
I2C Stop (master)	P

† Repeat steps 10 and 11 for all but the last byte read.

2.7.4 I²C Microcode Write Operation

A microcode write operation is required to down load microcode to the TVP5040 program RAM after power-up reset. During the write cycle the internal microprocessors program counter resets and points to location zero in the program RAM and remains reset. Upon completion of the write operation, a microprocessor CLEAR-RESET operation is required. This is performed by writing into the 7F register to clear reset and resume microprocessor function. (There is no specific data requirement to be written into the 7F register, any data will resume microprocessor function.)

STEP 1	**0**
I²C Start (master)	S

STEP 2	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C General address (master)	1	0	1	1	1	0	X	0

STEP 3	**9**
I²C Acknowledge (slave)	A

STEP 4	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Write register address (master)	0	1	1	1	1	1	1	0

Write to program RAM address=7E

STEP 5	**9**
I²C Acknowledge (slave)	A

STEP 6	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Write data (master)	Data	Data	Data	Data	Data	Data	Data	Data

STEP 7†	**9**
I²C Acknowledge (slave)	A

STEP 8	**0**
I²C Stop (master)	P

† Repeat steps 6 and 7 until all data has been written.

2.7.5 Microprocessor CLEAR-RESET

STEP 1	**0**
I2C Start (master)	S

STEP 2	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C General address (master)	1	0	1	1	1	0	X	0

STEP 3	**9**
I2C Acknowledge (slave)	A

STEP 4	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C Write register address (master)	0	1	1	1	1	1	1	1

Write to microprocessor clear reset address=7F

STEP 5	**9**
I2C Acknowledge (slave)	A

STEP 6	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C Write data (master)	Data	Data	Data	Data	Data	Data	Data	Data

Any data written to 7F starts the microprocessor.

STEP 7	**9**
I2C Acknowledge (slave)	A

STEP 8	**0**
I2C Stop (master)	P

2.7.6 I²C Microcode Read Operation

The data written during the microcode write operation can be read from the TVP5040 program RAM. During the read cycle, the internal microprocessors program counter resets and points to location zero in the program RAM and remains reset. Upon completion of the read operation, a microprocessor CLEAR-RESET operation is required. This is performed by writing into the 7F register to clear reset and resume the microprocessor function. (There is no specific data requirement to be written into the 7F register, any data resumes the microprocessor function.)

STEP 1	**0**
I²C Start (master)	S

STEP 2	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C General address (master)	1	0	1	1	1	0	X	0

STEP 3	**9**
I²C Acknowledge (slave)	A

STEP 4	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Read register address (master)	1	0	0	0	1	1	1	0

Read address=8E

STEP 5	**9**
I²C Acknowledge (slave)	A

STEP 6	**0**
I²C Stop (master)	P

2.7.6.1 Read Phase 2:

STEP 7	**0**
I²C Start (master)	S

STEP 8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C General address (master)	1	0	1	1	1	0	X	1

STEP 9	**7**
I²C Acknowledge (slave)	A

STEP 10	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

STEP 11	**7**
I²C Acknowledge (master)	A

Repeat STEP 10 and STEP 11 for all but the last byte read from program RAM.

STEP 12	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

STEP 13	**9**
I²C Not acknowledge (master)	$\overline{A}$

STEP 14	**0**
I²C Stop (master)	P

2.8 VIP Host Interface Port

The TVP5040 host interface is configured for video interface port (VIP) operation by attaching external pullup and pulldown resistors to the GLCO, PALI, and FID terminals. The following is the combination of resistors required to select VIP host mode, where 0=pulldown and 1=pullup.

	GLCO	PALI	FID
VIP host port enabled	0	1	0

The video interface port is a standard interface, conforming to the Video Electronics Standards Association (VESA™) VIP specification version 2.0 between a video enabled graphics device and one or more video devices. The video port of VIP transports various types of real-time signal streams. Signal names in parenthesis ( ) denote the signal name referenced in the VIP specification. Five terminals are required for host port transfers: VC3, VC0, VC1, VC2, and INTREQ. Table 2–4 summarizes the terminal functions of the VIP-mode host interface.

2.8.1 VIP Host Port Terminal Description

Table 2–4. VIP Host Port Terminal Description

SIGNAL	TYPE	DESCRIPTION
VC3 (VIPCLK)	O	VIP host clock (25-33 MHz)
VC0,VC1 (HAD[0:1])	I/O	Host address/data bus VC0 = (HAD_0) VC1 = (HAD_1)
VC2 (HCTL)	I/O (open drain)	Host control. This includes the symbolic signals of VFRAME, DTACK and VSTOP.
INTREQ ($\overline{\text{VIRQ}}$)	O (nominal open drain)	Interrupt request

VC3 (VIPCLK) is the host port clock, specified from 25-33 MHz. VIPCLK can be from any source.

VC0 and VC1 (HAD[0:1]) is a two wire bus, used to transfer commands, addresses and data between master and slave devices.

VC2 (HCTL) is a shared control terminal. It is driven by the master to initiate and terminate data transfers. It is driven by the slave to terminate and add wait states to data transfers. Because it is a shared control signal, special attention must be given to its generation to avoid bus conflicts.

INTREQ is a nominally open drain terminal used to signal interrupts to the host controller. This terminal may be configured as a conventional CMOS I/O buffer (non-open drain) if desired using the interrupt configuration register at subaddress C2. Contention is possible if multiple devices are connected to the INTREQ signal and it is configured in non-open drain mode.

Upon power up, the VIP module outputs remain in the high impedance state until a request from the motherboard signals the module to begin driving the bus.

VESA is a trademark of Video Electronics Standards Association.

2.8.2 VIP Phases

Figure 2–28 illustrates an example of a typical VIP transfer and Table 2–5 describes the sequence of phases involved in the VIP data transfer.

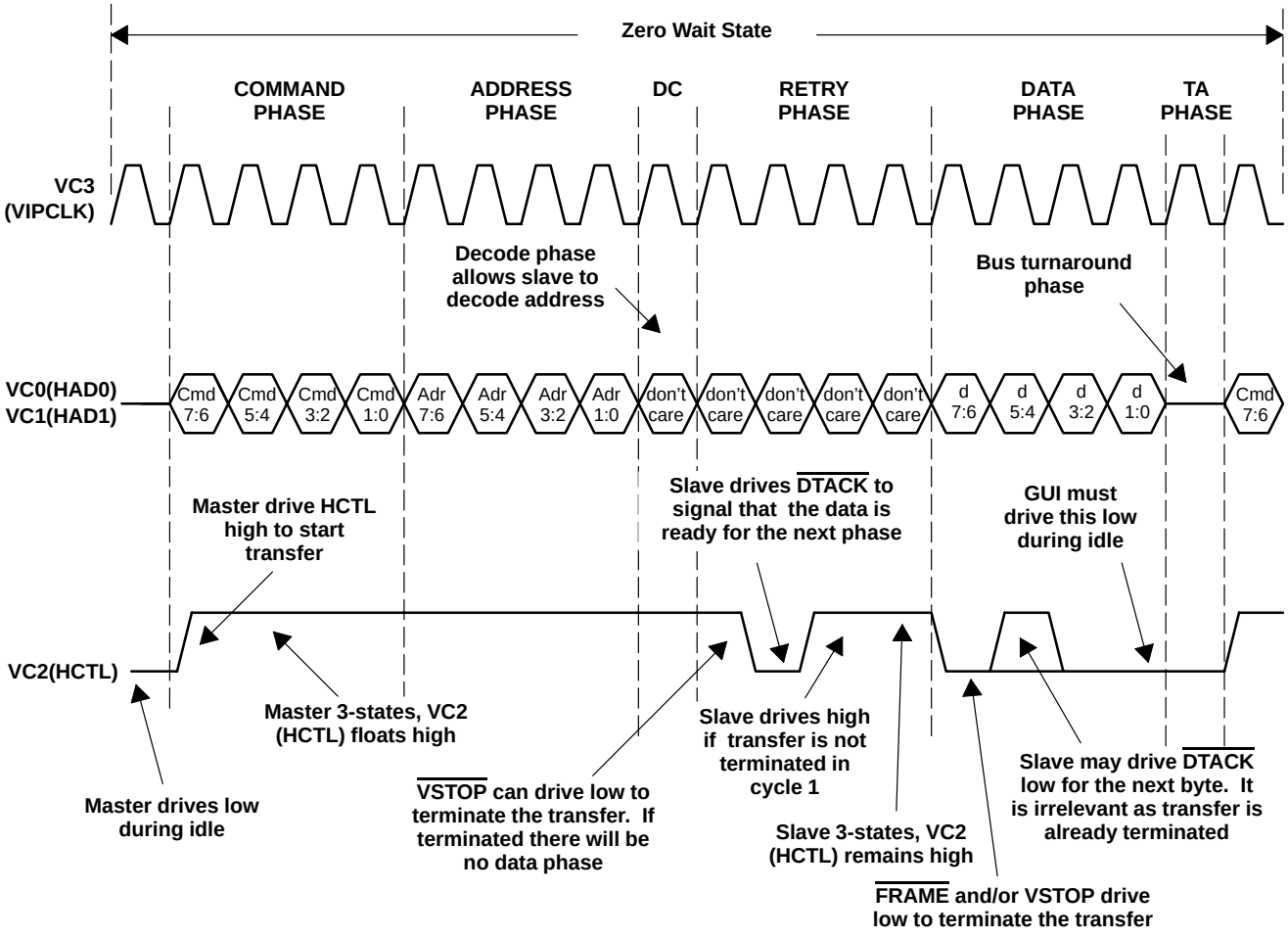


Figure 2–28. VIP Transfer

Table 2–5. VIP Host Port Phase Description

PHASE	EXPLANATION
Command	All host port transfers start with a command phase. The 8-bit command/address byte is multiplexed onto VC0 and VC1 (HAD[1:0]) during the command phase. The command byte selects between devices, read, and write cycles, register or FIFO transfers and contains the most significant four bits of the register address.
Address	During register transfers the command phase is followed by the address extension phase. The least significant 8-bits of the VIP register address are multiplexed onto VC0 and VC1 (HAD[1:0]) during the address extension phase. This phase is not present during FIFO transfers.
Decode	Following the command or command/address phase(s), a one clock delay is required to allow slave devices to decode the address and determine if they are able to respond within the 1 wait phase requirement for active operation.
Retry	The four clock cycles immediately following the decode phase constitute the retry phase. During the retry phase, the slave indicates its desire to terminate the operation without transferring any data (retry), add a wait phase or transfer the first byte of data. When the slave asserts VSTOP, the transfer ends with the retry phase. When the slave neither terminates the transfer nor accepts the byte, the retry phase is followed by a wait phase.
Wait	During the second cycle of a decode, retry or wait phase, the slave indicates its ability to transfer the next byte of data by driving VC2 (HCTL) low. When the slave does not drive VC2 (HCTL) low and the transfer is not terminated, the current phase is followed by a wait phase. During wait phases, the current owner (master for writes, slave for reads) continues to drive the HAD bus however no data is transferred. the slave is allowed to add one wait phase per byte to register accesses without compromising system timing. Additional wait phases are not prevented but overall system reliability may be compromised.
Data	When VC2 (HCTL) is deasserted during cycle 1 of a retry, wait or data phase, the current phase is followed by a data phase. Data is transferred between master and slave devices during data phases, multiplexed onto VC0 and VC1 (HAD[1:0]).
TA	Immediately following the last transfer phase of a read transfer, a one cycle delay is required giving the slave time to 3-state the VC0 and VC1 (HAD) bus. The master is free to begin a new bus transfer, driving VC0 and VC1 (HAD) and VC2 (HCTL) immediately following the TA phase.

2.8.3 VIP Commands and Address Space

Table 2–6 summarizes the supported VIP commands and the address space mapping. Note that only three of the four VIP FIFO DMA channels are used by TVP5040. The VBI data FIFO is mapped to FIFO A, the program memory for write operation is mapped to FIFO B, and the program memory for read operation is mapped to FIFO C. FIFO D is not used by TVP5040 and therefore is indicated as *not present* in the VIP status 1 register.

Table 2–6. Summary of VIP Commands and Address Spaces

COMMAND			Cmd/Addr	REGISTER ADDRESS	DATA	COMMENT
[7:4]			[3:0]	[7:0]	[7:0]	
01	0/1	0	0000	00000000 through 11111111	dddddddd	VIP configuration registers
01	0/1	0	0001	00000000 through 11111111	dddddddd	General TVP5040 registers
01	1	0	0010	00000000 through 11111111	xxxxxxxx	No latency read access 1 phase
01	1	0	0011	Address as previously written	ddddddd	No latency read access 2 phase
01	1	1	0000	No address phase	xx0/1xxx0/1	FIFO status 0 read
01	1	1	0001	No address phase	xxxxxx11	FIFO status 1 read
01	1	1	0100	No address phase	dddddddd	FIFO VBI data read (FIFO A)
01	0	1	0101	No address phase	dddddddd	FIFO program memory write (FIFO B)
01	1	1	0110	No address phase	dddddddd	FIFO program memory read (FIFO C)

2.8.4 Command Byte

During the command phase, the hardware control line(VC2) transitions high and the hardware address lines (VC0 and VC1) transmit the command byte from the host to the TVP5040. The command byte determines the nature of the data transfer and the TVP5040 address space which is affected.

	7	6	5	4	3	2	1	0
Command	DEVSEL1 (0)	DEVSEL0 (1)	R/W	F/R	A11	A10	A9	A8

NAME	DESCRIPTION
DEVSEL1:0	Device select. Always 01 for TVP5040
R/W	1=Read 0=Write
F/R	1=FIFO 0=Register access
A11:8	Address bus upper 4 bits For register accesses: 0000 = VIP-specific configuration registers 0001 = General TVP5040 registers 0010 = No latency read access phase 1 0011 = No latency read access phase 2 For FIFO accesses: 0000 = FIFO status 0 0001 = FIFO status 1 0100 = VBI FIFO 0101 = Program memory write FIFO 0110 = Program memory read FIFO

2.8.4.1 Access Latency and Wait States

VIP accesses to registers or the VBI FIFO may require the TVP5040 to insert one or more wait states into the access sequence. For register accesses the wait states may total up to 64 μs. All normal writes release the host port immediately but internal wait states continue to be generated until the operation completes. Any attempt to access the host port while the write operation has not completed results in slave termination by the TVP5040. For burst writes, the TVP5040 inserts wait states that may total up to 64 μs. Reads (except for no-latency reads detailed in section 2.8.4.2) hold the host port until completion. Figure 2–29 through Figure 2–32 illustrate examples of VIP accesses with wait states and slave termination by the TVP5040.

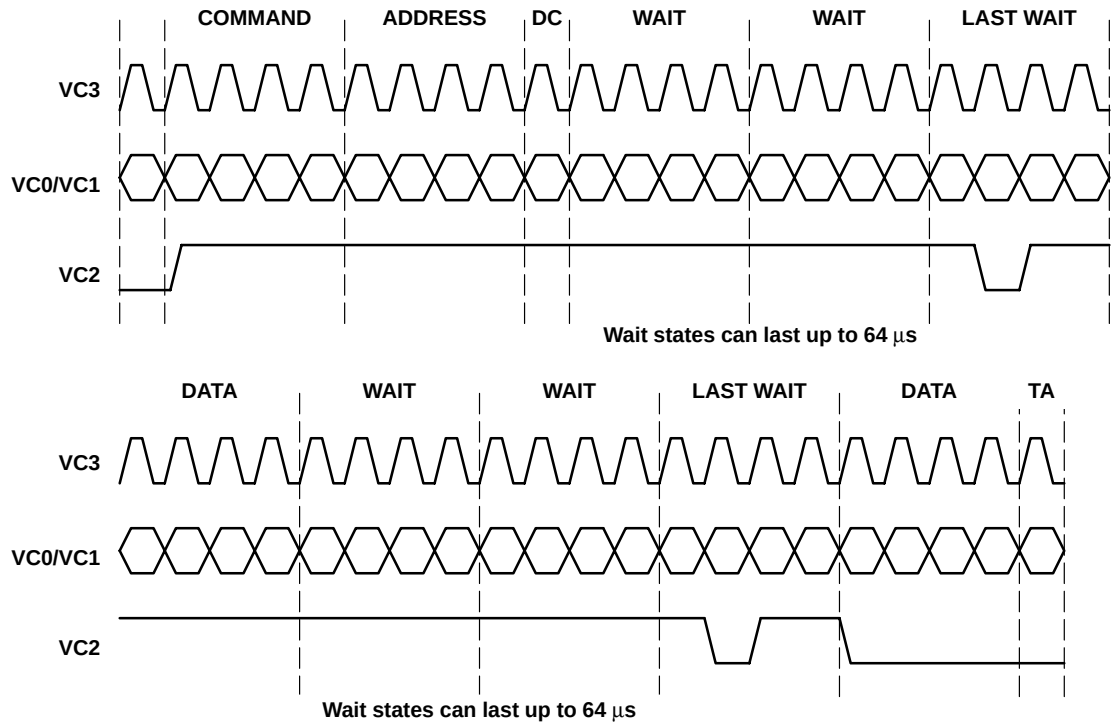


Figure 2–29. Reading From Registers With Wait States

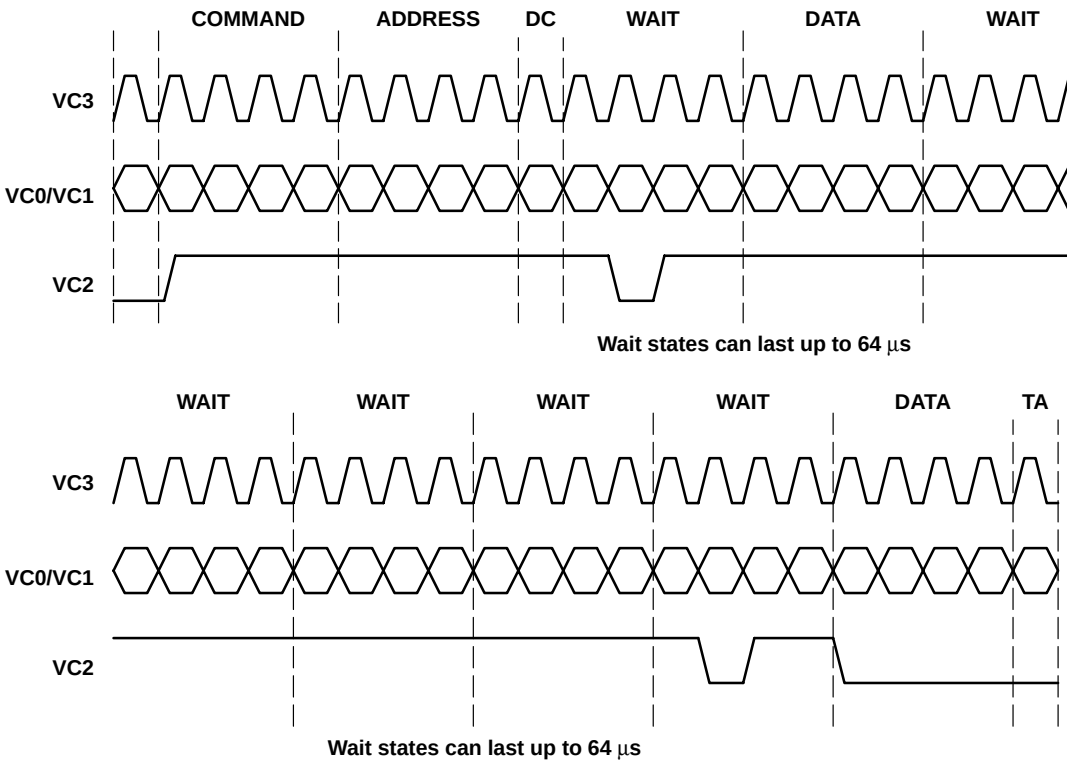


Figure 2–30. Writing to Registers With Wait States (Burst Write)

Write commands require one wait state before the data phase. For burst writes, subsequent data phases may require wait states up to 64 µs. Wait states before the second or subsequent data phases are not fixed.

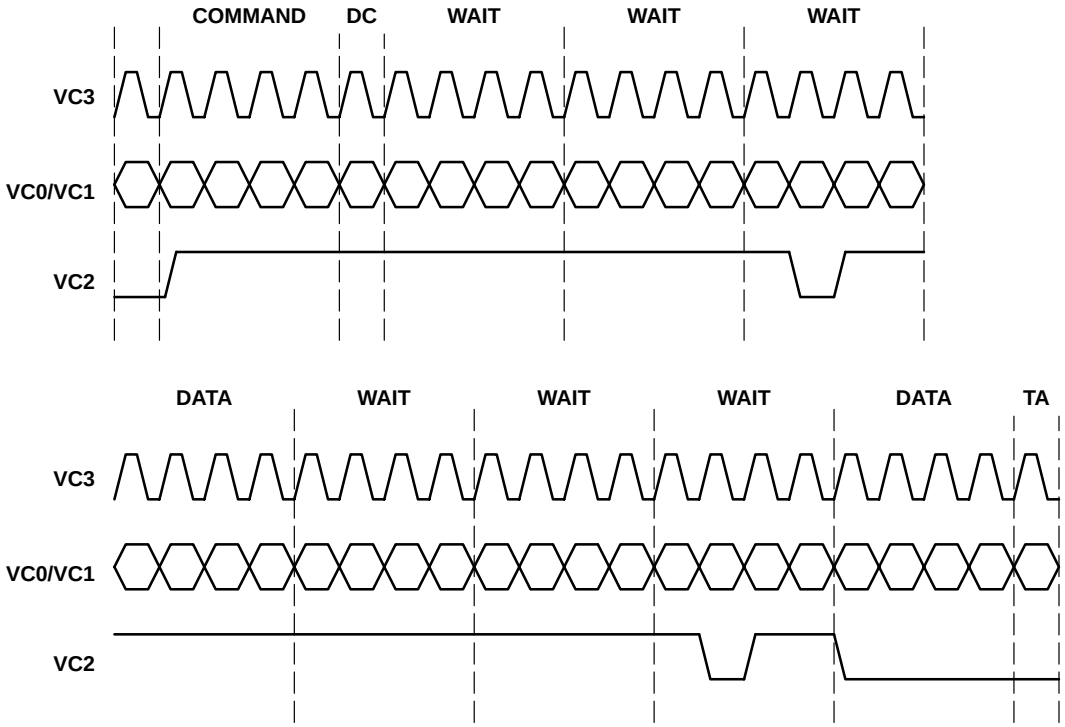


Figure 2–31. Reading From FIFO With Wait States

Read commands from the FIFO typically require three wait states when running at full speed (VIPCLK at 25 MHz).

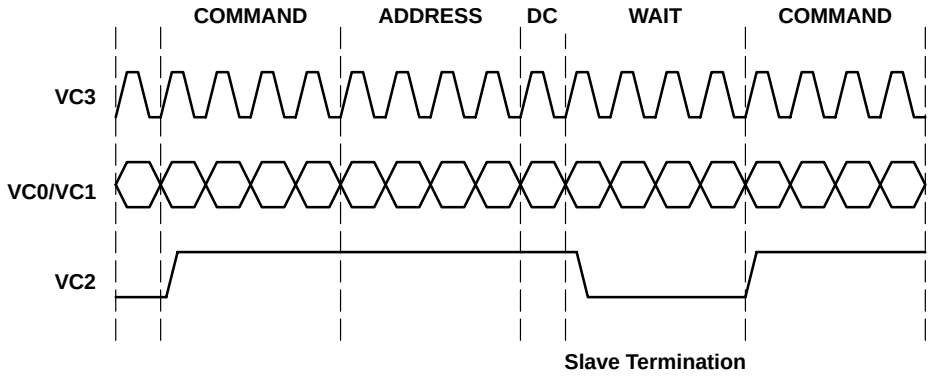


Figure 2–32. Slave Termination

VIP Configuration Registers: The TVP5040 supports VIP configuration registers which are accessible only in VIP host mode. Information on the register functions is available in section 2.13, VIP subaddresses 000-0FF. VIP configuration registers are read-only.

	COMMAND PHASE								ADDRESS PHASE								DATA PHASE (from TVP5040)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
VIP configuration register read	0	1	1	0	0	0	0	0	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D

General TVP5040 Registers: The bulk of the TVP5040 register space consists of status and control registers that are available to the host in I^2C, VIP, and VMI modes. Information on the register functions is available in section 2.14 VIP subaddresses 100-1FF.

	COMMAND PHASE								ADDRESS PHASE								DATA PHASE (from TVP5040)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
General TVP5040 register read	0	1	1	0	0	0	0	1	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D

	COMMAND PHASE								ADDRESS PHASE								DATA PHASE (to TVP5040)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
General TVP5040 register write	0	1	0	0	0	0	0	1	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D

2.8.4.2 No Latency Read

In order to avoid holding up the host port due to the extended wait states of a normal read operation, a special *no latency read* mode is implemented in TVP5040.

NOTE: This special mode is not part of the VIP specification.

The no latency read consists of two zero wait-state phases separated by an idle period, during which the host may perform other operations. The first phase identifies the register address to be read. In response to the first phase read, the TVP5040 outputs data immediately from an internal intermediate buffer. Note that the data in the intermediate data buffer is not from the register currently being addressed.

Following completion of the first phase, the host must wait for 64 μs to ensure that the data requested in the first phase is available in the intermediate data buffer. Any attempt to use the host port during this time results in slave termination by TVP5040. The host then initiates the second phase to read the data from the intermediate buffer.

	COMMAND PHASE								ADDRESS PHASE								DATA PHASE (from TVP5040)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
No latency read Phase 1	0	1	1	0	0	0	1	0	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X

	COMMAND PHASE								ADDRESS PHASE								DATA PHASE (from TVP5040)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
No latency read Phase 2	0	1	1	0	0	0	1	1	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D

A *pipelined* read of several registers can be done by having the host initiate a series of back-to-back phase 1 reads, with each phase 1 read occurring at least 64 μs from the previous phase 1 read. With this, for every phase 1 read, the TVP5040 returns the data for the previous phase 1 read. Finally, at the end, the host must initiate a phase 2 read to get the data for the last read transaction.

	COMMAND PHASE								ADDRESS PHASE								DATA PHASE (from TVP5040)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
No latency read (pipelined) Phase 1	0	1	1	0	0	0	1	0	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X

	COMMAND PHASE								ADDRESS PHASE								DATA PHASE (from TVP5040)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
No latency read (pipelined) Phase 1	0	1	1	0	0	0	1	1	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D

	COMMAND PHASE								ADDRESS PHASE								DATA PHASE (from TVP5040)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
No latency read (pipelined) Phase 2	0	1	1	0	0	0	1	1	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D

2.8.4.3 FIFO Status 0 Register

The FIFO status 0 register returns two bits which report status and six unused bits.

7	6	5	4	3	2	1	0
Undefined	Undefined	Undefined	DREQA	Undefined	Undefined	Undefined	VIRQ

DREQA: DMA request for FIFO A. This bit is the same as the teletext threshold bit (bit 1 of the interrupt status register at VIP subaddress 1C0). See section 2.14 for the definition of this bit.

VIRQ: This bit returns the status of the INTREQ terminal. Reading this bit does not clear the terminal.

	COMMAND PHASE								DATA PHASE							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FIFO status 0 read	0	1	1	1	0	0	0	0	d	d	d	0/1	d	d	d	0/1

There is no address phase associated with reading the FIFO status 0 register.

2.8.4.4 FIFO Status 1 Register

The FIFO status 1 register returns the status of the FIFO DMA channels in TVP5040.

7	6	5	4	3	2	1	0
Undefined	PRESENT-D (0)	R/W-C (1)	PRESENT-C (1)	R/W-B (0)	PRESENT-B (1)	R/W-A (1)	PRESENT-A (1)

R/W: This bit is set to 1 if the FIFO is a read port.

PRESENT: This bit is set to 1 if the FIFO is present, otherwise it is set to 0.

	COMMAND PHASE								DATA PHASE							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FIFO status 1 read	0	1	1	1	0	0	0	1	0	0	1	1	0	1	1	1

There is no address phase associated with reading the VBI FIFO 1 register. This register is read-only and is always set to 0x37.

2.8.4.5 VBI FIFO (FIFO A)

The VBI FIFO stores sliced VBI data in the format described in section 2.9.1. Data may be read from the FIFO at the average rate of 1 data byte per 3 cycles (1 data cycles, 2 wait cycles) when the VIPCLK is at maximum speed.

	COMMAND PHASE								DATA PHASE							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VBI FIFO read	0	1	1	1	0	1	0	0	D	D	D	D	D	D	D	D

There is no address phase associated with reading the VBI FIFO. FIFO polling is implemented.

2.8.5 VIP Microcode Write Operation (FIFO B)

A microcode write operation is required to download microcode to the TVP5040 program RAM after power-up reset. During the write cycle, the internal microprocessors program counter resets and points to location zero in the program RAM and remains reset. Upon completion of the write operation, a microprocessor CLEAR-RESET operation is required. This is performed by writing into the 017F register to clear reset and resume the microprocessor function. (There is no specific data requirement to be written into the 017F register; any data resumes the microprocessor function.)

	COMMAND PHASE								DATA PHASE (toTVP5040)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Microcode write	0	1	0	1	0	1	0	1	D	D	D	D	D	D	D	D
Program RAM FIFO for write																

	COMMAND PHASE								ADDRESS PHASE								DATA PHASE (to TVP5040)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Clear reset	0	1	0	0	0	0	0	1	0	1	1	1	1	1	1	1	D	D	D	D	D	D	D	D

There is no address phase associated with writing to the program RAM.

2.8.6 VIP Microcode Read Operation (FIFO C)

The data written during the microcode write operation can be read from the TVP5040 program RAM. During the read cycle, the internal microprocessors program counter resets and points to location zero in the program RAM and remains reset. Upon completion of the read operation, a microprocessor CLEAR-RESET operation is required. This is performed by writing into the 017F register to clear reset and resume the microprocessor function. (There is no specific data requirement to be written into the 017F register; any data resumes the microprocessor function.)

	COMMAND PHASE								DATA PHASE (from TVP5040)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Microcode read	0	1	1	1	0	1	1	0	D	D	D	D	D	D	D	D
Program RAM FIFO for Read																

	COMMAND PHASE								ADDRESS PHASE								DATA PHASE (from TVP5040)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Clear reset	0	1	0	0	0	0	0	1	0	1	1	1	1	1	1	1	D	D	D	D	D	D	D	D

There is no address phase associated with reading the program RAM.

2.8.7 Parallel Host Interface A

Parallel host interface A is compatible with the video module interface (VMI) proposal version 1.4 mode A. The terminal descriptions are defined in Table 2–7.

Table 2–7. Parallel Host Interface A Terminal Description

TERMINAL	SIGNAL	TYPE	DESCRIPTION
A[1:0]	HA[1:0]	I	Address bus from host
D[7:0]	HD[7:0]	I/O	Bidirectional data bus
VC3	$\overline{CS}$	I	Chip select, active low
VC2	$\overline{DS}$	I	Data strobe, active low
VC1	RD/$\overline{WR}$	I	Read, active high — Write, active low
VC0	$\overline{DTACK}$	O	Data acknowledge
INTREQ	INTREQ	O	Interrupt request, active low and open drain by default, an external pullup resistor is required—can be configured as a conventional CMOS buffer, active high with no external pullup resistor.

Parallel host interface A timing is shown in the Figure 2–33. The cycle is initiated by the host when VC2-$\overline{DS}$ transitions low. The TVP5040 responds by pulling VC0-$\overline{DTACK}$ low to indicate data has been received or that the requested data is present on the bus. The host then completes the cycle by pulling VC2-$\overline{DS}$ high. Once the host has completed the cycle, the TVP5040 sets VC0-$\overline{DTACK}$ to high impedance. A pullup is required to pull VC0-$\overline{DTACK}$ high to indicate the operation is complete.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su(1)}$	A[1:0],D[0:7], RD/$\overline{WR}$ setup until $\overline{DS}$ low		5			ns
$t_{d(1)}$	Delay $\overline{DTACK}$ low after $\overline{DS}$ low		0			ns
$t_{h(1)}$	A[1:0], D[0:7], RD/$\overline{WR}$ hold after $\overline{DS}$ high		5			ns
$t_{d(2)}$	Delay $\overline{DS}$ high after $\overline{DTACK}$ low		5			ns
$t_{d(3)}$	Delay $\overline{DTACK}$ high after $\overline{DS}$ high		0			ns
$t_{d(4)}$	Delay $\overline{DS}$ low(next cycle) after $\overline{DTACK}$ high		5			ns
$t_{su(2)}$	(Read cycle) D[7:0] setup until $\overline{DTACK}$ low		10			ns
$t_{h(2)}$	(Read cycle) D[7:0] hold after $\overline{DS}$ high		0			ns

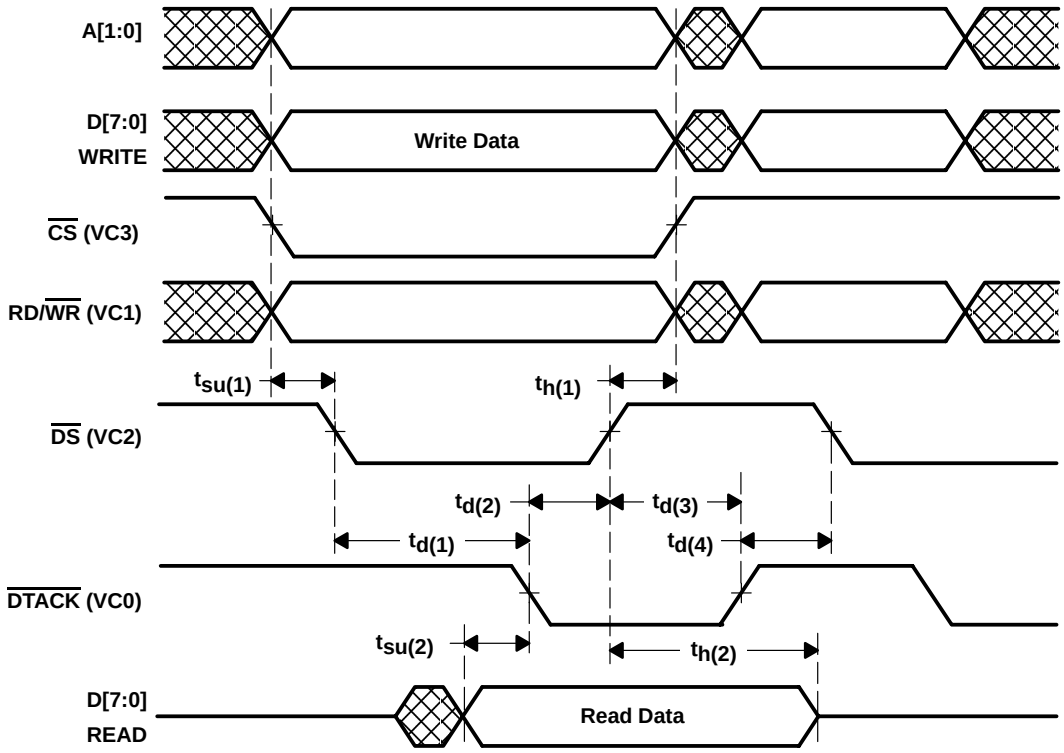


Figure 2–33. Parallel Host Interface A Timing

2.8.8 Parallel Host Interface B

Parallel host interface B is compatible with the video module interface (VMI) proposal version 1.4 mode B. The terminal descriptions are defined in Table 2–8.

Table 2–8. Parallel Host Interface B Terminal Description

TERMINAL	SIGNAL	TYPE	DESCRIPTION
A[1:0]	HA[1:0]	I	Address bus from host
D[7:0]	HD[7:0]	I/O	Bidirectional data bus
VC3	$\overline{CS}$	I	Chip select, active low
VC2	$\overline{RD}$	I	Read, active low
VC1	$\overline{WR}$	I	Write, active low
VC0	RDY	O	Ready, active high
INTREQ		O	Interrupt request, active low and open drain by default, an external pullup resistor is required—can be configured as a conventional CMOS buffer, active high with no external pullup resistor.

The parallel host interface B timing is shown in Figure 2–34. The cycle is initiated by the host when VC2-$\overline{RD}$ or VC1-$\overline{WR}$ transitions low. The TVP5040 responds by pulling VC0-RDY low. The TVP5040 then sets VC0-RDY to high impedance. A pullup resistor is required to indicate the data was received or that the requested data is present on the bus. The host then completes the cycle by pulling the asserted signal, VC2-$\overline{RD}$ or VC1-$\overline{WR}$ high.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su(3)}$	A[1:0], $\overline{CS}$ setup until $\overline{WR}$ or $\overline{RD}$ active		10			ns
$t_{h(3)}$	A[1:0], $\overline{CS}$ hold after $\overline{WR}$ or $\overline{RD}$ inactive		10			ns
$t_{d(5)}$	Delay RDY low after $\overline{WR}$ or $\overline{RD}$ active				28	ns
$t_{su(4)}$	D[7:0] setup until $\overline{WR}$ active		5			ns
$t_{h(4)}$	D[7:0] hold after $\overline{WR}$ inactive		10			ns
$t_{w(1)}$	RDY inactive pulse width		10			ns
$t_{w(2)}$	$\overline{WR}$ inactive until any command active		80			ns
$t_{su(5)}$	(Read cycle) D[7:0] setup until RDY active		0			ns
$t_{h(5)}$	(Read cycle) D[7:0] hold after $\overline{RD}$ inactive		0			ns
$t_{d(6)}$	Delay $\overline{WR}$ or $\overline{RD}$ inactive after RDY active		0			ns
$t_{w(3)}$	$\overline{WR}$, $\overline{RD}$ command pulse width		40			ns

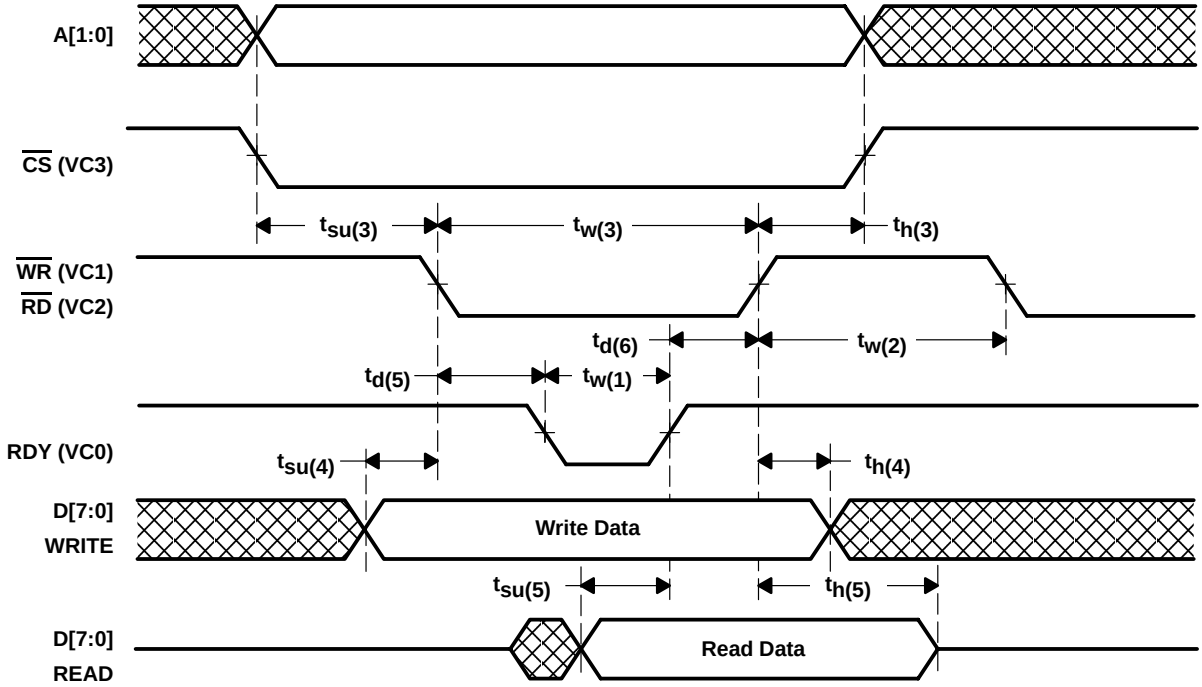


Figure 2–34. Parallel Host Interface B Timing

2.8.9 Parallel Host Interface C

The terminal descriptions are defined in Table 2–9.

Table 2–9. Parallel Host Interface C Terminal Description

TERMINAL	SIGNAL	TYPE	DESCRIPTION
A[1:0]	HA[1:0]	I	Address bus from host
D[7:0]	HD[7:0]	I/O	Bidirectional data bus
VC3	$\overline{CS}$	I	Chip select, active low
VC2	$\overline{DS}$	I	Data strobe, active low
VC1	RD/$\overline{WR}$	I	Read, active high—Write, active low
VC0	$\overline{RDY}$	O	Ready, active high
INTREQ		O	Interrupt request, active low and open drain by default, an external pullup resistor is required—can be configured as a conventional CMOS buffer, active high with no external pullup resistor.

Parallel host interface C timing is shown in Figure 2–35. The cycle is initiated by the host when VC2-$\overline{DS}$ transitions low. The TVP5040 responds by pulling VC0-RDY low. The TVP5040 will then set VC0-RDY to high impedance, a pullup resistor is required to indicate the data was received or that the requested data is present on the bus. The host then completes the cycle by pulling VC2-$\overline{DS}$ high.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su(6)}$	A[1:0],D[7:0], RD/$\overline{WR}$, $\overline{CS}$ setup until $\overline{DS}$ low		5			ns
$t_{h(6)}$	A[1:0],D[7:0], RD/$\overline{WR}$, $\overline{CS}$ hold after $\overline{DS}$ high		0			ns
$t_{d(7)}$	Delay RDY low after $\overline{DS}$ low		2			ns
$t_{su(7)}$	(Read cycle) D[7:0] setup until RDY high		20			ns
$t_{h(7)}$	(Read cycle) D[7:0] hold after $\overline{DS}$ high		0			ns

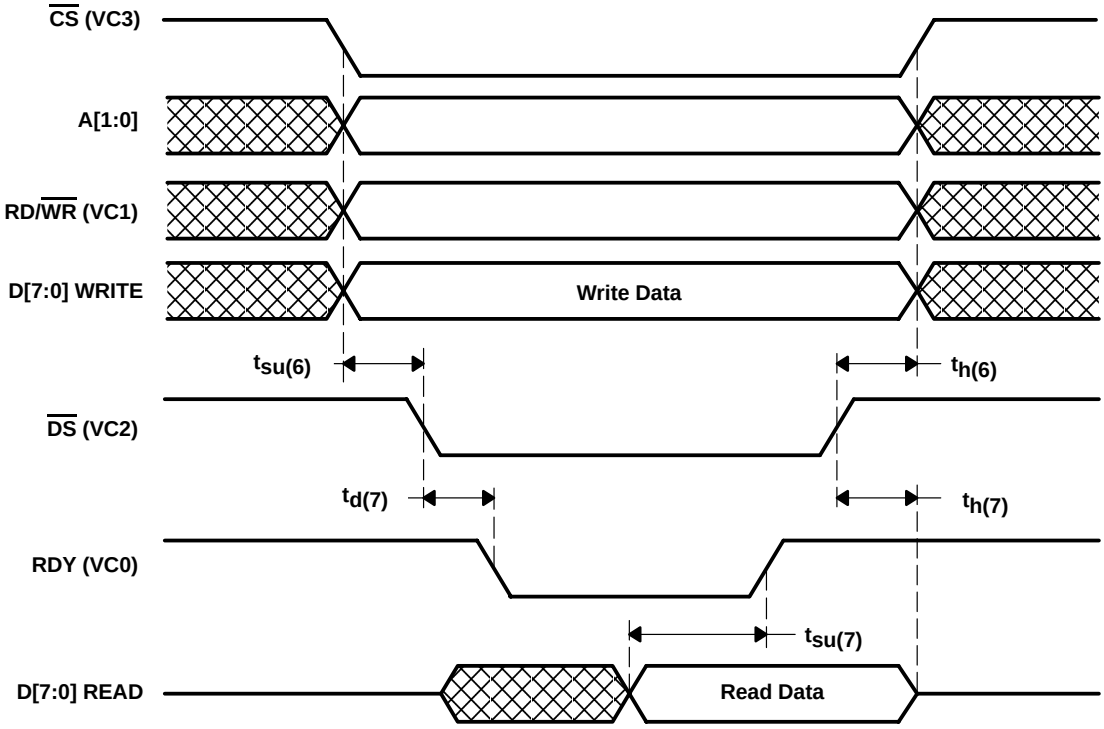


Figure 2–35. Parallel Host Interface C Timing

2.8.10 Parallel Host Interface Register Map

The parallel host interface (PHI) module contains only four registers that are directly accessible to the host (see Figure 2–36). The address register holds an indirect address for internal register access. When the host accesses the data register the PHI module reads or writes the internal register selected by the indirect address register. Two other registers are provided for direct access. The FIFO register provides direct access to the VBI FIFO. The other direct access register is the status/interrupt register. This register contains the state of the interrupt sources.

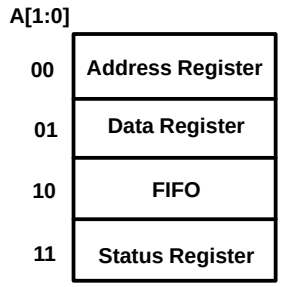


Figure 2–36. PHI Address Register Map

Normally, read or write operations require two accesses. To read the FIFO register, set A[1:0] to 2'b10, and perform a read cycle. The FIFO read data is placed on the D[7:0] bus. To read/write the status/interrupt register, set A[1:0] to 2'b11 and perform the read/write cycle. The read/write data is appropriately muxed to/from the external data bus.

Indirect register read/write

All PHI accesses except for the VBI FIFO and the status/interrupt register require a two-step operation. To access an indirect register, the desired internal address must first be written to the address register of the PHI. This is done by setting A[1:0] to 00 and performing a write cycle with D[7:0] = indirect register address. To write to an indirect register, the second step consists of writing the desired data to PHI address 01. To read an indirect register, the second step consists of reading the requested data from address 01.

Read Indirect Register

Step 1	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write register address	0	0	Register address							

Step 2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Read register data	0	1	Data from register							

Write Indirect Register

Step 1	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write register address	0	0	Register address							

Step 2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write register data	0	1	Data to register							

Latency

PHI accesses to indirect addresses 00-8F require special consideration due to response latencies of up to 64 μs for these addresses. Latency occurs between steps 1 and 2 for a read operation, and following step 2 for a write operation. To avoid violating PHI cycle time requirements the host can poll the cycle complete bit in the PHI status register following step 1 for a read or step 2 for a write. Alternatively, the cycle complete enable bit in the interrupt enable register (indirect address C1) can be set to generate an interrupt for the host when an access has been completed.

PHI accesses to indirect addresses 90-CF occur with minimal latency and interrupts are not generated for the completion of access cycles to these addresses.

VBI FIFO

The VBI FIFO containing sliced VBI data can be read directly by the PHI host.

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Read VBI FIFO	1	0	Data from FIFO							

Status/Interrupt Register

The status/interrupt register provides the host with information regarding the source of an interrupt. After an interrupt condition is set it can be reset by writing a 1 to the appropriate bit in the status/interrupt register. Section 2.14 contains a description of the PHI status/interrupt register.

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Access status/interrupt register	1	1	Data from status/interrupt register							

2.8.11 Parallel Host Interface Microcode Write Operation

A microcode write operation is required to down load microcode to the TVP5040 program RAM after power-up reset. During the write cycle, the internal microprocessors program counter resets and points to location zero in the program RAM and remains reset. Upon completion of the write operation, a microprocessor CLEAR-RESET operation is required. This is performed by writing into the 7F register to clear reset and resume the microprocessor function. (There is no specific data requirement to be written into the 7F register, any data will resume the microprocessor function.)

To avoid violating PHI cycle time requirements during a microcode write operation the host can poll the cycle complete bit in the PHI status register after writing each byte data to the PHI data register. Alternatively, the cycle complete enable bit in the interrupt enable register (indirect address C1) can be set to generate an interrupt for the host when a write has been completed.

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write microcode register address	0	0	0	1	1	1	1	1	1	0

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write microcode register data	0	1	First byte of microcode data (Wait for cycle complete status or interrupt.)							
Write microcode register data	0	1	Second byte of microcode data (Wait for cycle complete status or interrupt.)							
Write microcode register data	0	1	Last byte of microcode data (Wait for cycle complete status or interrupt.)							

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write clear-reset register address	0	0	0	1	1	1	1	1	1	1

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write clear-reset dummy data	0	1	Dummy data (Wait for cycle complete status or interrupt.)							

2.8.12 Parallel Host Interface Microcode Read Operation

The data read from indirect register 8E is read from the TVP5040 program RAM. During the read cycle, the internal microprocessors program counter resets and points to location zero in the program RAM and remains reset. Upon completion of the read operation, a microprocessor CLEAR-RESET operation is required. This is performed by writing into the 7F register to clear reset and resume the microprocessor function. (There is no specific data requirement to be written into the 7F register, any data will resume the microprocessor function.)

To avoid violating PHI cycle time requirements during a microcode read operation the host can poll the cycle complete bit in the PHI status register after writing to the PHI address register. Alternatively, the cycle complete enable bit in the interrupt enable register (indirect address C1) can be set to generate an interrupt for the host when the read data is available in the PHI data register.

Step 1	**A1**	**A0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Write program RAM read address	0	0	1	0	0	0	1	1	1	0
	(Wait for cycle complete status or interrupt)									

Step 2	**A1**	**A0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Read program RAM read data	0	1	data							

NOTE: Repeat Steps 1 and 2 until all program RAM data has been read.

Step 3	**A1**	**A0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Write clear-reset register address	0	0	0	1	1	1	1	1	1	1

Step 4	**A1**	**A0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Write clear-reset register data	0	1	Dummy data							
	(Wait for cycle complete status or interrupt)									

2.9 VBI Data Processor

The TVP5040 VBI data processor slices, parses, and performs error checking on teletext data contained in the vertical blanking interval or during active lines. Teletext formats supported are North American Basic Teletext Specification (NABTS) equivalent to ITU-R BT.653 system C, and World System Teletext (WST) equivalent to ITU-R BT.653 system B. Data is stored in an internal FIFO and may be read via the host port or transmitted as ancillary data in the digital video stream in BT.656 mode. The VBI data FIFO holds up to 14 lines of NABTS or 11 lines of WST data. Interrupts generated by the VBI data processor are configurable to enable host synchronization for retrieval of full-field teletext data.

Closed caption data may also be sliced by the VBI data processor and is stored in a register accessible via the host port.

2.9.1 Teletext Data Byte Order

The following table shows the order in which teletext data is read from the FIFO.

BYTE NUMBER	NABTS - 525 or 625 LINE SYSTEM	WST - 525 LINE SYSTEM	WST - 625 LINE SYSTEM
1	Video Line [7:0]	Video Line [7:0]	Video Line [7:0]
2	00, Hamming error, parity error, LPC error, match #2, match #1, video line [8]	00, Hamming error, parity error, 0, match #2, match #1, video line [8]	00, Hamming error, parity error, 0, match #2, match #1, video line [8]
3	Packet address 1	Magazine	Magazine
4	Packet address 2	Row address	Row address
5	Packet address 3	Data byte 1	Data byte 1
6	Continuity index	Data byte 2	Data byte 2
7	Packet structure	Data byte 3	Data byte 3
8	Data block 1	Data byte 4	Data byte 4
9	Data block 2	Data byte 5	Data byte 5
10	Data block 3	Data byte 6	Data byte 6
11	Data block 4	Data byte 7	Data byte 7
12	Data block 5	Data byte 8	Data byte 8
13	Data block 6	Data byte 9	Data byte 9
14	Data block 7	Data byte 10	Data byte 10
15	Data block 8	Data byte 11	Data byte 11
16	Data block 9	Data byte 12	Data byte 12
17	Data block 10	Data byte 13	Data byte 13
18	Data block 11	Data byte 14	Data byte 14
19	Data block 12	Data byte 15	Data byte 15
20	Data block 13	Data byte 16	Data byte 16
21	Data block 14	Data byte 17	Data byte 17
22	Data block 15	Data byte 18	Data byte 18
23	Data block 16	Data byte 19	Data byte 19
24	Data block 17	Data byte 20	Data byte 20
25	Data block 18	Data byte 21	Data byte 21
26	Data block 19	Data byte 22	Data byte 22
27	Data block 20	Data byte 23	Data byte 23
28	Data block 21	Data byte 24	Data byte 24
29	Data block 22	Data byte 25	Data byte 25
30	Data block 23	Data byte 26	Data byte 26
31	Data block 24	Data byte 27	Data byte 27
32	Data block 25	Data byte 28	Data byte 28
33	Data block 26	Data byte 29	Data byte 29
34	Data block 27/suffix	Data byte 30	Data byte 30
35	Data block 28/suffix	Data byte 31	Data byte 31
36	Padding byte†	Data byte 32	Data byte 32
37			Data byte 33
38			Data byte 34
39			Data byte 35
40			Data byte 36
41			Data byte 37
42			Data byte 38
43			Data byte 39
44			Data byte 40

† The padding byte is used to ensure an even number of writes. This byte does not contain any useful information. The read pointer automatically advances past this byte so the user does not have to read the padding byte.

2.9.2 Teletext as Ancillary Data in Video Stream

Sliced teletext data can be output as ancillary data in the video stream in ITU-R BT.656 mode. Teletext data is output on the Y7:0 terminals during the horizontal blanking period following the line from which the data was retrieved. Dummy ancillary data blocks with special timing header information are inserted during certain horizontal blanking periods to provide data synchronization information. Table 2–10 and Table 2–11 show the format and sequence of the ancillary data inserted into the video stream.

Table 2–10. NABTS 525/625-Line Ancillary Data Sequence

BYTE NO.	MSB 7	6	5	4	3	2	1	LSB 0	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data preamble
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	1	0	DID2	DID1	DID0	Data ID
5	1	0	0	0	0	0	0	0	Secondary data ID
6	1	0	0	0	1	0	0	1	Number of 32-bit data words
7	Video line number 7:0								Internal data ID
8	0	0	Hamming error	Parity error	LPC error	Match #2	Match #1	Video line 8	
9	Packet address 1								Data byte
10	Packet address 2								Data byte
11	Packet address 3								Data byte
12	Continuity index								Data byte
13	Packet structure								Data byte
14	Teletext data 1								Data byte
15	Teletext data 2								Data byte
39	Teletext data 26								Data byte
40	Teletext data 27/suffix								Data byte
41	Teletext data 28/suffix								Data byte
42	NEP	EP	Checksum						Checksum
43	1	0	0	0	0	0	0	0	Fill byte
44	1	0	0	0	0	0	0	0	Fill byte

Table 2–11. Dummy Timing Ancillary Data Sequence

BYTE NO.	MSB 7	6	5	4	3	2	1	LSB 0	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data preamble
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	1	0	DID2	DID1	DID0	Data ID
5	1	0	0	0	0	0	0	0	Secondary data ID
6	1	0	0	0	0	0	0	0	Number of 32-bit data words

In the tables above, EP is even parity on the lower 6 bits and NEP is negated even parity. The checksum for teletext data blocks is the 6 LSBs of the sum of the data bytes. The data ID byte provides timing information. Table 2–12 shows the possible values of the data ID byte and their meanings.

Table 2–12. Ancillary Data ID

DATA ID	EVENT IN SOURCE STREAM	DATA TYPE
50	Start of first, odd field	Dummy timing block
91	Sliced data of lines 1-23 of first field	VBI data
92	End of nominal VBI of first field, line 23	Dummy timing block
53	Sliced data of line 24 to end of first field	Full field teletext data
94	Start of second, even field	Dummy timing block
55	Sliced data of lines 1-23 of second field	VBI data
56	End of nominal VBI of second field, line 23	Dummy timing block
97	Sliced data of line 24 to end of second field	Full field teletext data

A dummy timing block is inserted into the video stream during the horizontal blanking period following line 23 of each field. If teletext data is available from line 23 it is inserted into the video stream prior to the dummy timing block.

2.10 Raw Video Data Output

The TVP5040 can output raw A/D samples in the ITU-656 VBI video stream if desired in order to process VBI data externally. The data occurs at 2x pixel rate. The data is preceded by a preamble sequence of 00, FF, FF, 60. The preamble sequence occurs immediately following the start of active video (SAV) sequence.

2.11 Reset and Initialization

Reset is initiated at power up or any time the RSTINB terminal is brought low. Table 2–13 describes the status of the TVP5040s terminals during and immediately after reset. Following a power-up reset, the host must download microcode to the TVP5040s program memory for use by the internal microprocessor.

Table 2–13. Reset Sequence

SIGNAL NAMES	DURING RESET	RESET COMPLETED
Y[9:0], UV[9:0], HSYN, VSYN, FID, PALI	Input	High-impedance if AVID is pulled down during reset. Active output if AVID is pulled up during reset.
AVID	Input	High-impedance if AVID is pulled down during reset. Active output if AVID is pulled up during reset.
SCLK, PCLK	High-impedance if PREF is pulled down during reset. Active if PREF is pulled up during reset.	Active output
PREF	Input	Active output
GLCO	Input	Active
VC0 in VIP mode	Output low	High impedance
VC0 in non VIP mode	High impedance	High impedance
D[7:0]	Input	High impedance
A[1:0] in PHI mode	Input	Input
RSTINB, SDA, SCL, I2CA, OEB, GPCL	Input	Input

2.12 Internal Control Registers

The TVP5040 is initialized and controlled by a set of internal registers which set all the device operating parameters. Communication between the external controller and TVP5040 is through a standard host port interface. Table 2–14 shows the summary of these registers. The reserved bits must be written with 0. The detailed programming information of each register is described in the following sections.

NOTE:

In general, the registers residing in the address space 00 through 8F for the I^2C and PHI host interface modes, and 0100 through 018F for the VIP host interface mode can be accessed only after the microcode has been down loaded to TVP5040s internal program RAM and a CLEAR-RESET operation has been issued to the internal microprocessor. The only exceptions are the registers involved in the microcode down load, read back, and CLEAR-RESET operations. These registers are at addresses 7E, 8E, and 7F respectively for the I^2C and PHI host interface modes and at 017F (CLEAR-RESET operation only) for the VIP host interface mode. (Note that for the VIP host interface mode the program RAM write and read FIFOs are mapped to addresses 1500 and 1600 respectively.)

Table 2–14. Registers Summary

REGISTER FUNCTION	VIP	PHI	I^2C	R/W
VIP vendor ID	0000 - 0001	NA	NA	R
VIP device ID	0002 - 0003	NA	NA	R
VIP subsystem vendor ID	0004 - 0005	NA	NA	R/W
VIP subsystem Device ID	0006 - 0007	NA	NA	R/W
VIP power state	0008	NA	NA	R/W
Reserved	0009	NA	NA	R/W
VIP power support	000A	NA	NA	R
Reserved	000B	NA	NA	R
VIP revision ID	000C - 000D	NA	NA	R
Reserved	000E - 00FF	NA	NA	R
Video input source selection 1	0100	00 ← 00	00	R†/W
Analog channel controls	0101	00 ← 01	01	R†/W
Operation mode controls	0102	00 ← 02	02	R†/W
Miscellaneous controls	0103	00 ← 03	03	R†/W
Reserved	0104	00← 04	04	R†/W
Software reset	0105	00 ← 05	05	R†/W
Color killer threshold control	0106	00 ← 06	06	R†/W
Luminance processing control 1	0107	00 ← 07	07	R†/W
Luminance processing control 2	0108	00 ← 08	08	R†/W
Brightness control	0109	00 ← 09	09	R†/W
Color saturation control	010A	00 ← 0A	0A	R†/W
Color hue control	010B	00 ← 0B	0B	R†/W
Contrast control	010C	00 ← 0C	0C	R†/W
Outputs and data rate select	010D	00 ← 0D	0D	R†/W
Luminance processing control 3	010E	00 ← 0E	0E	R†/W
Reserved	010F - 0115	00 ← 0F-15	0F-15	R†/W
Horizontal sync HSYN start NTSC/PAL	0116	00 ← 16	16	R†/W
Reserved	0117	00 ← 17	17	R†/W
Vertical blanking start	0118	00 ← 18	18	R†/W
Vertical blanking stop	0119	00 ← 19	19	R†/W
Chroma processing control 1	011A	00 ← 1A	1A	R†/W
Chroma processing control 2	011B	00 ← 1B	1B	R†/W
Interrupt reset B	011C	00←1C	1C	R†/W
Interrupt enable B	011D	00←1D	1D	R†/W
Interrupt configuration B	011E	00←1E	1E	R†/W
Reserved	011F	00 ← 1F	1F	R†/W
Video input source selection 2	0120	00 ← 20	20	R†/W
Reserved	0121–0124	00 ← 21-24	21-24	
Lock speed select	0125	00 ← 25	25	R†/W

NOTE: R = Read only for all interfaces
W = Write only for all interfaces
R/W = Read and write for all host interfaces (where applicable)
R†/W = Read and write for I2C and VIP host interfaces. Write only for PHI host interfaces.

Table 2–14. Registers Summary (Continued)

REGISTER FUNCTION	VIP	PHI	I²C	R/W
Crystal frequency	0126	00 ← 26	26	R†/W
Reserved	0127	00 ← 27	27	
Video standard	0128	00 ← 28	28	R†/W
Reserved	0129 – 017D	00 ← 29-7D	29-7D	
Reserved	017E	N/A	N/A	
NonVIP program RAM write	N/A	00 ← 7E	7E	W
Microprocessor reset clear	017F	00 ← 7F	7F	W
Major software revision	0180	00 ← 80	80	R
Status 1	0181	00 ← 81	81	R
Status 2	0182	00 ← 82	82	R
Status 3	0183	00 ← 83	83	R
Status 4	0184	00 ← 84	84	R
Interrupt status B	0185	00 ← 85	85	R
Interrupt B active	0186	00 ← 86	86	R
Minor software revision	0187	00 ← 87	87	R
Status 5	0188	00 ← 88	88	R
Vertical line count MSB	0189	00 ← 89	89	R
Vertical line count LSB	018A	00 ← 8A	8A	R
Analog die ID	018B	00 ← 8B	8B	R†/W
Digital die ID	018C	00 ← 8C	8C	R†/W
Reserved	018D	00 ← 8D	8D	
Reserved	018E	N/A	N/A	
NonVIP program RAM read	N/A	00 ← 8E	8E	R
Reserved	018F	00 ← 8F	8F	
TXF filter 1 parameters	0190 - 0194	00 ← 90 - 94	90 - 94	R/W
TXF filter 2 parameters	0195 - 0199	00 ← 95 - 99	95 - 99	R/W
TXF error filtering enable	019A	00 ← 9A	9A	R/W
TXF transaction processing enables	019B	00 ← 9B	9B	R/W
Reserved	019C - 019F	00 ← 9C-9F	9C-9F	
TTX control register	01A0	00 ← A0	A0	R/W
Line enable register A	01A1	00 ← A1	A1	R/W
Line enable register B	01A2	00 ← A2	A2	R/W
Custom sync pattern	01A3	00 ← A3	A3	R/W
Reserved	01A4 – 01AF	00 ← A4 - AF	A4 - AF	
Reserved	01B0	N/A	N/A	
NonVIP teletext FIFO	N/A	00 ← B0	B0	R
Reserved	01B1	00 ← B1	B1	
CC data	01B2	00 ← B2	B2	R
Buffer status A	01B3	00 ← B3	B3	R
Interrupt threshold	01B4	00 ← B4	B4	R/W
Interrupt line number	01B5	00 ← B5	B5	R/W
FIFO control	01B6	00 ← B6	B6	R/W
FIFO RAM test	01B7	00 ← B7	B7	R/W

NOTE: R = Read only for all interfaces
W = Write only for all interfaces
R/W = Read and write for all host interfaces (where applicable)
R†/W = Read and write for I2C and VIP host interfaces. Write only for PHI host interfaces.

Table 2–14. Registers Summary (Continued)

REGISTER FUNCTION	VIP	PHI	I²C	R/W
Reserved	01B8 - 01BF	00 ← B8 - BF	B8 - BF	
Interrupt status register A	01C0	00 ← C0	C0	R/W
Interrupt enable A	01C1	00 ← C1	C1	R/W
Interrupt configuration A	01C2	00 ← C2	C2	R/W
Reserved	01C3 – 01FF	00 ← C3 - FF	C3 - FF	
No-latency read access 1	02xx	NA	NA	R
No-latency read access 2	03xx	NA	NA	R
VIP status 0	1000	N/A	N/A	R
VIP status 1	1100	N/A	N/A	R
Reserved	1200 – 1300	N/A	N/A	
VIP teletext FIFO	1400	N/A	N/A	R/W
VIP program RAM write FIFO	1500	N/A	N/A	W
VIP program RAM read FIFO	1600	N/A	N/A	R
Reserved	1700- 1F00	N/A	N/A	R/W
PHI teletext FIFO	N/A	10b	N/A	R
PHI status/interrupt A	N/A	11b	N/A	R/W

NOTE: R = Read only for all interfaces
W = Write only for all interfaces
R/W = Read and write for all host interfaces (where applicable)
R†/W = Read and write for I2C and VIP host interfaces. Write only for PHI host interfaces.

2.13 Register Definitions

2.13.1 VIP Vendor ID

VIP address	000 - 001h
PHI address	NA
I²C address	NA

Address	7	6	5	4	3	2	1	0
000	0	1	0	0	1	1	0	0
001	0	0	0	1	0	0	0	0

This field identifies the manufacturer of the device. Address 001 is the MSB. This field is a constant of 104C.

2.13.2 VIP Device ID

VIP address	002 - 003h
PHI address	NA
I²C address	NA

Address	7	6	5	4	3	2	1	0
002	0	1	0	0	0	0	0	0
003	0	1	0	1	0	0	0	1

This field identifies the particular device. Address 003 is the MSB. This field is a constant of 5140H.

2.13.3 VIP Subsystem Vendor ID

VIP address	004 - 005h
PHI address	NA
I^2C address	NA

Address	7	6	5	4	3	2	1	0
004	Loaded from UV [7:0] pins on powerup reset							
005	Loaded from Y [7:0] pins on powerup reset							

This field identifies the subsystem manufacturer (for example, the board manufacturer). Address 005 is the MSB. The values of this field are set at the device power up or reset by sampling the state of Y[7:0] and UV[7:0] terminals. The Y[7:0] and UV[7:0] terminals may be tied to pullup or pulldown resisters to determine a fixed value for the subsystem vendor ID.

The default can be overwritten by writing a different value to the register as the first access to this register after reset. This register is read-only after the first write or read.

2.13.4 VIP Subsystem Device ID

VIP address	006 - 007h
PHI address	NA
I^2C address	NA

Address	7	6	5	4	3	2	1	0
006	Loaded from D [7:0] pins on powerup reset							
007	Loaded from A[1:0], VSYN, HSYN, Y[9:8], and UV[9:8] pins on powerup reset.							

This field identifies the subsystem device. Address 007 is the MSB. This field is one time writeable, similar to the subsystem vendor ID.

2.13.5 VIP Power State

VIP address	008h
PHI address	NA
I_2C address	NA

7	6	5	4	3	2	1	0
0	0	0	0	0	0	Power state	

This register is both readable and writable. When read, this register indicates the current power state of TVP5040. Bit 0 and bit 1 define four possible power states.

0 0 = P0 state. Fully on. This is the normal operation mode. (default)

0 1 = P1 state. Not supported

1 0 = P2 state. Not supported.

1 1 = P3. A/D converters are turned off and the internal clock is reduced to minimum. Power may or may not be removed.

Writing to these two bits forces TVP5040 to one of the four power states as defined above.

2.13.6 VIP Power Support

VIP address	00Ah
PHI address	NA
I2C address	NA

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bit 0 and 1 of this read-only register defines the power states that TVP5040 supports. 00 indicates TVP5040 does not support the optional P1 or P2 state as defined by VIP 1.1 specification.

2.13.7 VIP Revision ID

VIP address	00C – 00Dh
PHI address	NA
I2C address	NA

Address	7	6	5	4	3	2	1	0
00C	0	0	0	0	0	0	0	1
00D	0	0	0	0	0	0	0	1

This identifies the device hardware revision. Address 00D is the MSB. This field is a constant of 0101.

2.13.8 Video Input Source Selection 1

VIP address	100h
PHI address	00h
I2C address	00h

7	6	5	4	3	2	1	0
Reserved						Channel 1 source selection	Channel 2 source selection

Channel 1 source selection:
0 = VI1A selected (default)
1 = VI1B selected

Channel 2 source selection:
0 = VI2A selected (default)
1 = VI2B selected

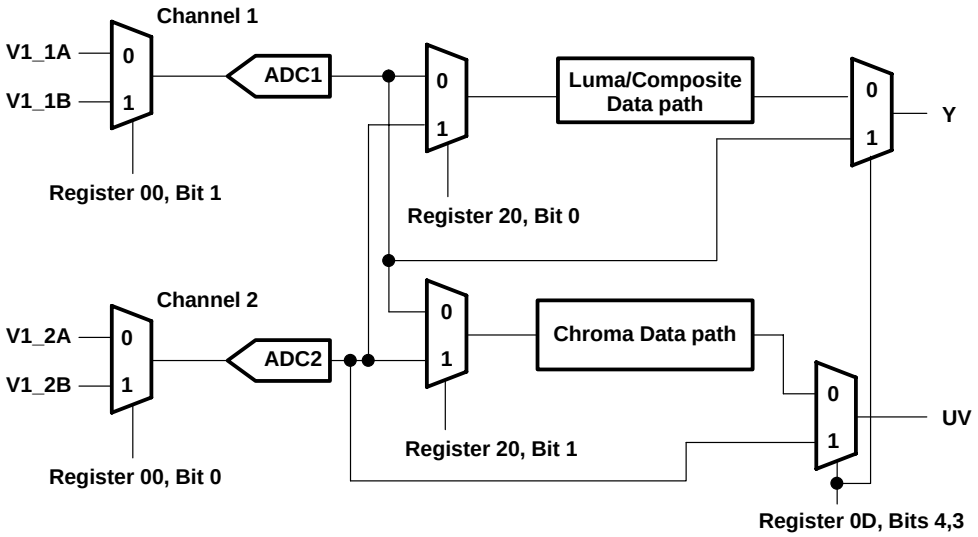


Figure 2–37. Video Input Source Selection

Table 2–15. Analog Channel and Video Mode Selection

	INPUT(S) SELECTED	ADDRESS 00		ADDRESS 20	
		BIT 1	BIT 0	BIT 1	BIT 0
Composite	1A	0	x	0	0
	1B	1	x	0	0
	2A	x	0	1	1
	2B	x	1	1	1
S-video	1A luma, 2A chroma	0	0	1	0
	1A luma, 2B chroma	0	1	1	0
	1B luma, 2A chroma	1	0	1	0
	1B luma, 2B chroma	1	1	1	0
	2A luma, 1A chroma	0	0	0	1
	2A luma, 1B chroma	1	0	0	1
	2B luma, 1A chroma	0	1	0	1
	2B luma, 1B chroma	1	1	0	1

2.13.9 Analog Channel Controls

VIP address	101h
PHI address	01h
I^2C address	01h

7	6	5	4	3	2	1	0
Reserved		Automatic offset control, channel 2		Automatic offset control, channel 1		Automatic gain control	

Automatic offset control, channel 2:

00 = Automatic offset control disabled
01 = Automatic offset control enabled (default)
10 = Reserved
11 = Offset control frozen

Automatic offset control, channel 1:

00 = Automatic offset control disabled
01 = Automatic offset control enabled (default)
10 = Reserved
11 = Offset control frozen

Automatic gain control:

00 = Disabled (fixed gain value)
01 = AGC enabled using luma input as the reference (default)
10 = Reserved
11 = AGC frozen

2.13.10 Operation Mode Controls

VIP address	102h
PHI address	02h
I^2C address	02h

7	6	5	4	3	2	1	0
Reserved	Reserved	TV/VCR mode		Reserved	Color subcarrier DTO frozen	Reserved	Powerdown mode

TV/VCR mode:

00 = Automatic, mode determined by the internal detection circuit (default)
01 = Reserved
10 = VCR (nonstandard video) mode
11 = TV (standard video) mode

With automatic detection enabled, unstable or nonstandard syncs on input video will force the device into VCR mode. This turns off the luminance and chrominance comb filters and turns on the chroma trap filter.

TV/VCR MODE	ACE	CE	CM[2:0]	LE	CF	LF	STANDARD	NOTE
00	0/1 0/1	0/1 1/1	XXX/000 1XX/000	1/0 1/0	10/00 01/00	11/00 11/00	NTSC PAL	Autodetection and switching between VCR/TV
01	X	X	XXX	X	XX	XX		Manual programming
10	0 0	0 1	XXX 1XX	1 1	10 01	11 11	NTSC PAL	VCR mode
11	1 1	1 1	000 000	0 0	00 00	00 00	NTSC PAL	TV mode

ACE = Adaptive comb filter enable. Chrominance control register 1A, bit 3
CE = Chrominance comb filter enable. Chrominance control register 1A, bit 2
CM[2:0] = Chrominance comb filter mode. Chrominance control register 1A, bit 7-5.
LE = Luminance filter select. Luminance processing control #2 Register 08, bit 6
CF = Chrominance filter select. Chrominance control #2 register 1B, bit 1 and 0.
LF = Luminance filter select. Luminance control #3 register 0E, bit 1 and 0.
X = No change

Color subcarrier DTO frozen:

0 = Color subcarrier DTO increments by the internally-generated phase increment. (default)
GLCO terminal outputs the phase increment.
1 = Color subcarrier DTO forced to nominal value

Powerdown mode:

0 = Normal operation (default)
1 = Power-down mode. A/Ds are turned off and internal clocks are reduced to minimum.

2.13.11 Miscellaneous Control

VIP address	103h
PHI address	03h
I^2C address	03h

7	6	5	4	3	2	1	0
GPCL terminal function select		PALI terminal and FID terminal function select	Y U/V output enable	HSYN, VSYN, AVID, FID, PALI output enable	Reserved	Vertical blanking on/off	Clock output enable

GPCL terminal function select:

00 = GPCL is logic 0 output (default)
01 = GPCL is logic 1 output
10 = GPCL is vertical blank output
11 = GPCL is external sync lock control input

When GPCL is configured as a vertical blank output, the vertical blanking on/off bit is used to activate the output. When GPCL is configured as a sync lock control, it can be used to force the internal PLLs to their normal settings. This causes all clocks and synchronization signals to assume nominal values. The sync lock control input is active high.

PALI terminal and FID terminal function select:

0 = PALI outputs PAL indicator signal and terminal FID outputs field ID signal (default)
1 = PALI outputs horizontal lock indicator (HLK) and terminal FID outputs vertical lock indicator (VLK)

Y U/V output enable:

0 = Y U/V high impedance (default)
1 = Y U/V active

Horizontal sync (HSYN), vertical sync (VSYN), active video indicator (AVID), PALI, and FID output enables:

0 = HSYN, VSYN, AVID, PALI, and FID are high impedance
1 = HSYN, VSYN, AVID, PALI, and FID are active

This bit is default to 0 after reset if the AVID terminal is pulled down during reset or default to 1 if the AVID terminal is pulled up during reset.

Vertical blanking on/off control:

0 = Vertical blanking off (default)
1 = Vertical blanking on

Clock enable:

0 = SCLK and PCLK outputs are high impedance
1 = SCLK and PCLK outputs are enabled

This bit is default to 0 after reset if the PREF terminal is pulled down during reset or default to 1 if the AVID is pulled up during reset.

Table 2–16. Digital Output Control

OEB PIN	AVID PIN	REG 03, BIT 4 (TVPOE)	REG C2, BIT 2 (VDPOE)	YUV OUTPUT	NOTES
1	X	X	X	High impedance	At all times
0	1 during reset	X	X	Active after reset	After reset and before YUV output enable bits are programmed. TVPOE bit defaults to 1 and VDPOE bit defaults to 1.
0	0 during reset	X	X	High impedance after reset	After reset and before YUV output enable bits are programmed. TVPOE bit defaults to 0 and VDPOE bit defaults to 1.
0	X	0	X	High impedance	After both YUV output enable bits are programmed
0	X	X	0	High impedance	After both YUV output enable bits are programmed
0	X	1	1	Active	After both YUV output enable bits are programmed

2.13.12 Software Reset

VIP address	105h
PHI address	05h
I2C address	05h

7	6	5	4	3	2	1	0
Reserved							Software reset

Software reset:

0 = No software reset (default)
1 = Software reset of the device

The software reset applies only to the microcode internal variables.

2.13.13 Color Killer Threshold Control

VIP address	106h
PHI address	06h
I2C address	06h

7	6	5	4	3	2	1	0
Reserved	Automatic color killer		Color killer threshold				

Automatic color killer:

00 = Automatic mode (default)
01 = Reserved
10 = Color killer enabled. The UV terminals are forced to a zero color state.
11 = Color killer disabled

Color killer threshold (ref. 0 dB = nominal burst amplitude):

11111 = –30 dB
10000 = –24 dB (default)
00000 = –18 dB

2.13.14 Luminance Processing Control 1

VIP address	107h
PHI address	07h
I2C address	07h

7	6	5	4	3	2	1	0
Luma bypass mode	Pedestal not present	Reserved	Luma bypass during vertical blank	Luminance signal delay with respect to chrominance signal			

Luma bypass mode select:

0 = Input video bypasses the chroma trap and comb filters. Chroma outputs are forced to zero. (default)
1 = Input video bypasses the whole luma processing.
Raw A/D data is output alternatively as UV data and Y data at SCLK rate. The output data is properly clipped to comply to CCIR601 coding range. Only valid for 10-bit YUV output format (YUV output format = 100 or 111 at register 0D)

Pedestal not present:

0 = 7.5 IRE pedestal is present on the analog video input signal (default)
1 = Pedestal is not present on the analog video input signal

Luminance bypass mode during vertical blanking:

0 = No (default)
1 = Yes

When the luminance bypass is enabled, the luminance comb and notch filters are turned off and the chrominance components of the output video are sent to a zero color state. Luminance bypass occurs for the duration of the vertical blanking as defined by register 18 and 19. This feature may be used to prevent distortion of test and data signals present during the vertical blanking interval.

Luma signal delay with respect to chroma signal in pixel clock increments (range –8 to 7 pixel clocks):

1111 = –8 pixel clocks delay
1011 = –4 pixel clocks delay
1000 = –1 pixel clocks delay
0000 = 0 pixel clocks delay (default)
0011 = 3 pixel clocks delay
0111 = 7 pixel clocks delay

2.13.15 Luminance Processing Control 2

VIP address	108h
PHI address	08h
I^2C address	08h

7	6	5	4	3	2	1	0
Reserved	Luminance filter select	Reserved		Peaking gain		Reserved	

Luminance filter select:

0 = Luminance comb filter enabled (default)
1 = Luminance chroma trap filter enabled

Peaking gain:

00 = Peaking disabled (default)
01 = 3 dB
10 = 6 dB
11 = 12 dB

Peaking frequency:

Square-pixel sampling rate:

NTSC	PAL	PAL M	PAL (Combination-N)
2.4 MHz	2.9 MHz	2.4 MHz	2.9 MHz

ITU-R BT.601 sampling rate:

All standards
2.6 MHz Refer to Figures 2–16, 2–17 and 2–18.

2.13.16 Brightness Control

VIP address	109h
PHI address	09h
I2C address	09h

7	6	5	4	3	2	1	0
Brightness control							

Brightness:

1 1 1 1 1 1 1 1 = 255 (bright)
1 0 0 0 1 0 1 1 = 139 (ITU-R BT.601 level)
1 0 0 0 0 0 0 0 = 128 (default)
0 0 0 0 0 0 0 0 = 0 (dark)

2.13.17 Color Saturation Control

VIP address	10Ah
PHI address	0Ah
I2C address	0Ah

7	6	5	4	3	2	1	0
Saturation control							

Saturation:

1 1 1 1 1 1 1 1 = 255 (maximum)
1 0 0 0 0 0 0 0 = 128 (default)
0 0 0 0 0 0 0 0 = 0 (no color)

2.13.18 Hue Control

VIP address	10Bh
PHI address	0Bh
I2C address	0Bh

7	6	5	4	3	2	1	0
Hue control							

Hue:

0 1 1 1 1 1 1 1 = 180 degrees
0 0 0 0 0 0 0 0 = 0 degrees (default)
1 0 0 0 0 0 0 0 = –180 degrees

2.13.19 Contrast Control

VIP address	10Ch
PHI address	0Ch
I2C address	0Ch

7	6	5	4	3	2	1	0
Contrast control							

Contrast:

1 1 1 1 1 1 1 1 = 255 (maximum contrast)
1 0 0 0 0 0 0 0 = 128 (default)
0 0 0 0 0 0 0 0 = 0 (minimum contrast)

2.13.20 Outputs and Data Rates Select

VIP address	10Dh
PHI address	0Dh
I^2C address	0Dh

7	6	5	4	3	2	1	0
Sampling rate	YUV output code range	UV code format	YUV data path bypass		YUV output format		

Sampling rate:

0 = ITU-R BT.601 sampling rate
1 = Square pixel sampling rate
(This bit only applies when the video standard autoswitch microcode is running)

YUV output code range:

0 = ITU-R BT.601 coding range (Y ranges from 16 to 235. Cr and Cb range from 16 to 240)
1 = Extended coding range (Y, Cr and Cb range form 1 to 254) (default)

UV code format:

0 = Offset binary code (2s complement + 128) (default)
1 = Straight binary code (2s complement)

YUV data path bypass:

00 = Normal operation. (default)
01 = YUV output pins connected to decimation filter output, decoder function bypassed. Both Y and UV busses output data at PCLK rate.
10 = YUV output pins connected to A/D output, decoder function bypassed, for raw video data output. Both Y and UV busses output data at SCLK rate.
11 = Reserved

YUV output format:

000 = 20-bit 4:2:2 YUV (default)
001 = Reserved
010 = Reserved
011 = Reserved
100 = 10-bit 4:2:2 UYVYUYVY
101 = Reserved
110 = Reserved
111 = 10-Bit ITU-R BT. 656 interface

2.13.21 Luminance Control 3

VIP address	10Eh
PHI address	0Eh
I2C address	0Eh

7	6	5	4	3	2	1	0
Reserved						Luminance filter select	

Luminance filter stopband bandwidth (MHz):

	NTSC CCIR601	NTSC Square pixel	PAL CCIR601	PAL Square pixel
00 =	1.2129	1.1026	1.2129	1.3252
01 =	0.8701	0.7910	0.8701	0.9507
10 =	0.7383	0.6712	0.7383	0.8066
11 =	0.5010	0.4554	0.5010	0.5474

Luminance filter select[1:0] selects one of the four chroma trap filters to produce luminance signal by removing the chrominance signal from the composite video signal. The stop band of the chroma trap filter is centered at the chroma subcarrier frequency with stopband bandwidth controlled by the two control bits. Refer to Figure 2–12, 2-13, and 2-14 for the frequency responses of the filters. The control 00 is a default mode.

2.13.22 Horizontal Sync HSYN Start NTSC/PAL

VIP address	116h
PHI address	16h
I2C address	16h

7	6	5	4	3	2	1	0
HSYN start							

HSYN Start:

1 1 1 1 1 1 1 1 = –127 × 4 pixel clocks
1 1 1 1 1 1 1 0 = –126 × 4 pixel clocks
1 1 1 1 1 1 0 1 = –125 × 4 pixel clocks
1 0 0 0 0 0 0 0 = 0 pixel clocks (defaults)
0 1 1 1 1 1 1 1 = 1 × 4 pixel clocks
0 1 1 1 1 1 1 0 = 2 × 4 pixel clocks
0 0 0 0 0 0 0 0 = 128 × 4 pixel clocks

2.13.23 Vertical Blanking VBLK Start

VIP address	118h
PHI address	18h
I^2C address	18h

7	6	5	4	3	2	1	0
VBLK start							

VBLK start:

0 1 1 1 1 1 1 1 = 127 lines after start of vertical blanking interval
0 0 0 0 0 0 0 1= 1 line after start of vertical blanking interval
0 0 0 0 0 0 0 0 = same time as start of vertical blanking interval (default)
1 1 1 1 1 1 1 1 = 1 line before start of vertical blanking interval
1 0 0 0 0 0 0 0 = 128 lines before start of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals as shown in Table 2–17. The setting in this register determines the timing of the GPCL signal when it is configured to output vertical blank(see register 03). The setting in this register is also used to determine the duration of the luma bypass function (see register 07).

Table 2–17. Vertical Blanking Interval Start and End

STANDARD	FIELD	START LINE NUMBER	END LINE NUMBER
NTSC	odd	1	21
	even	263.5	284.5
PAL	odd	623.5	23.5
	even	311	335
MPAL	odd	523	21
	even	260.5	284.5
PAL (Combination-N)	odd	623.5	23.5
	even	311	335

2.13.24 Vertical Blanking VBLK Stop

VIP address	119h
PHI address	19h
I^2C address	19h

7	6	5	4	3	2	1	0
VBLK end							

VBLK End:

0 1 1 1 1 1 1 1 = 127 lines after end of vertical blanking interval
0 0 0 0 0 0 0 1= 1 line after end of vertical blanking interval
0 0 0 0 0 0 0 0 = same time as end of vertical blanking interval (default)
1 1 1 1 1 1 1 1 = 1 line before end of vertical blanking interval
1 0 0 0 0 0 0 0 = 128 lines before end of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals as shown in Table 2–17. The setting in this register determines the timing of the GPCL signal when it is configured to output vertical blank(see register 03). The setting in this register is also used to determine the duration of the luma bypass function (see register 07).

2.13.25 Chrominance Control 1

VIP address	11Ah
PHI address	1Ah
I^2C address	1Ah

7	6	5	4	3	2	1	0
Chrominance comb filter mode [2:0] (CM[2:0])			Color DTO reset	Chrominance adaptive comb filter enable (ACE)	Chrominance comb filter enable (CE)	Automatic color gain control	

Table 2–18. Chrominance Comb Filter Selection

ACE	CE	CM[2]	CM[1]	CM[0]	COMB FILTER SELECTION
0	0	X	X	X	Comb filter disabled
0	1	0	0	X	Fixed 3-line comb filter with (1/4, 1/2, 1/4) coefficients
0	1	0	1	X	Fixed 3-line comb filter with (1, 0, 1) coefficients
0	1	1	X	X	Fixed 2-line comb filter
1	X	X	0	0	Adaptive between 3-line (1/4,1/2,1/4) comb filter and 2-line comb filter
1	X	X	0	1	Adaptive between 3-line (1/4,1/2,1/4) comb filter and no comb filter (default for NTSC-M and NTSC-443)
1	X	X	1	0	Adaptive between 3-line (1,0,1) comb filter and 2-line comb filter
1	X	X	1	1	Adaptive between 3-line (1,0,1) comb filter and no comb filter (default for PAL, M-PAL, combination-N PAL)

Color DTO reset:

0 = Color subcarrier DTO not reset. (default)
1 = Color subcarrier DTO reset

Color subcarrier DTO is reset to zero and the color subcarrier DTO bit then immediately returns to zero.

When this bit is set, the subcarrier DTO phase reset bit is transmitted on the GCLO terminal on the next occurrence of a specified line (NTSC or PAL).

Automatic color gain control:

00 = ACC enabled (default)

01 = Reserved

10 = ACC disabled

11 = ACC frozen

2.13.26 Chrominance Control 2

VIP address	11Bh
PHI address	1Bh
I2C address	1Bh

7	6	5	4	3	2	1	0
Reserved						Chrominance filter select	

Chrominance output bandwidth (MHz):

	NTSC CCIR601	NTSC Square Pixel	PAL CCIR601	PAL Square Pixel
00 =	1.2129	1.1026	1.2129	1.3252
01 =	0.8701	0.7910	0.8701	0.9507
10 =	0.7383	0.6712	0.7383	0.8066
11 =	0.5010	0.4554	0.5010	0.5474

Refer to Figures 2–6, 2-7, 2-8 and 2-9 for the frequency responses of the filters. The control 00 is default mode**.**

2.13.27 Interrupt Reset Register B

VIP address	11Ch
PHI address	1Ch
I2C address	1Ch

7	6	5	4	3	2	1	0
Software init reset	Macrovision detect changed reset	TVP command ready reset	Field rate changed reset	Line alternation changed reset	Color lock changed reset	H/V lock changed reset	TV/VCR changed reset

Software Init	0 = No effect on interrupt register B (default)	1 = Reset software init bit
Macrovision Detect Changed Reset	0 = No effect on interrupt register B (default)	1 = Reset Macrovision detect changed bit
TVP Command Ready Reset	0 = No effect on interrupt register B (default)	1 = Reset TVP command ready bit
Field Rate Changed Reset	0 = No effect on interrupt register B (default)	1 = Reset field rate changed bit
Line Alternation Changed Reset	0 = No effect on interrupt register B (default)	1 = Reset line alternation changed bit
Color Lock Changed Reset	0 = No effect on interrupt register B (default)	1 = Reset color lock changed bit
H/V Lock Changed Reset	0 = No effect on interrupt register B (default)	1 = Reset H/V lock changed bit
TV/VCR Changed Reset	0 = No effect on interrupt register B (default)	1 = Reset TV/VCR changed bit

The interrupt reset register B is used by the external processor to reset the interrupt status bits in the interrupt register B. Bits loaded with a 1 allows the corresponding interrupt status bit to reset to 0. Bits loaded with a 0 have no effect on the interrupt status bits.

2.13.28 Interrupt Enable Register B

VIP address	11Dh
PHI address	1Dh
I^2C address	1Dh

7	6	5	4	3	2	1	0
Software init occurred	Macrovision detect changed	TVP command ready	Field rate changed	Line alternation changed	Color lock changed	H/V lock changed	TV/VCR changed

Software init	0 = Software init interrupt source masked (default)	1 = Software init interrupt source enabled
Macrovision Detect Changed	0 = Macrovision detect interrupt source masked (default)	1 = Macrovision detect interrupt source enabled
TVP Command Ready	0 = TVP command interrupt source masked (default)	1 = TVP command interrupt source enabled
Field Rate Changed	0 = Field rate interrupt source masked (default)	1 = Field rate interrupt source enabled
Line Alternation Changed	0 = Line alternation interrupt source masked (default)	1 = Line alternation interrupt source enabled
Color Lock Changed	0 = Color lock interrupt source masked (default)	1 = Color lock interrupt source enabled
H/V Lock Changed	0 = H/V lock interrupt source masked (default)	1 = H/V lock interrupt source enabled
TV/VCR Changed	0 = TV/VCR interrupt source masked (default)	1 = TV/VCR interrupt source enabled

The interrupt enable register B is used by the external processor to mask unnecessary interrupt sources for interrupt B. Bits loaded with a 1 allows the corresponding interrupt condition to generate an interrupt on the external pin. Conversely bits loaded with a 0 masks the corresponding interrupt condition from generating an interrupt on the external pin. Note this register only affects the external terminal, it does not affect the bits in the interrupt status register. A given condition can set the appropriate bit in the status register and not cause an interrupt on the external pin. To determine if this device is driving the interrupt terminal, either perform a logical AND of the interrupt status register B with the interrupt enable register B or check the state of the interrupt B bit in the interrupt B active register.

2.13.29 Interrupt Configuration Register B

VIP address	11Eh
PHI address	1Eh
I^2C address	1Eh

7	6	5	4	3	2	1	0
Reserved							Interrupt polarity B

Interrupt Polarity	0 = Interrupt B is active low. 1 = Interrupt B is active high. (default)	Must be same as interrupt polarity A bit at bit 0 of interrupt configuration register A at address C2

The interrupt configuration register B is used to configure the polarity of interrupt B on the external interrupt terminal. Note that when the interrupt B is configured for active low, the terminal is driven low when active and 3-state when inactive (open-collector). Conversely, when the interrupt B is configured for active high, it is driven high for active and driven low for inactive.

2.13.30 Video Input Source Selection 2

VIP address	120h
PHI address	20h
I2C address	20h

7	6	5	4	3	2	1	0
Reserved	Reserved	Decimation filter bypass enable	Reserved	Reserved	Reserved	Chroma channel select	Luma/composite channel select

Decimation filter bypass:

0 = Bypass disabled (default)
1 = Bypass enabled

Chroma Channel Select:

0 = ADC1 selected (default)
1 = ADC2 selected

Luma/composite channel select:

0 = ADC1 selected (default)
1 = ADC2 selected

See also: Video input source selection 1 register, I2C address 00

2.13.31 Lock Speed Select

VIP address	125h
PHI address	25h
I2C address	25h

7	6	5	4	3	2	1	0
Reserved							Lock speed

Lock speed:

0 = Fast lock disabled (default)
1 = Fast lock enabled

2.13.32 Crystal Frequency

VIP address	126h
PHI address	26h
I2C address	26h

7	6	5	4	3	2	1	0
Reserved							Crystal frequency

Crystal frequency:

0 = 14.31818 MHz (default)
1 = 27 MHz

2.13.33 Video Standard

VIP address	128h
PHI address	28h
I2C address	28h

7	6	5	4	3	2	1	0
Reserved				Video Standard			

Video standard:

0000 = Autoswitch mode
0001 = (M) NTSC square pixel
0010 = (M) NTSC ITU-R BT.601
0011 = (B, G, H, I, N) PAL square pixel
0100 = (B, G, H, I, N) PAL ITU-R BT.601
0101 = (M) PAL square pixel
0110 = (M) PAL ITU-R BT.601
0111 = (Combination-N) PAL square pixel
1000 = (Combination-N) ITU-R BT.601
1001 = NTSC 4.43 square pixel
1010 = NTSC 4.43 ITU-R BT.601

With the autoswitch code running, the user can force the device to operate in a particular video standard mode and sampling rate by writing the appropriate value into this register.

2.13.34 NonVIP Program RAM Write

VIP address	N/A
PHI address	7Eh
I2C address	7Eh

7	6	5	4	3	2	1	0
Program RAM Write Data							

If the PHI or I2C host interface is enabled, the program RAM can be written via the nonVIP program RAM write register at address 7E. If the VIP host interface is enabled, the program RAM can be written via VIP FIFO B at location 5 in the VIP FIFO address space.

2.13.35 Microprocessor Reset Clear

VIP address	17Fh
PHI address	7Fh
I2C address	7Fh

7	6	5	4	3	2	1	0
Data							

A write with any data to this register must be performed to restart the internal microprocessor after the completion of the microcode download to the program RAM or after the microcode upload from the program RAM.

2.13.36 Major Software Revision Number

VIP address	180h
PHI address	80h
I^2C address	80h

7	6	5	4	3	2	1	0
Microcode major revision number							

This register contains the major software revision number for the microcode.

2.13.37 Status Register 1

VIP address	181h
PHI address	81h
I^2C address	81h

7	6	5	4	3	2	1	0
Peak white detect status	Line-alternating status	Field rate status	Lost lock detect status	Color subcarrier lock status	Vertical sync lock status	Horizontal sync lock status	TV/VCR status

Peak white detect status:

0 = Peak white is not detected.
1 = Peak white is detected.

Line-alternating status:

0 = Not line-alternating
1 = Line alternating

Field rate status:

0 = 60 Hz
1 = 50 Hz

Lost lock detect status:

0 = No lost lock since status register 1 was last read.
1 = Lost lock since status register 1 was last read.

Color subcarrier lock status:

0 = Color subcarrier is not locked.
1 = Color subcarrier is locked.

Vertical sync lock status:

0 = Vertical sync is not locked.
1 = Vertical sync is locked.

Horizontal sync lock status:

0 = Horizontal sync is not locked.
1 = Horizontal sync is locked.

TV/VCR status:

0 = TV
1 = VCR

2.13.38 Status Register 2

VIP address	182h
PHI address	82h
I2C address	82h

7	6	5	4	3	2	1	0
Reserved		PAL switch polarity	Field sequence status	AGC and offset status	Reserved	Macrovision detection	

PAL switch polarity of first line of odd field:

0 = PAL switch is zero (Color burst phase = 135 degree)
1 = PAL switch is one (Color burst phase = 225 degree)

Field sequence status:

0 = Even field
1 = Odd field

Automatic gain and offset status:

0 = Automatic gain and offset is not frozen.
1 = Automatic gain and offset is frozen.

Macrovision detection:

00 = No copy protection
01 = AGC pulses/pseudosyncs present
10 = AGC pulses/pseudosyncs present and 2-line color striping present
11 = AGC pulses/pseudosyncs present and 4-line color striping present

2.13.39 Status Register 3

VIP address	183h
PHI address	83h
I2C address	83h

7	6	5	4	3	2	1	0
AGC gain							

AGC gain (step size = 0.831%):

0 0 0 0 0 0 0 0 = –6 dB
0 1 0 0 0 0 0 0 = – 3 dB
1 0 0 0 0 0 0 0 = 0 dB
1 1 0 0 0 0 0 0 = 3 dB
1 1 1 1 1 1 1 1 = 6 dB

2.13.40 Status Register 4

VIP address	184h
PHI address	84h
I^2C address	84h

7	6	5	4	3	2	1	0
Subcarrier to horizontal (SCH) phase							

SCH (color DTO subcarrier phase at 50% of the falling edge of horizontal sync of line one of odd field; step size 360 deg/256):

0 0 0 0 0 0 0 0 = 0.00 degree
0 0 0 0 0 0 0 1 = 1.41 degree
0 0 0 0 0 0 1 0 = 2.81 degree
1 1 1 1 1 1 1 0 = 357.2 degree
1 1 1 1 1 1 1 1 = 358.6 degree

2.13.41 Interrupt Status Register B

VIP address	185h
PHI address	85h
I^2C address	85h

7	6	5	4	3	2	1	0
Software init	Macrovision detect changed	TVP command ready	Field rate changed	Line alternation changed	Color lock changed	H/V lock changed	TV/VCR changed

Software init	0 = Software init has not completed (default)	1 = Software init has completed
Macrovision detect changed	0 = Macrovision detect status has not changed (default)	1 = Macrovision detect status has changed.
TVP command ready	0 = TVP is not ready to accept a new command (default)	1 = TVP is ready to accept a new command
Field rate changed	0 = Field rate has not changed (default)	1 = Field rate has changed
Line alternation changed	0 = Line alternation has not changed (default)	1 = Line alternation has changed
Color lock changed	0 = Color lock status has not changed (default)	1 = Color lock status has changed
H/V lock changed	0 = H/V lock status has not changed (default)	1 = H/V lock status has changed
TV/VCR changed	0 = TV/VCR status has not changed (default)	1 = TV/VCR mode detect has changed

The interrupt status register B is polled by the external processor to determine the interrupt source for interrupt B. After an interrupt condition is set, it can be reset by writing to interrupt reset register B at subaddress ICh with a 1 in the appropriate bit.

2.13.42 Interrupt B Active Register

VIP address	186h
PHI address	86h
I^2C address	86h

7	6	5	4	3	2	1	0
0							Interrupt B

Interrupt B	0 = Interrupt B is not active.	1 = Interrupt B is active (default).

The interrupt status register is polled by the external processor to determine if interrupt B is active.

2.13.43 Minor Software Revision Number

VIP address	187h
PHI address	87h
I2C address	87h

7	6	5	4	3	2	1	0
Microcode minor revision number							

This register contains the minor revision number for the TVP5040 microcode. This is a number from 0 to 99.

2.13.44 Status Register 5

VIP address	188h
PHI address	88h
I2C address	88h

7	6	5	4	3	2	1	0
Autoswitch mode	Reserved	Reserved		Video Standard			Sampling Rate

This register contains information about the detected video standard and the sampling rate at which the device is currently operating. When autoswitch code is running, this register must be tested to determine which video standard has been detected.

Autoswitch mode:

0 = Stand-alone (forced video standard) mode
1 = Autoswitch mode

Video standard:

000 = (M) NTSC
001 = (B, G, H, I) PAL
010 = (M) PAL
011 = (Combination-N) PAL
100 = NTSC 4.43
101–111 = Reserved

Sampling rate:

0 = Squire pixel
1 = ITU–BT.601

2.13.45 Vertical Line Count MSB

VIP address	189h
PHI address	89h
I2C address	89h

7	6	5	4	3	2	1	0
Reserved						Vertical Line Count MSB	

Vertical line count MSB:

Vertical line count bits [9:8]

2.13.46 Vertical Line Count LSB

VIP address	18Ah
PHI address	8Ah
I2C address	8Ah

7	6	5	4	3	2	1	0
Vertical Line Count LSB							

Vertical line count LSB:

Vertical line count bits [7:0]

These registers 89h and 8Ah can be read and combined to extract the current vertical line count. This can be used with nonstandard video signals such as a VCR in fast-forward or rewind modes to synchronize downstream video circuitry.

2.13.47 Analog Die ID

VIP address	018Bh
PHI address	8Bh
I2C address	8Bh

7	6	5	4	3	2	1	0
Analog die ID							

This register identifies the analog die ID.

2.13.48 Digital Die ID

VIP address	018Ch
PHI address	8Ch
I2C address	8Ch

7	6	5	4	3	2	1	0
Digital die ID							

This register identifies the digital die ID.

2.13.49 NonVIP Program RAM Read

VIP address	N/A
PHI address	8Eh
I2C address	8Eh

7	6	5	4	3	2	1	0
Program RAM Read Data							

The program RAM can be read via the nonVIP program RAM read register at address 8E if PHI or I2C host interface is enabled or via VIP FIFO B at location 6 in VIP FIFO address space if VIP host interface is enabled.

2.13.50 TXF Filter 1 Parameters

VIP address	190h – 194h
PHI address	90h – 94h
I^2C address	90h – 94h

ADDRESS	7	6	5	4	3	2	1	0
90h	Filter 1 Mask_1[3:0]				Filter 1 Pattern_1[3:0]			
91h	Filter 1 Mask_2[3:0]				Filter 1 Pattern_2[3:0]			
92h	Filter 1 Mask_3[3:0]				Filter 1 Pattern_3[3:0]			
93h	Filter 1 Mask_4[3:0]				Filter 1 Pattern_4[3:0]			
94h	Filter 1 Mask_5[3:0]				Filter 1 Pattern_5[3:0]			

For an NABTS system, the packet prefix consists of five bytes: P1, P2, P3, CI and PS. Each byte contains four data bits interlaced with four Hamming protection bits.

Pattern_1[3:0] corresponds to P1[7], P1[5], P1[3], P1[1] (Packet Address)
Pattern_2[3:0] corresponds to P2[7], P2[5], P2[3], P2[1] (Packet Address)
Pattern_3[3:0] corresponds to P3[7], P3[5], P3[3], P3[1] (Packet Address)
Pattern_4[3:0] corresponds to CI[7], CI[5], CI[3], CI[1] (Continuity Index)
Pattern_5[3:0] corresponds to PS[7], PS[5], PS[3], PS[1] (Packet Structure)

For a WST system (PAL or NTSC), the magazine and row address group consists of two bytes. The two bytes contain three bits of magazine number (M[2:0]) and 5 bits of row address (R[4:0]), interlaced with eight Hamming protection bits.

Pattern_1[3:0] corresponds to R[0], M[2], M[1], M[0] (Magazine and row LSBit)
Pattern_2[3:0] corresponds to R[4], R[3], R[2], R[1] (Upper bits of row address)
Pattern_3[3:0] is ignored
Pattern_4[3:0] is ignored
Pattern_5[3:0] is ignored

The mask bits enable filtering using the corresponding bit in the pattern register. For example, a 1 in the LSB of Mask_1 means that the TXF module compares the LSB of Nibble_1 in the pattern register to the first data bit of the transaction. A 0 in the LSB of Mask_1 means that the TXF module ignores the first data bit of the transaction.

NOTE: The TXF filter 1 parameters can only be written and read when both the filter 1 and filter 2 enable bits (in register 9Bh) are 0. When reading the values, the values must be read consecutively, starting with the first value.

These registers hold the search parameters for filter 1. The parameters are used to parse the first five bytes of NABTS Teletext transactions or the first two bytes WST transactions. These bytes of teletext are expected to always contain four data bits interlaced with four Hamming protection bits. The protection bits are ignored by the filter.

2.13.51 TXF Filter 2 Parameters

VIP address	195h – 199h
PHI address	95h – 99h
I^2C address	95h – 99h

ADDRESS	7	6	5	4	3	2	1	0
95h	Filter 2 Mask_1[3:0]				Filter 2 Pattern_1[3:0]			
96h	Filter 3 Mask_2[3:0]				Filter 2 Pattern_2[3:0]			
97h	Filter 2 Mask_3[3:0]				Filter 2 Pattern_3[3:0]			
98h	Filter 2 Mask_4[3:0]				Filter 2 Pattern_4[3:0]			
99h	Filter 2 Mask_5[3:0]				Filter 2 Pattern_5[3:0]			

For an NABTS system, the packet prefix consists of five bytes: P1, P2, P3, CI and PS. Each byte contains four data bits interlaced with four Hamming protection bits.

Pattern_1[3:0] corresponds to P1[7], P1[5], P1[3], P1[1] (Packet address)
Pattern_2[3:0] corresponds to P2[7], P2[5], P2[3], P2[1] (Packet address)
Pattern_3[3:0] corresponds to P3[7], P3[5], P3[3], P3[1] (Packet address)
Pattern_4[3:0] corresponds to CI[7], CI[5], CI[3], CI[1] (Continuity index)
Pattern_5[3:0] corresponds to PS[7], PS[5], PS[3], PS[1] (Packet structure)

For a WST system (PAL or NTSC), the magazine and row address group consists of two bytes. The two bytes contain three bits of magazine number (M[2:0]) and five bits of row address (R[4:0]), interlaced with eight Hamming protection bits.

Pattern_1[3:0] corresponds to R[0], M[2], M[1], M[0] (Magazine and row LSBit)
Pattern_2[3:0] corresponds to R[4], R[3], R[2], R[1] (Upper bits of row address)
Pattern_3[3:0] is ignored
Pattern_4[3:0] is ignored
Pattern_5[3:0] is ignored

The mask bits enable filtering using the corresponding bit in the pattern register. For example, a 1 in the LSB of Mask_1 means that the TXF module compares the LSB of Nibble_1 in the pattern register to the first data bit of the transaction. A 0 in the LSB of Mask_1 means that the TXF module ignores the first data bit of the transaction.

NOTE: The TXF Filter 2 parameters can only be written and read when both the Filter 1 and Filter 2 enable bits (in register 9Bh) are 0. When reading the values, the values must be read consecutively, starting with the TXF Filter 1 parameter values.

These registers hold the search parameters for Filter 2. The parameters are used to parse the first five bytes of NABTS teletext transactions or the first two bytes WST transactions. These bytes of teletext are expected to always contain four data bits interlaced with four Hamming protection bits. The protection bits are ignored by the filter.

2.13.52 TXF Error Filtering Enables

VIP address	19Ah
PHI address	9Ah
I^2C address	9Ah

7	6	5	4	3	2	1	0
Reserved				LPC Error Enable	CCD Parity Error Enable	Teletext Parity Error Enable	Hamming Error Enable

LPC error enable	0 = disable (default)	1 = enable
CCD parity error enable	0 = disable (default)	1 = enable
Teletext parity error enable	0 = disable (default)	1 = enable
Hamming error enable	0 = disable (default)	1 = enable

These bits allow the TXP module to discard transactions based on bit errors. The Hamming error enable allows error correction and detection of Hamming encoded bytes. The teletext parity error enable allows the TXP to discard teletext transactions with parity errors. The CCD parity error enable allows the TXP to discard closed caption transactions with parity errors. The LPC error enable allows the TXP to discard teletext transactions with longitudinal parity errors.

2.13.53 TXF Transaction Processing Enables

VIP address	19Bh
PHI address	9Bh
I^2C address	9Bh

7	6	5	4	3	2	1	0
Reserved			Filter 2 enable	Filter 1 enable	CCD odd field enable	CCD even field enable	Teletext enable

Filter 2 enable	0 = disable (default)	1 = enable
Filter 1 enable	0 = disable (default)	1 = enable
CCD odd field enable	0 = disable (default)	1 = enable
CCD even field enable	0 = disable (default)	1 = enable
Teletext enable	0 = disable (default)	1 = enable

These bits are used to enable or disable certain features. The teletext enable allows the TXP module to receive teletext data. If this bit is 0, all outputs from the TXP remain idle while teletext data is present. The CCD even field enable and CCD odd field enable allow the TXP to receive closed caption data. The filter 1 enable allows the TXF module to parse data based on the values in the filter 1 parameters register. The filter 2 enable allows the TXF module to parse data based on the values in the filter 2 parameters register.

2.13.54 TTX Control Register

VIP address	1A0h
PHI address	A0h
I^2C address	A0h

7	6	5	4	3	2	1	0
Reserved				Full-Field Enable	Custom Framing Code	CCD Enable	TTX Mode

Full field enable	0 = No TTX search after VBI area	1 = TTX search all lines after VBI
Custom sync	0 = Use default TTX sync pattern	1 = Use sync pattern register
CCD enable	0 = Closed caption is DISABLED	1 = Closed caption is ENABLED
TTX mode	0 = NABTS	1 = WST

The TTX control register allows the operating parameters of the TDR to be controlled. Note that the TTX mode selection is independent of PAL/NTSC mode. This effectively controls the default framing code and data rate. Closed caption is affected by 525 lines vs 625 lines (but not NABTS/WST). For NTSC and PAL M, the CCD data search is on Line 21; for PAL B, G, I, combination-N it is on Line 22. The custom framing code affects teletext data only—closed caption data always uses the default sync pattern.

2.13.55 Line Enable Registers A, B

VIP address	1A1h – 1A2h
PHI address	A1h – A2h
I^2C address	A1h – A2h

	7	6	5	4	3	2	1	0
A1h – Line Enable Register A	Enable line 17/280 (14/327)	Enable line 16/279 (13/326)	Enable line 15/278 (12/325)	Enable line 14/277 (11/324)	Enable line 13/276 (10/323)	Enable line 12/275 (9/322)	Enable line 11/274 (8/321)	Enable line 10/273 (7/320)

	7	6	5	4	3	2	1	0
A2h – Line Enable Register B	Enable line 25/288 (22/335)	Enable line 24/287 (21/334)	Enable line 23/286 (20/333)	Enable line 22/285 (19/332)	Enable line 21/284 (18/331)	Enable line 20/283 (17/330)	Enable line 19/282 (16/329)	Enable line 18/281 (15/328)

NOTE: Line numbers in parenthesis refer to 625 Line systems

Line enable XX	0 = No TTX Search on line XX	1 = Search line XX for TTX data

In both VBI only and full field modes, the vertical interval lines can be individually enabled or disabled. Only lines that are enabled are searched for the selected type of teletext data. This allows some amount of filtering on a physical location basis. If closed caption data is enabled, this overrides the enable/disable bit for line 21 (22). If full field mode is enabled, *all lines after the vertical interval* are searched for the selected type of the teletext data. The registers are initialized to 0x00 on reset.

2.13.56 Sync Pattern Register

VIP address	1A3h
PHI address	A3h
I^2C address	A3h

7	6	5	4	3	2	1	0
Framing Code [7:0]							

If the custom sync bit is set in the control register, the sync comparator uses the contents of the sync pattern register as the bit pattern for the teletext framing code. Otherwise, the default sync patterns are used. Relative to the sync pattern register, incoming bits are shifted in MSB first. To illustrate; the default WST framing code would be specified as 0xE4 and the default NABTS framing code would be specified as 0xE7 (although the MSB vs LSB is ambiguous for the latter).

> **NOTE:** The custom sync option is only valid for NABTS or WST messages; closed caption always uses the EIA standard start bit pattern.

2.13.57 Teletext FIFO

VIP address	N/A
PHI address	B0h
I^2C address	B0h

7	6	5	4	3	2	1	0
Teletext Data FIFO [7:0]							

The teletext FIFO can be accessed via the regular teletext FIFO register at address B0h if PHI or I2C host interface is enabled or via VIP FIFO A at location 4 in VIP FIFO address space if VIP host interface is enabled.

Reading this location returns 1 byte from the FIFO that stores teletext transactions. If the FIFO is empty, a read returns the same value as the previous read**.** *It is the driver software's or application software's responsibility to assure that the correct number of bytes per transaction are read out from the teletext FIFO.* The transaction length depends on whether the data is NABTS, WST-NTSC, or WST-PAL.

2.13.58 Closed Caption Data

VIP address	1B2h
PHI address	B2h
I^2C address	B2h

The closed caption data contains two bytes per transaction. To retrieve both bytes, this register must be read twice. The first read returns the first byte of the message; the second read returns the second byte. Further reads return the first byte until new data is received. In order to distinguish between closed caption data received in the odd and even fields, software can test the field sequence status bit (Address 82h, bit 4).

2.13.59 Buffer Status

VIP address	1B3h
PHI address	B3h
I^2C address	B3h

7	6	5	4	3	2	1	0
Reserved	CCD avail	Tx count [3:0]				FIFO full	Teletext data avail

CCD avail — This status bit indicates that closed caption data has been received. The status bit is cleared when both of the two bytes have been read.

Tx count — This value represents the number of *complete* teletext transactions in the FIFO.

FIFO full — This bit indicates that the maximum number of complete teletext transaction is in the FIFO.

Teletext avail — This bit indicates that at least one *complete* teletext transaction is in the FIFO. This bit is cleared when the FIFO is emptied.

2.13.60 Interrupt Threshold

VIP address	1B4h
PHI address	B4h
I^2C address	B4h

7	6	5	4	3	2	1	0
Reserved				Threshold Value [3:0]			

Threshold value — This value determines how many teletext transactions must be received before the teletext threshold bit is set in the interrupt status register. The default value is 5.

2.13.61 Interrupt Line Number

VIP address	1B5h
PHI address	B5h
I^2C address	B5h

7	6	5	4	3	2	1	0
Reserved		Data Required	Interrupt Line Number [4:0]				

Data required — If this bit is set HIGH, the teletext data bit in the interrupt status register A is only set if there is data in the FIFO. This bit does not affect the CC odd field and CC even field bits in the interrupt status register A. The default value for this bit is 1.

Interrupt line number — This value determines which video line number is used to generate the teletext data, CC even field, and CC odd field bits in the interrupt status register A at address C0. The register value is examined at the start of the line. Since there is no line 0, a value of all zeros in this register disables the three interrupt signals that use this condition. The default value is 24 (18h).

2.13.62 FIFO Control

VIP address	1B6h
PHI address	B6h
I^2C address	B6h

7	6	5	4	3	2	1	0
Reserved			CCD reset	Read in Progress	RAM Test	TTX PHI Output Enable	FIFO Reset

CCD reset — When a 1 is written to this register bit, the closed caption register is reset. Also, the flag is cleared to 0. This bit is automatically cleared back to 0.

Read in progress — This bit indicates that the first byte of a teletext transaction has been read, but the last byte has not been read. This bit can be used to verify data alignment as it is read from the FIFO.

RAM test — Setting this bit high allows the external processor to write data into the FIFO. In this mode, data from the TXP is ignored. This allows the micro to test the RAM by writing and reading test patterns. The default value is zero.

TTX PHI output enable — A 1 in this register enables access to the teletext data in the FIFO through the parallel host port or I^2C interface and disables access from the output formatter. A 0 disables access from the parallel host port or I^2C interface and enables access from the output formatter. The default value is one.

FIFO reset — When a 1 is written to this register bit, the FIFO is flushed. This is done by clearing the read and write pointers to zero, clearing the Tx count to zero, and clearing all status flags. This bit is automatically cleared back to 0.

2.13.63 FIFO RAM Test

VIP address	1B7h
PHI address	B7h
I^2C address	B7h

7	6	5	4	3	2	1	0
FIFO RAM Data							

FIFO RAM test register provides diagnostic capability into the internal teletext FIFO. This register can be written sequentially with a block of data. The data is read back using the teletext FIFO data register at address B0h to verify the correct operation of the FIFO.

2.13.64 Interrupt Status Register A

VIP address	1C0h
PHI address	C0h
I^2C address	C0h

7	6	5	4	3	2	1	0
TvpLOCK state	TvpLOCK interrupt	Cycle complete	Bus error	CC odd field	CC even field	Teletext threshold	Teletext data

tvpLOCK state
0 = TVP not locked to video (default)
1 = TVP locked to video signal
Reflects the present state of the tvpLOCK.

tvpLOCK interrupt
0 = A transition has not occurred on the tvpLOCK signal (default)
1 = A transition has occurred on the tvpLOCK signal
Note, an interrupt is generated on any transition of the Lock signal.

Cycle complete
0 = Read or write cycle in progress (default)
1 = Read or write cycle complete

Bus error
0 = No bus error (default)
1 = PHI interface detected an illegal access

CC odd field
0 = Buffer empty (default)
1 = Odd field closed caption buffer contains data

CC even field
0 = Buffer empty (default)
1 = Even field closed caption buffer contains data

Teletext threshold
0 = Threshold not reached (default)
1 = Teletext data in buffer has reached configurable threshold

Teletext data
0 = Teletext data buffer empty or the video line number has not reached the value programmed in the interrupt line number register at address B5. (default)
1 = Teletext data buffer contains a complete transaction and the video line number = interrupt line number
Note this bit can be configured to occur whenever the video line number = interrupt line number register regardless of the data.

The interrupt status register A is polled by the external processor to determine the interrupt source. After an interrupt condition is set it can be reset by writing to this register with a 1 in the appropriate bit(s).

2.13.65 Interrupt Enable Register A

VIP address	1C1h
PHI address	C1h
I^2C address	C1h

7	6	5	4	3	2	1	0
tvpLOCK state	tvpLOCK interrupt enable	Cycle complete enable	Bus Error Enable	CC odd field enable	CC even field enable	Teletext threshold enable	Teletext data enable

The interrupt enable register A is used by the external processor to mask unnecessary interrupt sources for interrupt A. Bits loaded with a 1 allow the corresponding interrupt condition to generate an interrupt on the external pin. Conversely bits loaded with a 0 mask the corresponding interrupt condition from generating an interrupt on the external pin. Note this register only affects the interrupt A on the external terminal, it does not affect the bits in the interrupt status register A. A given condition can set the appropriate bit in the status register and not cause an interrupt on the external terminal. To determine if this device is driving the interrupt terminal either perform a logical AND of the interrupt status register A with the interrupt enable register A, or check the state of the interrupt A bit in the interrupt configuration register A.

2.13.66 Interrupt Configuration Register A

VIP address	1C2h
PHI address	C2h
I^2C address	C2h

7	6	5	4	3	2	1	0
Reserved					YUV output enable A	Interrupt A	Interrupt polarity A

YUV output enable A	0 = YUV pins are 3-state
	1 = YUV pins are active if other conditions are met
Interrupt A	0 = Interrupt terminal is not active
	1 = Interrupt terminal is active
	Reflects state of interrupt A on the external pin
Interrupt polarity	0 = Interrupt is active low
	1 = Interrupt is active high

The interrupt configuration register A is used to configure the polarity of the external in interrupt pin. Note that when the interrupt is configured for active low the terminal is driven low when active and 3-state when inactive (open-collector). Conversely, when the terminal is configured for active high it is driven high for active and driven low for inactive. The interrupt A bit is read-only.

2.13.67 VIP Teletext FIFO

VIP address	1400h
PHI address	N/A
I^2C address	N/A

7	6	5	4	3	2	1	0
Teletext Data FIFO [7:0]							

The teletext FIFO can be accessed via the regular teletext FIFO register at address B0 if PHI or I2C host interface is enabled, or via VIP FIFO A at location 4 in VIP FIFO address space if VIP host interface is enabled.

Reading this location returns 1 byte from the FIFO that stores teletext transactions. If the FIFO is empty, a read returns the same value as the previous read**.** *It is the driver software's or application software's responsibility to assure that the correct number of bytes per transaction are read out from the teletext FIFO.* The transaction length depends on the whether the data is NABTS, WST-NTSC, or WST-PAL.

2.13.68 VIP Program RAM Write

VIP address	1500h
PHI address	N/A
I^2C address	N/A

7	6	5	4	3	2	1	0
Program RAM Write Data							

If the PHI or I^2C host interface is enabled, the program RAM can be written via the nonVIP program RAM write register at address 7E. If the VIP host interface is enabled, the program RAM can be written via VIP FIFO B at location 5 in the VIP FIFO address space.

2.13.69 VIP Program RAM Read

VIP address	1600h
PHI address	N/A
I^2C address	N/A

7	6	5	4	3	2	1	0
Program RAM Read Data							

If the PHI or I^2C host interface is enabled, the program RAM can be read via the nonVIP program RAM read register at address 8E. If the VIP host interface is enabled, the program RAM can be read via VIP FIFO B at location 6 in the VIP FIFO address space.

2.13.70 Parallel Host Interface Teletext FIFO

VIP address	N/A
PHI address	10b
I^2C address	N/A

7	6	5	4	3	2	1	0
Teletext FIFO							

This read-only register is only accessible when the PHI interface is enabled. To access this register, use the direct address of 10. Notice almost all the PHI registers are accessed through an indirect address scheme, by writing the indirect address to address 00 and then write to or read from address 01. This register contains the same information as the teletext FIFO register at indirect address B0 and is the recommended way of reading data from the teletext FIFO due to its efficiency.

2.13.71 Parallel Host Interface Status/Interrupt A

VIP address	N/A
PHI address	11b
I^2C address	N/A

7	6	5	4	3	2	1	0
TvpLOCK state	TvpLOCK interrupt	Cycle complete	Bus error	CC odd field	CC even field	Teletext threshold	Teletext data

The read-write register is only accessible when the VMI interface is enabled. To access this register, use the direct address of 11. Notice almost all the VMI registers are accessed through an indirect address scheme, by writing the indirect address to address 00 and then writing to or reading from address 01. This register contains the same information as the interrupt status register A at indirect address C0 and is the recommended way of reading the interrupt/status information due to its efficiency. After an interrupt condition is set, it can be reset by writing to this register with a 1 in the appropriate bit(s).

tvpLOCK state	0 = TVP not locked to video (default) 1 = TVP locked to video signal Reflects the present state of the tvpLOCK.
tvpLOCK interrupt	0 = A transition has not occurred on the tvpLOCK signal (default) 1 = A transition has occurred on the tvpLOCK signal Note, an interrupt is generated on any transition of the lock signal.
Cycle complete	0 = Read or write cycle in progress 1 = Read or write cycle complete (default)
Bus error	0 = No bus error (default) 1 = PHI interface detected an illegal access
CC odd field	0 = Buffer empty (default) 1 = Odd field closed caption buffer contains data
CC even field	0 = Buffer empty (default) 1 = Even field closed caption buffer contains data
Teletext threshold	0 = Threshold not reached (default) 1 = Teletext data in buffer has reached configurable threshold
Teletext data	0 = Teletext data buffer empty or we have not reached the video line number that equals the interrupt line number register (default) 1 = Teletext data buffer contains a complete transaction and the video line number = interrupt line number Note this bit can be configured to occur whenever the video line number = interrupt line number register regardless of the data.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Digital power supply voltage, DV_{DD} . . . . . –0.3 V to 3.6 V
Analog power supply voltage, AV_{DD} . . . . . –0.5 V to 3.6 V
Digital input voltage, Vi . . . . . –0.3 V to DV_{DD}+0.3 V
Operating free-air temperature, T_A . . . . . 0°C to 70°C
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Maximum total power dissipation, P_D . . . . . 2.5 W

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Digital supply voltage, DV_{DD}	3	3.3	3.6	V
Analog supply voltage, AV_{DD}	3.1	3.3	3.5	V
Analog input voltage, V_i(p-p) (ac coupling necessary)	0.5	1	1.26	V
Digital input voltage high, V_{IH}	2			V
Digital input voltage low, V_{IL}			0.8	V
Input voltage high, VC0 and VC1 in I^2C mode, V_{IH} (I^2C)	2.3			V
Input voltage low, VC0 and VC1 in I^2C mode, V_{IL} (I^2C)			1	V
Output current, Vout=2.4 V, I_{OH}	–4	–8		mA
Output current, Vout=0.4 V, I_{OL}	6	8		mA
Operating free-air temperature, T_A	0		70	°C

3.2.1 Crystal Specifications

	MIN	NOM	MAX	UNIT
Frequency		14.31818		MHz
Frequency tolerance			±50	ppm

3.3 Electrical Characteristics Over Recommended Voltage and Temperature Ranges, DV_{DD} = 3.3 V, AV_{DD} = 3.3 V, T_A = 70°C (unless otherwise noted)

3.3.1 DC Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(D)}$	Digital supply current			220	340	mA
$I_{DD(A)}$	Analog supply current			80	150	mA
I_{lkg}	Input leakage current				10	µA
C_i	Input capacitance	By design			8	pF
V_{OH}	Output voltage high		2.4			V
V_{OL}	Output voltage low				0.4	V

NOTE 1: Measured with a load of 10 kΩ in parallel to 15 pF.

3.3.2 Analog Processing and A/D Converters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zi	Input impedance, analog video inputs	By design	200			kΩ
C_i	Input capacitance, analog Video inputs	By design			10	pF
Vi(pp)	Input voltage range	$C_{coupling}$ = 0.1 µF	0.50	1	1.41	V
ΔG	Gain control range		–5		5	dB
DNL	DC differential nonlinearity	A/D only		0.75	1	LSB
	Frequency response	Multiburst (60 IRE)		–0.9	–3	dB
	Crosstalk	6 MHz			–50	dB
	Noise spectrum	Luminance ramp (100 kHz full; tilt-null)		–57		dB
	Differential phase	Modulated ramp		0.7		°(pk-pk)
	Differential gain	Modulated ramp		0.5%		

3.4 Timing

3.4.1 Clocks, Video Data, and Sync Timing

PARAMETER		TEST CONDITIONS (see NOTE 2)	MIN	TYP	MAX	UNIT
	Duty cycle PCLK, SCLK		40%	50%	60%	
$t_{r(1)}$	Rise time SCLK	10% to 90%		3		ns
$t_{f(1)}$	Fall time SCLK	90% to 10%		2		ns
$t_{r(2)}$	Rise time PCLK	10% to 90%		3		ns
$t_{f(2)}$	Fall time PCLK	90% to 10%		2		ns
$t_{d(8)}$	Delay time, SCLK rising edge to PREF				5	ns
$t_{d(9)}$	Delay time, SCLK falling edge to PCLK	See Note 3	–2		3	ns
$t_{d(10)}$	Delay time, SCLK falling edge to digital outputs except PCLK, PREF	See Note 3	–2		10	ns

NOTES: 2. C_L = 50 pF
3. SCLK falling edge may occur up to 2 ns after PREF, Y, UV output transition.

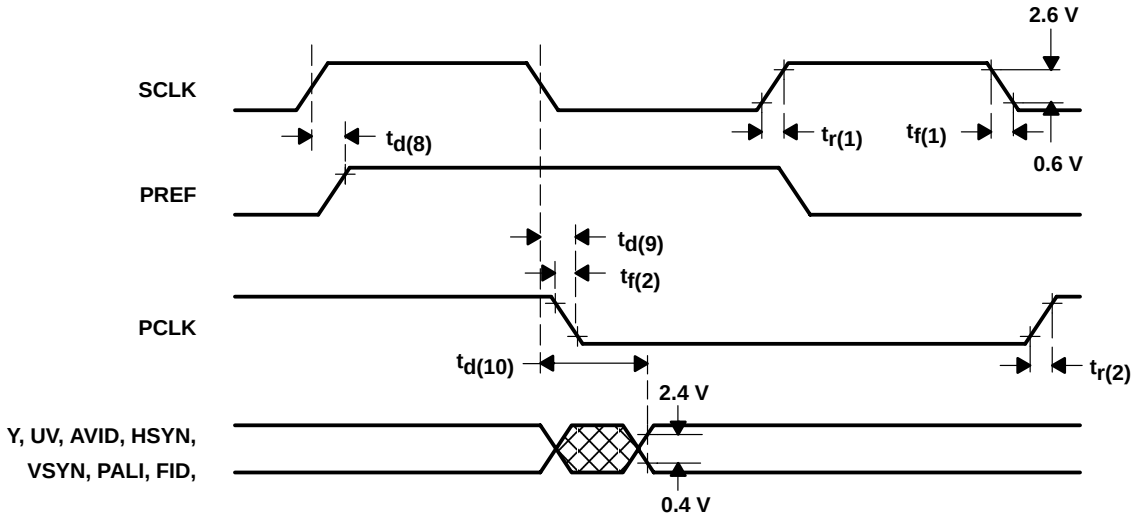


Figure 3–1. Clocks, Video Data, and Sync Timing

3.4.2 I²C Host Port Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(11)}$	Bus free time between STOP and START		1.3			µS
$t_{su(8)}$	Setup time for a (repeated) START condition		0.6			µS
$t_h(8)$	Hold time (repeated) START condition		0.6			µS
$t_{su(9)}$	Setup time for a STOP condition		0.6			µS
$t_{su(10)}$	Data setup time		100			nS
$t_{h(9)}$	Data hold time		0		0.9	µS
$t_{r(3)}$	Rise time VC1(SDA) and VC0(SCL) signal				250	nS
$t_{f(3)}$	Fall time VC1(SDA) and VC0(SCL) signal				250	nS
	Capacitive load for each bus line				400	pF
	I²C clock frequency				400	kHz

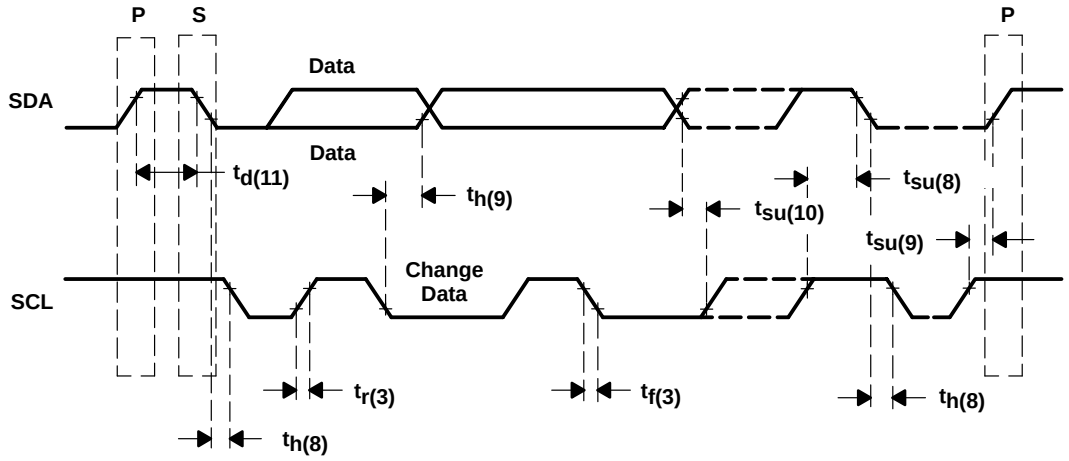


Figure 3–2. I²C Host Port Timing

3.4.3 VIP Host Port Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su(11)}$	VC0,VC1,VC2 setup to VC3 (VIPCLK)		5			ns
$t_{h(10)}$	VC3 (VIPCLK) to VC0, VC1, VC2 hold time		0			ns
$t_{pd(1)}$	Propagation delay, VC3 (VIPCLK) to VC0, VC1, VC2, INTREQ				11	ns

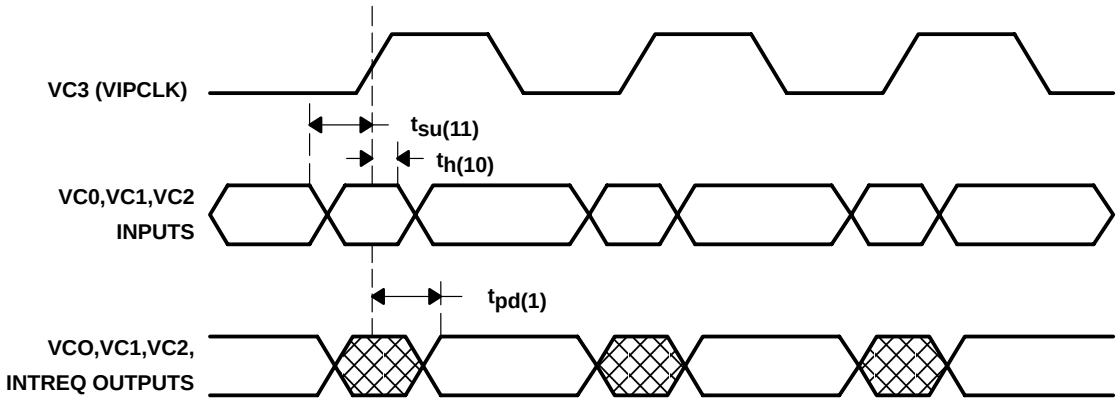


Figure 3–3. VIP Host Port Timing

3.4.4 Parallel Host Interface A

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su(1)}$	A[1:0],D[0:7], RD/$\overline{WR}$ setup until $\overline{DS}$ low		5			ns
$t_{d(1)}$	Delay $\overline{DTACK}$ low after $\overline{DS}$ low		0			ns
$t_{h(1)}$	A[1:0], D[0:7], RD/$\overline{WR}$ hold after $\overline{DS}$ high		5			ns
$t_{d(2)}$	Delay $\overline{DS}$ high after $\overline{DTACK}$ low		5			ns
$t_{d(3)}$	Delay $\overline{DTACK}$ high after $\overline{DS}$ high		0			ns
$t_{d(4)}$	Delay $\overline{DS}$ low(next cycle) after $\overline{DTACK}$ high		5			ns
$t_{su(2)}$	(Read cycle) D[7:0] setup until $\overline{DTACK}$ low		10			ns
$t_{h(2)}$	(Read cycle) D[7:0] hold after $\overline{DS}$ high		0			ns

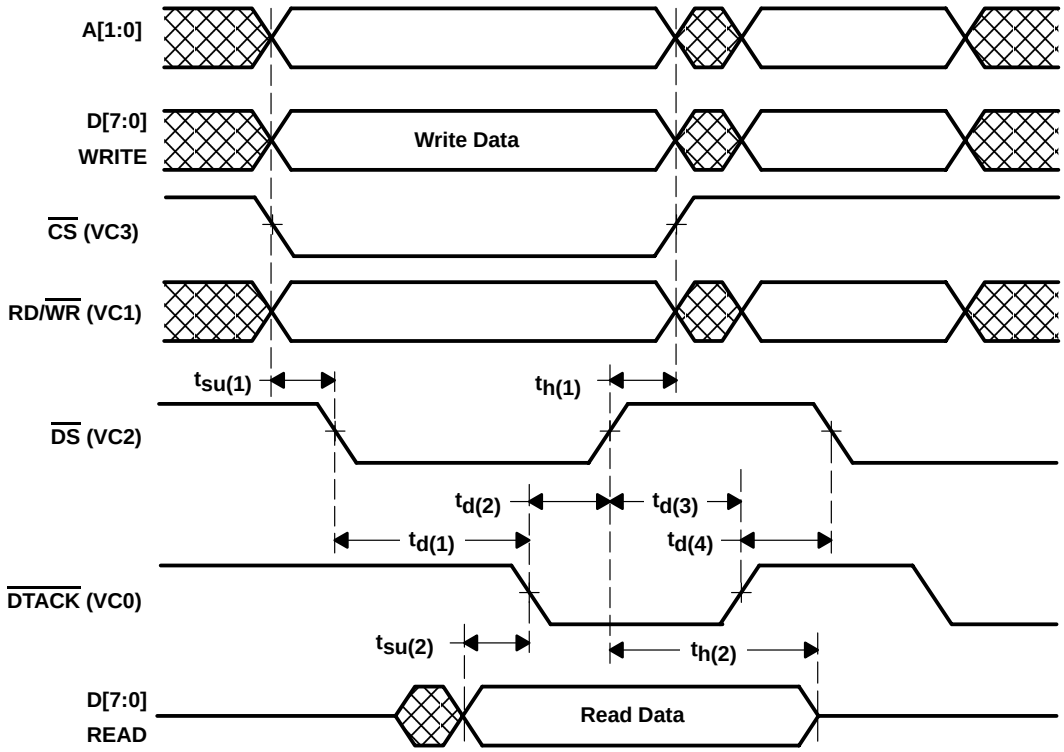


Figure 3–4. Parallel Host Interface A Timing

3.4.5 Parallel Host Interface B

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su(3)}$	A[1:0], $\overline{CS}$ setup until $\overline{WR}$ or $\overline{RD}$ active		10			ns
$t_{h(3)}$	A[1:0], $\overline{CS}$ hold after $\overline{WR}$ or $\overline{RD}$ inactive		10			ns
$t_{d(5)}$	Delay RDY low after $\overline{WR}$ or $\overline{RD}$ active				28	ns
$t_{su(4)}$	D[7:0] setup until $\overline{WR}$ active		5			ns
$t_{h(4)}$	D[7:0] hold after $\overline{WR}$ inactive		10			ns
$t_{w(1)}$	RDY inactive pulse width		10			ns
$t_{w(2)}$	$\overline{WR}$ inactive until any command active		80			ns
$t_{su(5)}$	(Read cycle) D[7:0] setup until RDY active		0			ns
$t_{h(5)}$	(Read cycle) D[7:0] hold after $\overline{RD}$ inactive		0			ns
$t_{d(6)}$	Delay $\overline{WR}$ or $\overline{RD}$ inactive after RDY active		0			ns
$t_{w(3)}$	$\overline{WR}$, $\overline{RD}$ command pulse width		40			ns

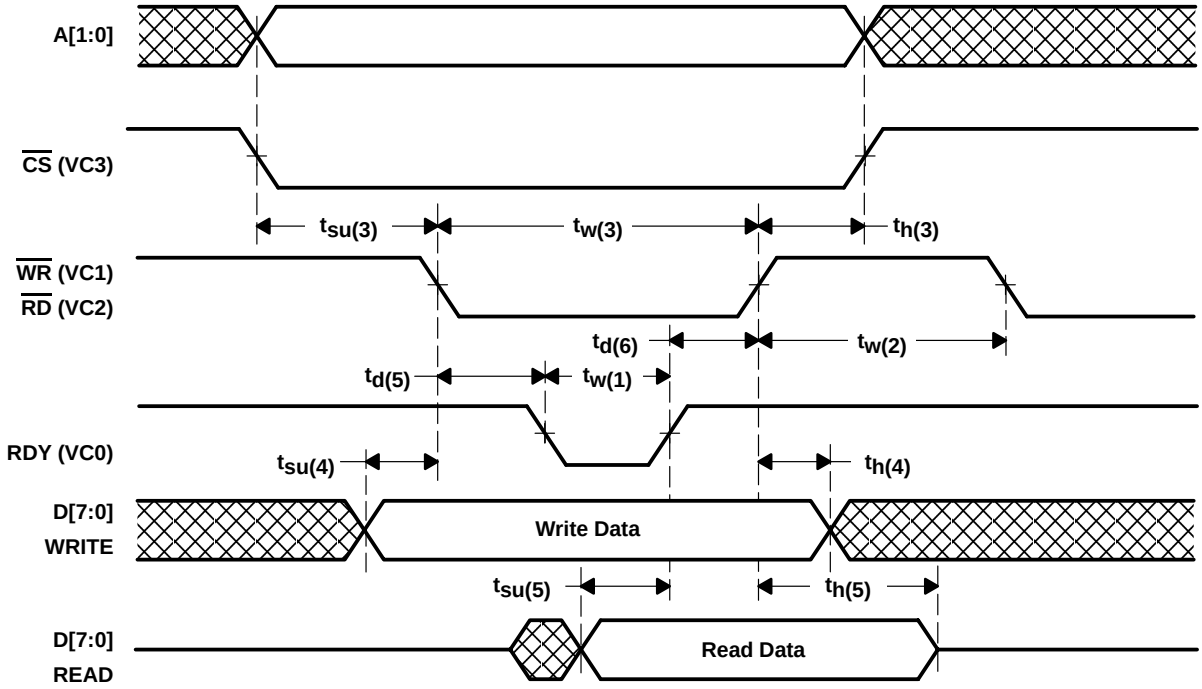


Figure 3–5. Parallel Host Interface B Timing

3.4.6 Parallel Host Interface C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su(6)}$	A[1:0],D[7:0], RD/$\overline{WR}$, $\overline{CS}$ setup until $\overline{DS}$ low		5			ns
$t_{h(6)}$	A[1:0],D[7:0], RD/$\overline{WR}$, $\overline{CS}$ hold after $\overline{DS}$ high		0			ns
$t_{d(7)}$	Delay RDY low after $\overline{DS}$ low		2			ns
$t_{su(7)}$	(Read cycle) D[7:0] setup until RDY high		20			ns
$t_{h(7)}$	(Read cycle) D[7:0] hold after $\overline{DS}$ high		0			ns

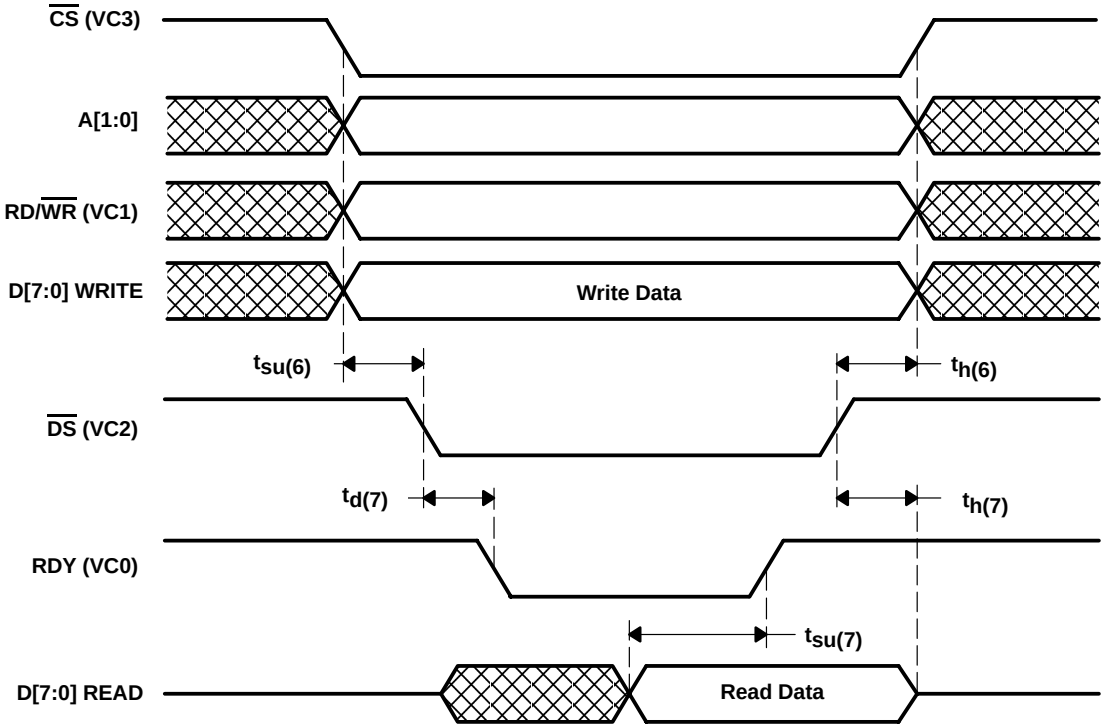


Figure 3–6. Parallel Host Interface C Timing

4 Application Information

4.1 Microcode Download

The TVP5040 has an internal processor and an associated 5Kx20 instruction RAM. The microprocessor controls many of the device functions including PLL operation, AGC, sync, and register configuration. This programmable architecture allows the TVP5040 performance to be enhanced with upgraded algorithms. The microcode for the internal processor is downloaded to the TVP5040 during each power-up as described later.

The details of downloading the microcode depends on the host interface being used (I^2C, VIP, or PHI).

4.1.1 Timing Requirement for Start of Download

Following the negation of the reset signal (RSTINB asserted high), the microcode instructions may be downloaded after at least 4 pixel clock (PCLK) cycles have elapsed. Note that this time period is longer if the TVP5040 has not already been initialized.

4.1.2 General Microcode Download Procedure

In general, the procedure is initiated by addressing the program RAM write register (address 7Eh) for a write operation. After this the internal microprocessor is disabled and the internal microcode RAM is ready for microcode download. The first instruction byte and subsequent instruction bytes written to the program RAM write register are loaded to sequential locations of the microcode RAM. Each 20-bit instruction is transmitted using three bytes, with the most significant byte first. Since the microcode RAM is 20-bits wide, the upper four bits of the most significant byte are discarded before the data is written to the microcode RAM.

It is possible to complete the microcode download in a single burst of consecutive write cycle. If needed, the data may be transmitted in separate blocks, so long as no other TVP5040 register (other than address 7Eh) is accessed in between blocks. If another TVP5040 register is accessed, the microprocessor internal instruction RAM address pointer is reset to zero and resumes operation.

4.1.3 Microprocessor Restart Operation

As noted before, the internal microprocessor unit is disabled during microcode download. Therefore, after completion of the microcode download (that is, all microcode instructions have been written to the program RAM), a write cycle to a register 7Fh is required to wake up the microprocessor and restart normal operation of the TVP5040.

4.1.3.1 Timing Requirement fort Microprocessor Restart

After the microprocessor-restart operation has been initiated, the microprocessor takes up to 5 ms for its initialization code to complete. Only then register initialization via the host port begin. The following sections describe how this latency is handled for the different host interfaces.

4.1.3.2 Implementation for I^2C Bus

After the restart operation has been performed, the TVP5040 drives the I^2C clock (SCL) low to signal the I^2C master to wait I^2C implementation vary in the way this is handled. A problem arises when the I^2C master tries to generate STOP condition without checking if the I^2C bus is free (that is, SCL high). This attempted-STOP condition is not recognized by the I^2C slave. The master then stops for a software-generated delay to meet the timing requirement mentioned in Section 4.1.3.1. Finally, the I^2C master resumes operation by generating a START condition. Since no STOP condition was recognized by the slave, this is seen as a RESTART condition, which the TVP5040 does not support.

To prevent this from happening, it is necessary for the master to wait until the I^2C bus is free (that is, SCL high) before generating a STOP condition, thus insuring that a valid STOP condition is generated. This provides the optimal amount of delay and eliminates the need for a software-generated delay.

The I^2C master must also wait until the I^2C bus is free (that is, SCL high) before generating a START condition.

4.1.3.3 Implementation for PHI Bus

For PHI host interface-based applications, the interrupt request (INTREQ) pin (or interrupt status register polling) may be used to determine when the TVP5040 is ready to proceed with host interface activity. This eliminates the need for a software-generated delay.

4.1.3.4 Implementation for VIP

For VIP host interfaced-based application, the slave-terminate and master-retry mechanisms are used to handle the latency after microprocessor restart. TVP5040 slaves terminate all VIP access until the microprocessor initialization is completed. Meanwhile, the VIP master repeatedly retries the current VIP access until it is accepted by the TVP5040. This eliminates the need for a software-generated delay.

4.1.4 Microcode Data File

TI provides the TVP5040 microcode as binary code in a Hex-ASCII file format. Figure 4–1 is an example of this file format. The file is available via the TI Web pages beginning at URL: http://www.ti.com

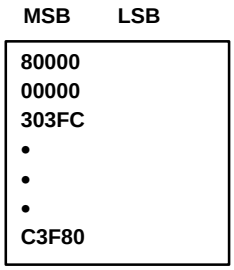


Figure 4–1. TVP5040 Microcode in Hex-ASCII Format

4.1.5 Default Values

The Table 4–1 shows initial values of the registers after the microcode downloaded with an autoswitch mode setting. The default mode is NTSC ITU-R BT.601.

Table 4–1. Default Values

ADDRESS	VALUE	NOTE
00	00	Video input source selection : Channel 1: V11A selected, Channel: V12A Selected
01	15	Automatic offset control enabled, AGC enabled using luma input as the reference
02	00	TV/VCR mode: automatic, Color subcarrier DTO frozen: DTO increments by the internally-generated phase increments. Power-down mode: Normal operation
03	01	GPCL is logic 0 output. PALI outputs PAL indicator signal and FID outputs field ID signal. Y U/V high-impedance. HSYN, VSYN, AVID, PALI, and FID are high-impedance. Vertical blanking off SCLK and PCLK outputs are high-impedance. (If the AVID pin is pulled down during reset and the PREF is pulled down during reset.)
	09	GPCL is logic 0 output. PALI outputs PAL indicator signal and FID outputs field ID signal. Y U/V high-impedance. SCLK and PCLK outputs are enabled. HSYN, VSYN, AVID, PALI, and FID are active. (If the AVID pin is pulled up during reset.)
05	00	No software reset
06	10	Automatic color killer on, color killer threshold: –24 dB
07	00	Input video bypasses the chroma trap and comb filters. 7.5 IRE pedestal is present. Luma bypasses mode during vertical blanking: No, Luma signal delay: 0 pixel clocks delay.
08	00	Luma comb filter enabled, peaking gain disabled.
09	80	Brightness: 128
0A	80	Color saturation: 128
0B	00	Hue control: 0 degrees
0C	80	Contrast control: 128
0D	40	ITU–R BT.601 sampling rate, ITU–R BT.601 coding range, offset binary code, YUV data path bypass: normal operation, YUV output format: 20–bit 4:2:2 YUV
0E	00	Luminance filter select: 1.2129 MHz, NTSC CCIR601
16	80	HSYN start: 0 pixel clocks
18	00	Vertical blanking VBLK start: same time as start of vertical blanking interval
19	00	Vertical blanking VBLK stop: same time as end of vertical blanking interval
1A	2C	Adaptive between 3-line comb filter, Color DTO not reset, Automatic color gain control enabled.
1B	00	Chrominance output bandwidth: 1.2129 MHz
1C	00	All interrupt reset: no effect
1D	00	All interrupt source masked
1E	01	Interrupt B is active high
20	00	Decimation filter bypass disabled, Chroma: ADC1 selected, Luma/composite: ADC1 selected
25	00	Lock speed: Fast lock disabled
26	00	Crystal frequency: 14.31818 MHz
28	00	Video standard: Autoswitch mode
9A	00	LPC error disabled, CCD parity error disabled, teletext parity error disabled, Hamming error disabled
9B	00	Filter 2 disabled, Filter 1 disabled, CCD odd field disabled, CCD even field disabled, teletext disabled
A0	00	No TTX search after VBI area, use default TTX sync. closed caption is disabled, NABTS
A1	00	No TTX search
A2	00	No TTX search
B4	05	Threshold value: 5
B5	38	Data required, interrupt line number: 24
B6	02	TTX PHI/I^2C output enabled
C1	00	All interrupt disabled
C2	04	YUV pins are 3-state, interrupt terminal is not active, interrupt is active low

4.2 Designing With PowerPAD™

The TVP5040 is housed in a high-performance, thermally enhanced, 80–pin PowerPAD package (TI package designator: 80PFP). Use of the PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing the PowerPAD PCB features, the use of solder masks (or other assembly techniques) may be required to prevent any inadvertent shorting by the exposed PowerPAD of connection etches or vias under the package. The recommended option, however, is not to run any etches or signal vias under the device, but to have only a grounded thermal land as explained below.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD package. The thermal land will vary in size, depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

More information on the package and other requirements for using thermal lands and thermal vias are detailed in the TI application note PowerPAD *Thermally Enhanced Package Application Report*, TI literature number SLMA002, available via the TI Web pages beginning at URL: http://www.ti.com

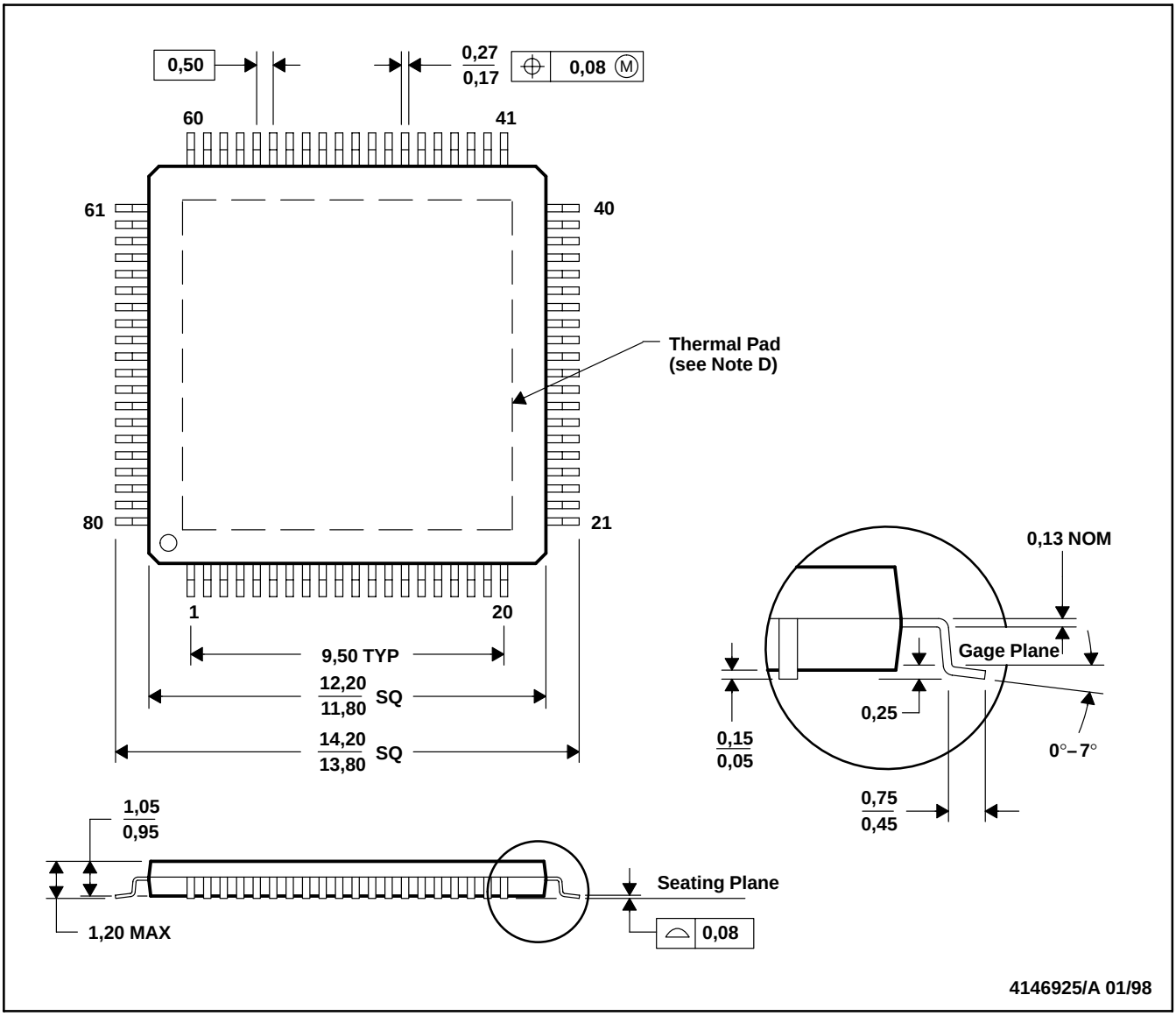
For the TVP5040, this thermal land should be grounded to the low impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground terminal landing pads be connected directly to the grounded thermal land. The land size should be as large as possible without shorting device signal terminals. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low impedance ground plane for the device.

PowerPAD is a trademark of Texas Instruments.

5 Mechanical Data

PFP (S-PQFP-G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

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