FAIRCHILD
SEMICONDUCTOR ™

MM74HC4049 • MM74HC4050
Hex Inverting Logic Level Down Converter •
Hex Logic Level Down Converter

General Description

The MM74HC4049 and the MM74HC4050 utilize advanced silicon-gate CMOS technology, and have a modified input protection structure that enables these parts to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0–15V CMOS logic can be converted to 0–5V logic when using a 5V supply. The modified input protection has no diode connected to V_{CC}, thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition each part can be used as a sim-

ple buffer or inverter without level translation. The MM74HC4049 is pin and functionally compatible to the CD4049BC and the MM74HC4050 is compatible to the CD4050BC

Features

■ Typical propagation delay: 8 ns
■ Wide power supply range: 2V–6V
■ Low quiescent supply current: 20 μA maximum (74HC)
■ Fanout of 10 LS-TTL loads

Ordering Code:

Order Number	Package Number	Package Description
MM74HC4049M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4049SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4049MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153. 4.4mm Wide
MM74HC4049N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HC4050M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4050SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4050MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153. 4.4mm Wide
MM74HC4050N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

TOP VIEW
MM74HC4049

TOP VIEW
MM74HC4050

MM74HC4049 • MM74HC4050
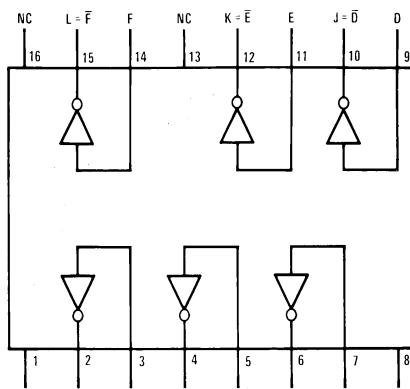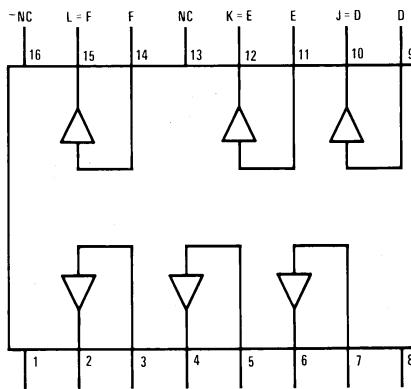
Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to +18V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{ZK}, I_{OK})	−20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input Voltage (V_{IN})	0	15	V
DC Output Voltage (V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C Typ	T_A = −40°C to 85°C	T_A = −55°C to 125°C	Units
					Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $|I_{OUT}| \leq 20$ μA	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $|I_{OUT}| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	V
		$|I_{OUT}| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	V
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $|I_{OUT}| \leq 20$ μA	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $|I_{OUT}| \leq 4$ mA	4.5V	0.2	0.26	0.33	V
		$|I_{OUT}| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	μA
		V_{IN} = 15V	2.0V		±0.5	±5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	μA

Note: the table above has columns for T_A = 25°C (Typ), T_A = −40°C to 85°C, and T_A = −55°C to 125°C. Values for V_{IH}: at 25°C guaranteed 1.5/3.15/4.2, −40 to 85°C 1.5/3.15/4.2, −55 to 125°C 1.5/3.15/4.2. I_{IN} 6.0V: ±0.1, ±1.0, ±1.0. V_{IN}=15V 2.0V: ±0.5, ±5, ±5. I_{CC} 6.0V: 2.0, 20, 40.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

$V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$ Typ	$T_A = 25°C$	$T_A = -40°$ to $85°C$	$T_A = -55°$ to $125°C$	Units
					Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	30	85	100	130	ns
			4.5V	10	17	20	26	ns
			6.0V	9	15	18	22	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted

0.386 − 0.394
(9.804 − 10.00)

16 15 14 13 12 11 10 9

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO.1
IDENT

1 2 3 4 5 6 7 8

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
(0.203)

0.014 − 0.020 TYP
(0.356 − 0.508)

M16A (REV H)
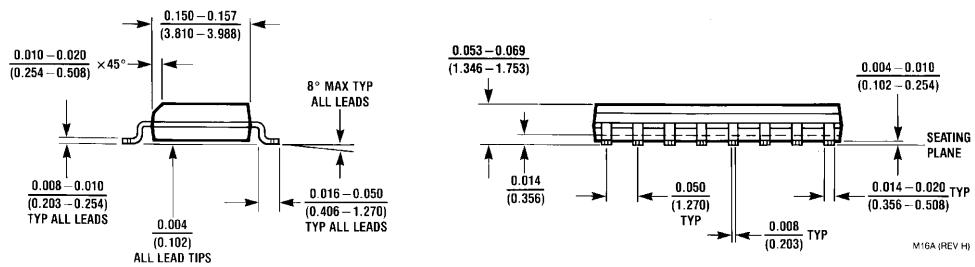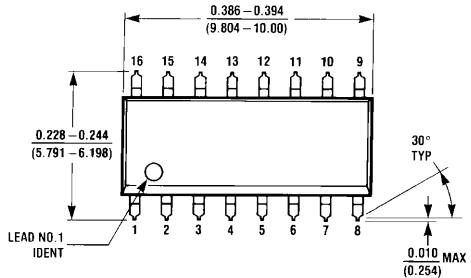
16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

10.2±0.1
-A-

0.47 TYP

16   9

7.8

3.9

5.3±0.1
-B-

PIN #1 IDENT.

1   8

0.2 C B A
ALL LEAD TIPS

16 15   10 9

5.01 TYP
9.27 TYP

(2.13 TYP)

1   2   7   8

1.27 TYP   0.6 TYP

LAND PATTERN RECOMMENDATION

ALL LEAD TIPS
0.1 C

2.1 MAX.

-C-

1.27 TYP

1.8±0.1

0.15±0.05

0.35-0.51

0.12 M C A
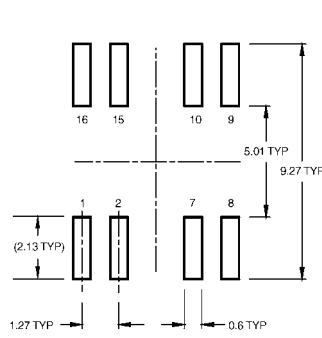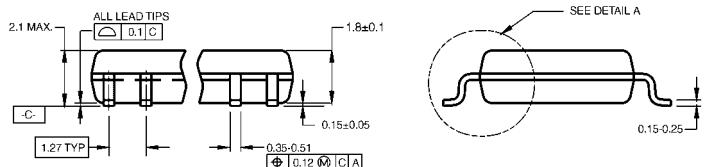
DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.15-0.25

7° TYP

GAGE PLANE
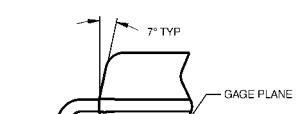
16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS METRIC ONLY

LAND PATTERN RECOMMENDATION

7.72 TYP.

4.16 TYP.

(1.78 TYP)

0.42 TYP

0.65 TYP

5.0 ± 0.1

-A-

16

9

6.4

4.4 ± 0.1

-B-

3.2

1

8

PIN #1 IDENT.

⌂ 0.2 C B A

ALL LEAD TIPS

⌂ 0.1 C

ALL LEAD TIPS

-C-

0.65 TYP

0.19 − 0.30 TYP

(0.90)

1.1 MAX TYP

0.10 ± 0.05 TYP

⊕ 0.13 Ⓜ A B Ⓢ C Ⓢ

GAGE PLANE

0.25

0°–8°

SEATING PLANE

0.6 ± 0.1

DETAIL A
TYPICAL, SCALE: 40X

SEE DETAIL A

0.09–0.20 TYP

MTC16 (REV C)
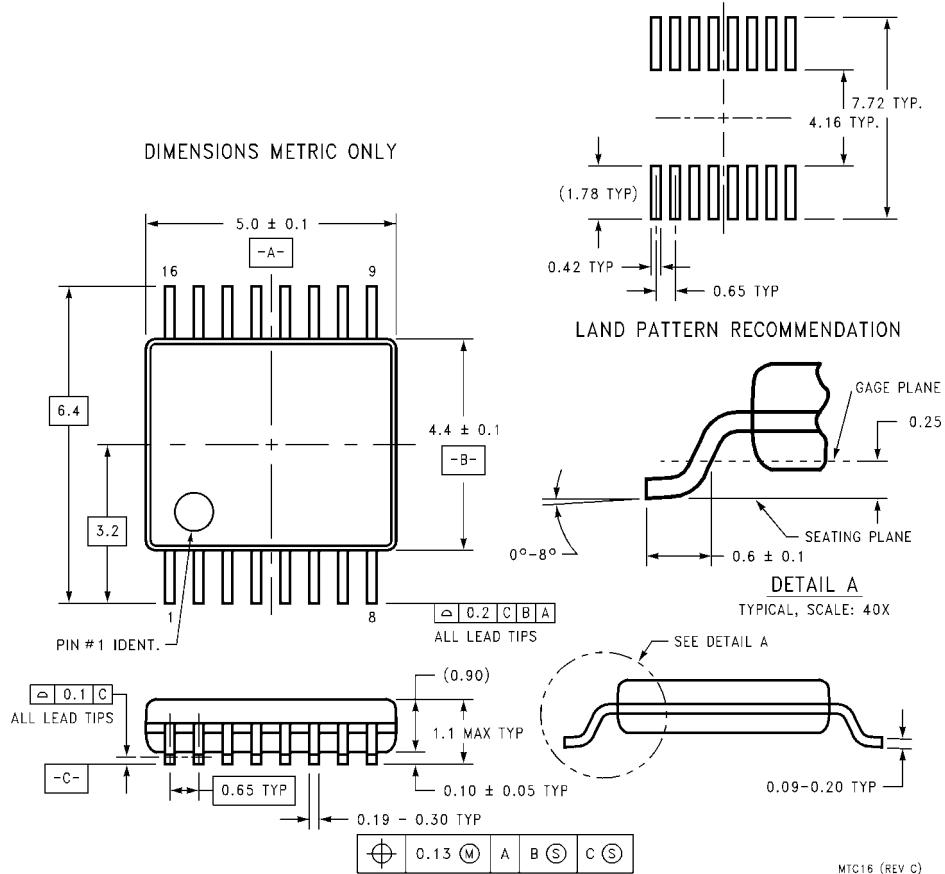
16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.740 − 0.780
(18.80 − 19.81)

0.090
(2.286)

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1 IDENT

OPTION 01

INDEX AREA

PIN NO. 1 IDENT

OPTION 02

0.065
(1.651)

0.130 ± 0.005
(3.302 ± 0.127)

0.060
(1.524) TYP

4° TYP OPTIONAL

0.145 − 0.200
(3.683 − 5.080)

0.020
(0.508) MIN

0.125 − 0.150
(3.175 − 3.810)

0.014 − 0.023
(0.356 − 0.584) TYP

0.050 ± 0.010
(1.270 ± 0.254) TYP

90° ± 4° TYP

0.030 ± 0.015
(0.762 ± 0.381)

0.100 ± 0.010
(2.540 ± 0.254) TYP

0.300 − 0.320
(7.620 − 8.128)

95° ± 5°

0.280
(7.112) MIN

$\left(0.325^{+0.040}_{-0.015}\right)$

$\left(8.255^{+1.016}_{-0.381}\right)$

0.008 − 0.016
(0.203 − 0.406) TYP

N16E (REV F)
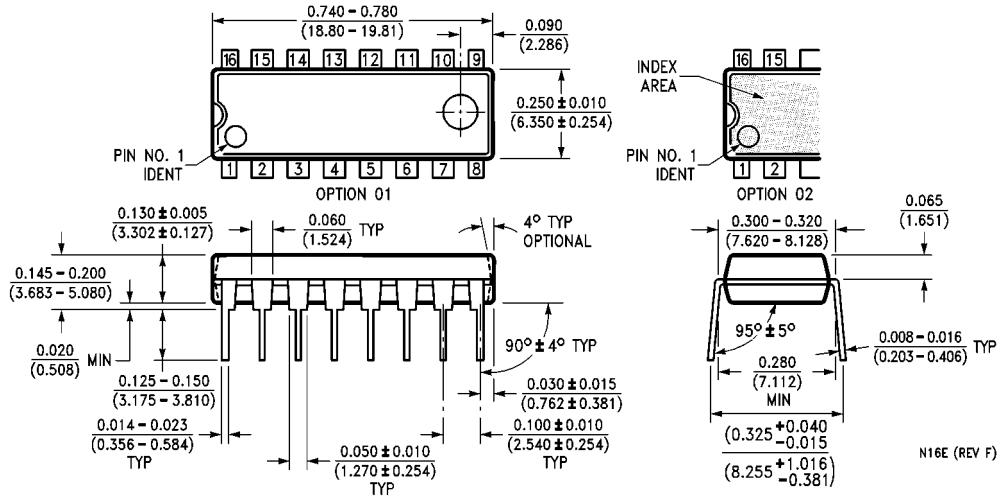
16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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