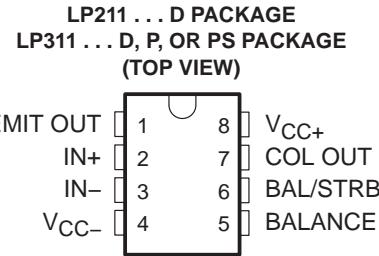


- Low Power Drain . . . 900 μ W Typical With 5-V Supply
- Operates From ± 15 V or From a Single Supply as Low as 3 V
- Output Drive Capability of 25 mA
- Emitter Output Can Swing Below Negative Supply
- Response Time . . . 1.2 μ s Typ
- Low Input Currents:
 - Offset Current . . . 2 nA Typ
 - Bias Current . . . 15 nA Typ
- Wide Common-Mode Input Range:
 - 14.5 V to 13.5 V Using ± 15 -V Supply
- Offset Balancing and Strobe Capability
- Same Pinout as LM211, LM311
- Designed To Be Interchangeable With Industry-Standard LP311



description/ordering information

The LP211 and LP311 devices are low-power versions of the industry-standard LM211 and LM311 devices. They take advantage of stable, high-value, ion-implanted resistors to perform the same function as the LM311 series, with a 30:1 reduction in power consumption, but only a 6:1 slowdown in response time. They are well suited for battery-powered applications and all other applications where fast response times are not needed. They operate over a wide range of supply voltages, from ± 18 V down to a single 3-V supply with less than 300- μ A current drain, but are still capable of driving a 25-mA load. The LP211 and LP311 are quite easy to apply free of oscillation if ordinary precautions are taken to minimize stray coupling from the output to either input or to the trim pins. In addition, offset balancing is available to minimize input offset voltage. Strobe capability also is provided to turn off the output (regardless of the inputs) by pulling the strobe pin low.

The LP211 is characterized for operation from -25°C to 85°C . The LP311 is characterized for operation from 0°C to 70°C .

ORDERING INFORMATION

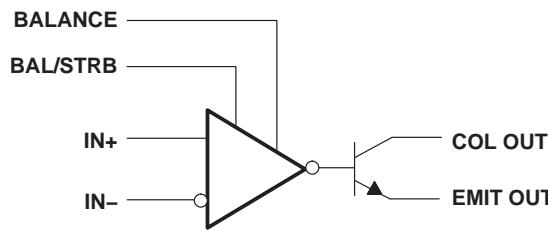
| TA | V_{IO} max AT 25°C | PACKAGE [†] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|----------------------|--------------|--------------------------|---------------------|
| -0°C to 70°C | 7.5 mV | PDIP (P) | Tube of 50 | LP311P | LP311P |
| | | SOIC (D) | Tube of 75 | LP311D | LP311 |
| | | | Reel of 2500 | LP311DR | |
| | SOP (PS) | Reel of 2000 | LP311PSR | L311 | |
| -25°C to 85°C | 7.5 mV | SOIC (D) | Tube of 75 | LP211D | LP211 |
| | | | Reel of 2500 | LP211DR | |

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

LP211, LP311
LOW-POWER DIFFERENTIAL COMPARATORS
WITH STROBES

SLCS003D – JUNE 1987 – REVISED SEPTEMBER 2003

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|----------------|
| Supply voltage (see Note 1): V_{CC+} | 18 V |
| V_{CC-} | -18 V |
| Differential input voltage, V_{ID} (see Note 2) | ± 30 V |
| Input voltage, V_I (either input, see Notes 1 and 3) | ± 15 V |
| Voltage from emitter output to V_{CC-} | 30 V |
| Voltage from collector output to V_{CC-} | 40 V |
| Voltage from collector output to emitter output | 40 V |
| Duration of output short circuit (see Note 4) | 40 V |
| Package thermal impedance, θ_{JA} (see Notes 5 and 6): D package | 97°C/W |
| P package | 85°C/W |
| PS package | 95°C/W |
| Operating virtual junction temperature, T_J | 150°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |

[†] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential input voltages are at $IN+$ with respect to $IN-$.
 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage of ± 15 V, whichever is less.
 4. The output may be shorted to ground or to either power supply.
 5. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 6. The package thermal impedance is calculated in accordance with JEDEC 51-7.

recommended operating conditions

| | | MIN | MAX | UNIT |
|----------------------------|----------------|-----------------|-----------------|------|
| ($ V_{CC\pm} \leq 15$ V) | Input voltage | $V_{CC-} + 0.5$ | $V_{CC+} - 1.5$ | V |
| $V_{CC+} - V_{CC-}$ | Supply voltage | 3.5 | 30 | V |

LP211, LP311
LOW-POWER DIFFERENTIAL COMPARATORS
WITH STROBES

SLCS003D – JUNE 1987 – REVISED SEPTEMBER 2003

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | TA | MIN | TYP† | MAX | UNIT |
|---|--|------------|-----|------|-------|------|
| V_{ID} Input offset voltage | RS < 100 k Ω , See Note 7 | 25°C | | 2 | 7.5 | mV |
| | | Full range | | | 10 | |
| V_{OL} Low-level output voltage | $V_{ID} < -10$ mV, See Note 8 | 25°C | | 0.4 | 1.5 | V |
| | $V_{CC} = 4.5$ V, $V_{ID} < -10$ mV, See Note 8 | Full range | | 0.1 | 0.4 | |
| I_{IO} Input offset current | See Note 7 | 25°C | | 2 | 25 | nA |
| | | Full range | | | 35 | |
| I_{IB} Input bias current | | 25°C | | 15 | 100 | nA |
| | | Full range | | | 150 | |
| Low-level strobe current | $V_{(strobe)} = 0.3$ V, $V_{ID} < -10$ mV, See Note 9 | 25°C | | 100 | 300 | µA |
| $I_{O(off)}$ Output off-state current | $V_{ID} > 10$ mV, $V_{CE} = 35$ V | 25°C | | 0.2 | 100 | nA |
| AVD Large-signal differential-voltage amplification | $R_L = 5$ k Ω | 25°C | 40 | 100 | | V/mV |
| I_{CC+} Supply current from V_{CC+} | $V_{ID} = -50$ mV, $R_L = \infty$ | Full range | | 150 | 300 | µA |
| I_{CC-} Supply current from V_{CC-} | $V_{ID} = 50$ mV, $R_L = \infty$ | Full range | | - 80 | - 180 | µA |

† All typical values are at $V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$.

- NOTES: 7. The offset voltages and offset currents given are the maximum values required to drive the output within 1 V of either supply with a 1-mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.
8. Voltages are with respect to EMIT OUT and V_{CC-} tied together.
9. The strobe should not be shorted to ground; it should be current driven at 100 µA to 300 µA.

switching characteristics, $V_{CC\pm} = \pm 5$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

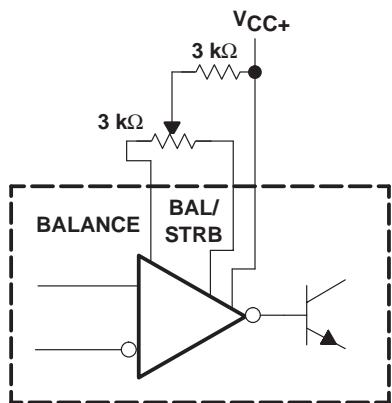
| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---------------|-----------------|-----|------|
| Response time | See Note 10 | 1.2 | µs |

NOTE 10: The response time is specified for a 100-mV input step with 5-mV overdrive.

LP211, LP311 LOW-POWER DIFFERENTIAL COMPARATORS WITH STROBES

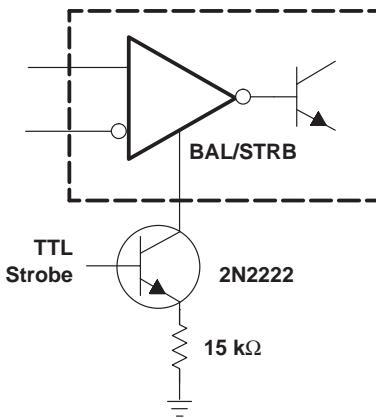
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TYPICAL APPLICATION CIRCUIT



NOTE: If offset balancing is not used, the **BALANCE** and **BAL/STRB** pins should be shorted together.

Figure 1. Offset Balancing



NOTE: Do not connect strobe pin directly to ground, because the output is turned off whenever current is pulled from the strobe pin.

Figure 2. Strobing

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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| LP211D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| LP211DE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| LP211DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| LP211DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| LP211DRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| LP211DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| LP211P | OBsolete | PDIP | P | 8 | | TBD | Call TI | Call TI |
| LP311D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| LP311DE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| LP311DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| LP311DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| LP311DRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| LP311DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| LP311P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| LP311PE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| LP311PWLE | OBsolete | TSSOP | PW | 8 | | TBD | Call TI | Call TI |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

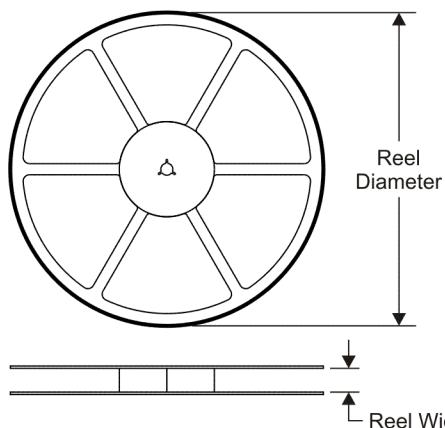
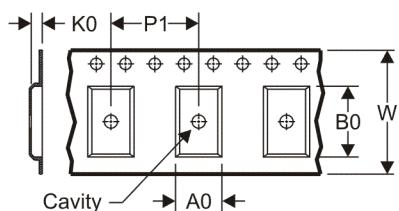
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

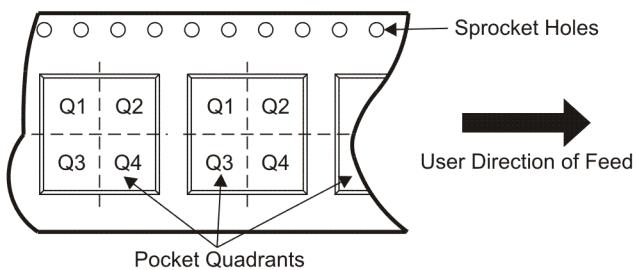
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP211DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LP311DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

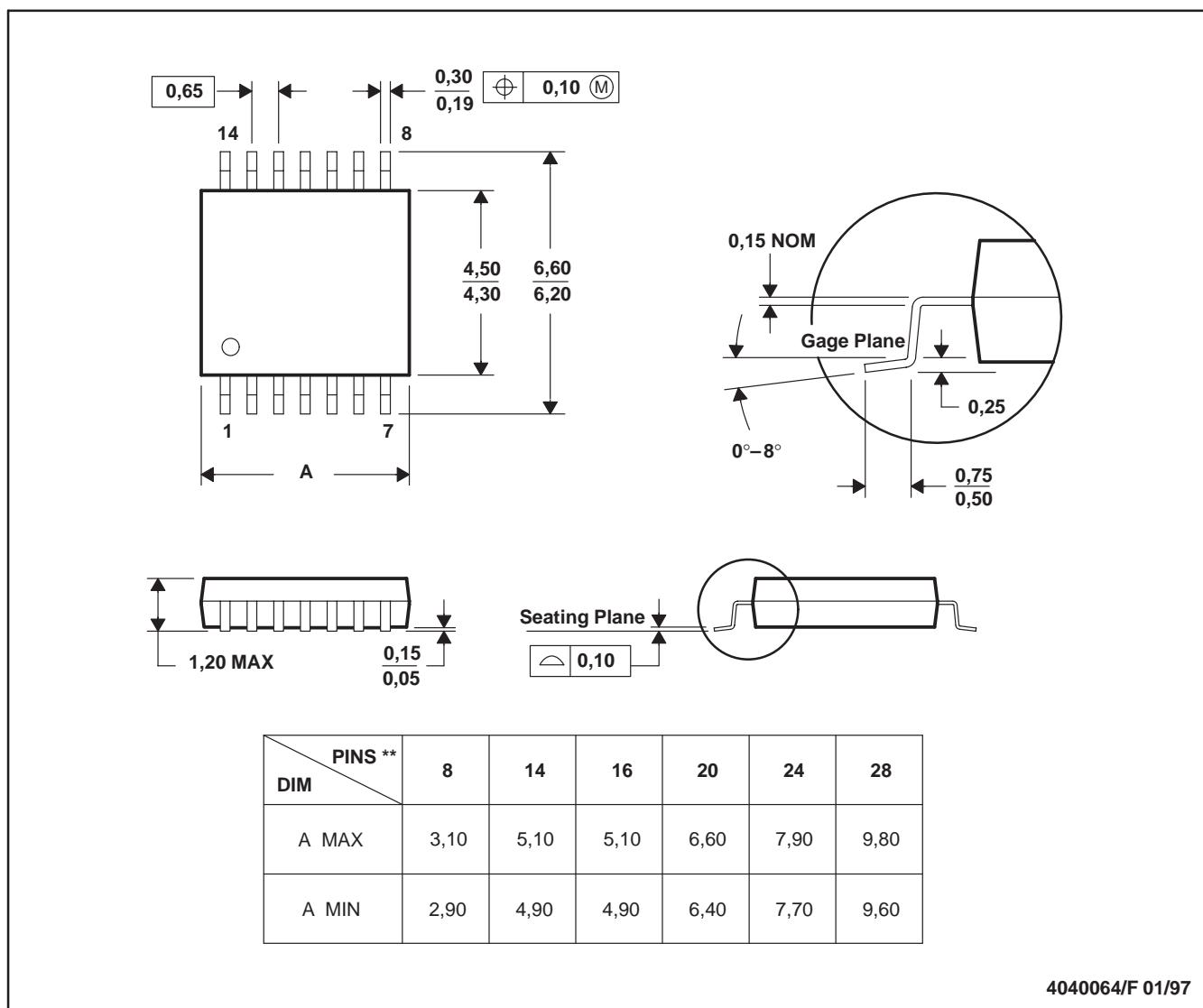
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------|--------------|-----------------|------|------|-------------|------------|-------------|
| LP211DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| LP311DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

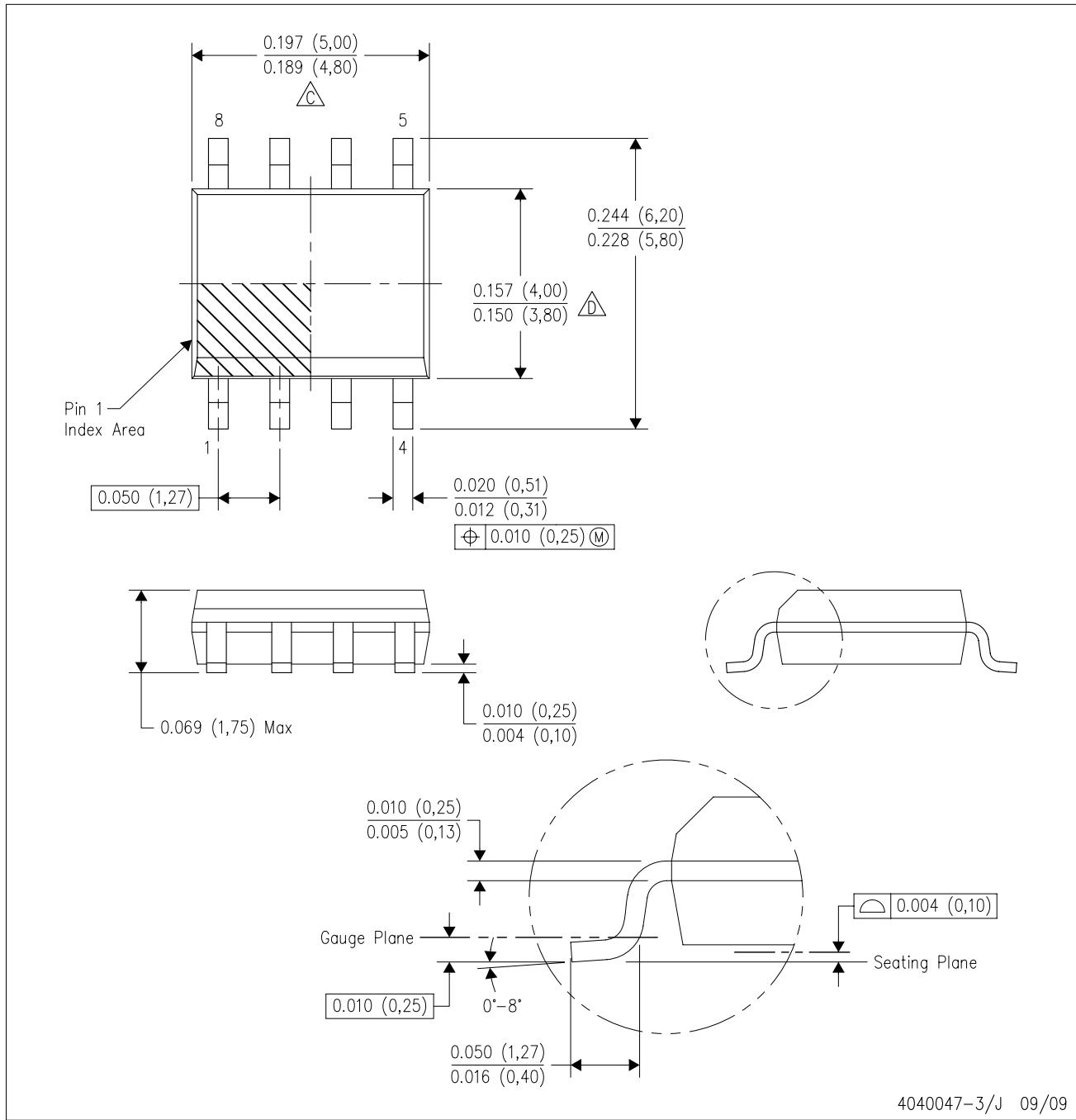
14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-153

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

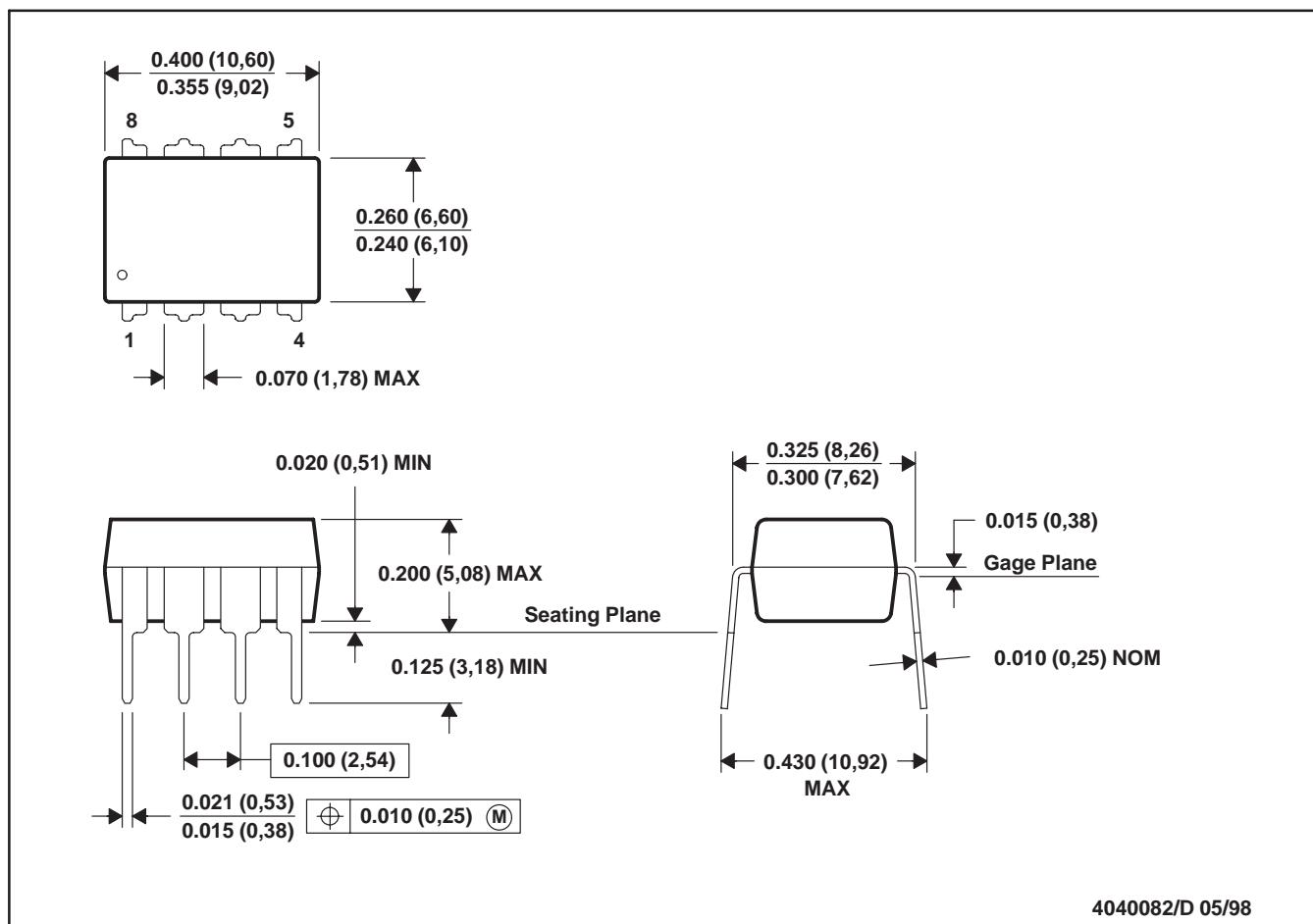
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

△D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AA.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

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