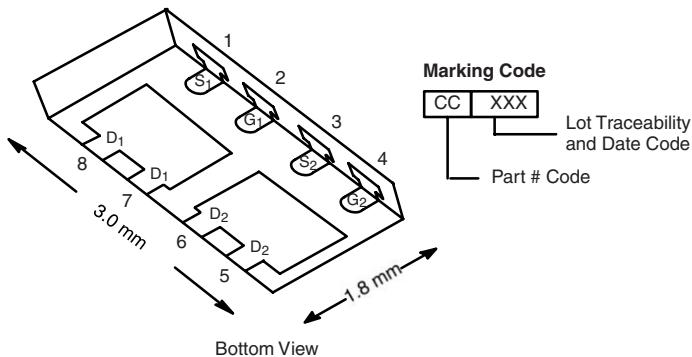


Dual N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
40	0.112 at $V_{GS} = 10$ V	6 ^a	2.2 nC
	0.171 at $V_{GS} = 4.5$ V	4.9	

PowerPAK ChipFET Dual



Ordering Information: Si5944DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

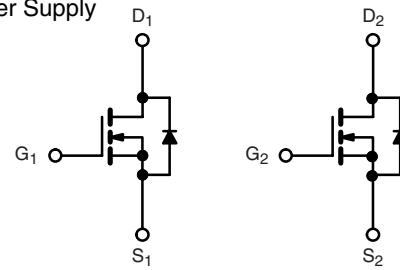


FEATURES

- Halogen-free
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® ChipFET® Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.8 mm Profile

APPLICATIONS

- DC-DC Power Supply



N-Channel MOSFET

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	6 ^a	A
		4.87	
		3.28 ^{b, c}	
		2.63 ^{b, c}	
Pulsed Drain Current	I_{DM}	10	
Continuous Source-Drain Diode Current	I_S	8.33	
		1.68 ^{b, c}	
Single Pulse Avalanche Current	I_{AS}	5	mJ
		E_{AS}	
Avalanche Energy	P_D	1.25	
		10	
		6.4	
		2.0 ^{b, c}	
Maximum Power Dissipation		1.3 ^{b, c}	W
		10	
		6.4	
		2.0 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	$t \leq 5$ s	R_{thJA}	52	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	15	18

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 5$ s.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 110 °C/W.

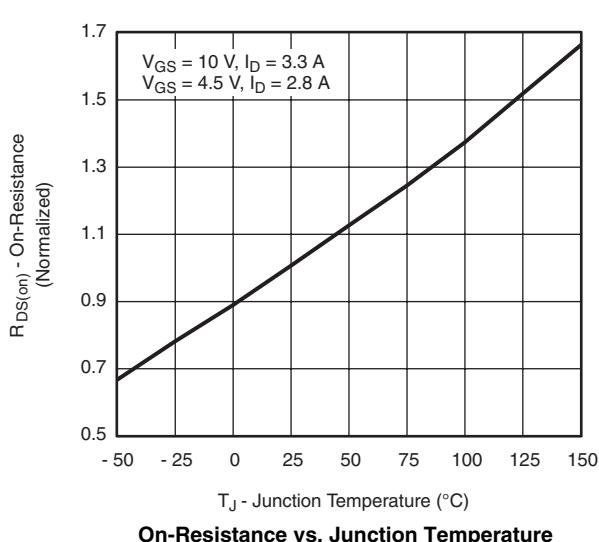
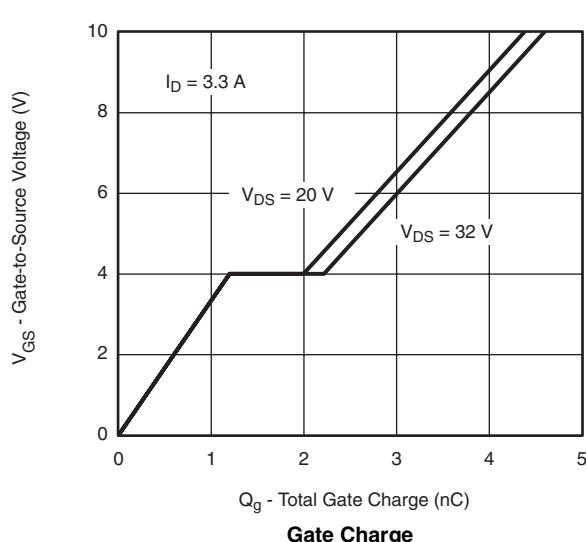
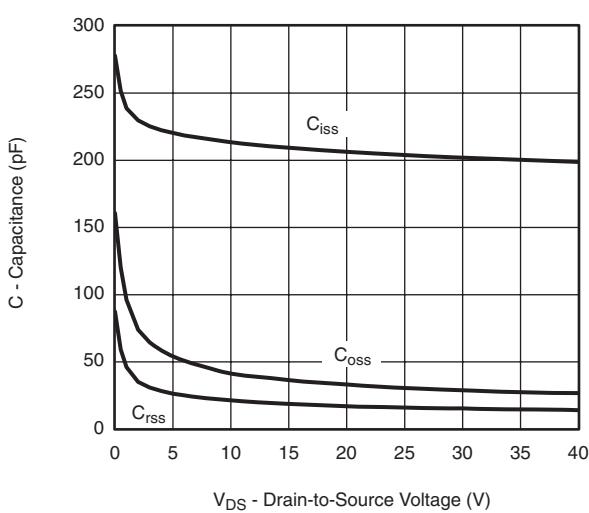
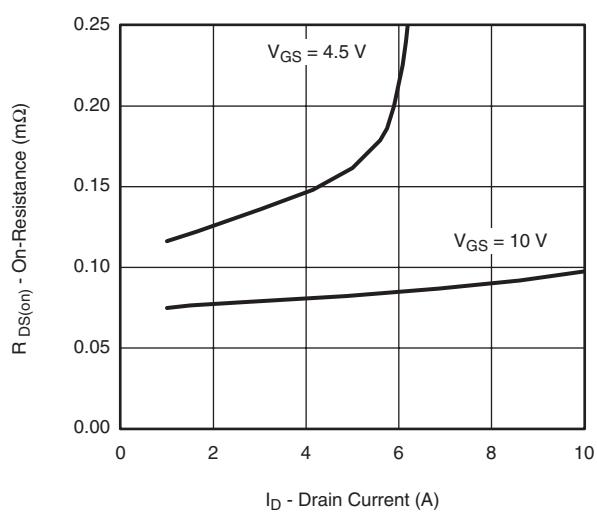
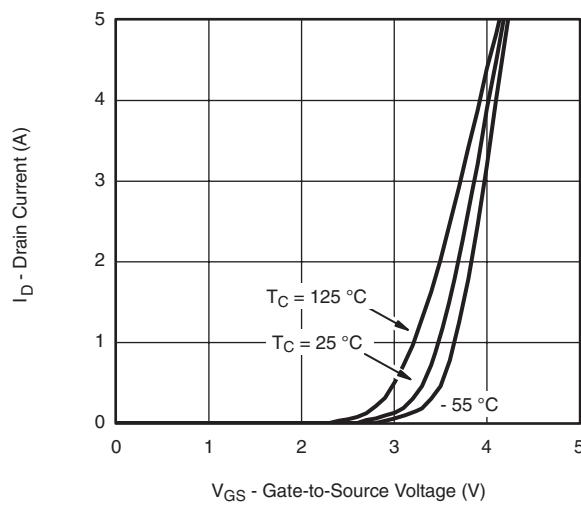
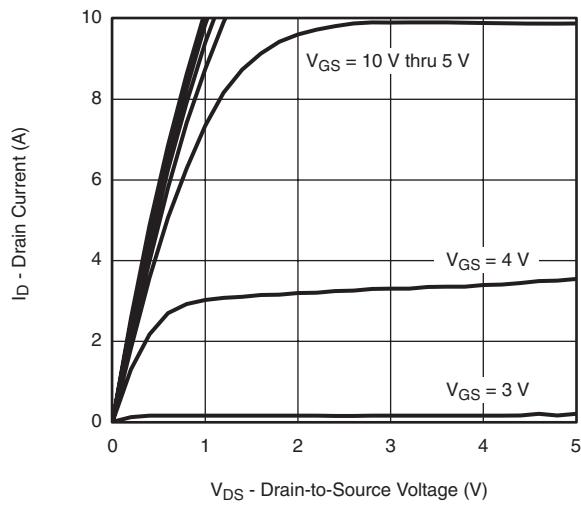
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

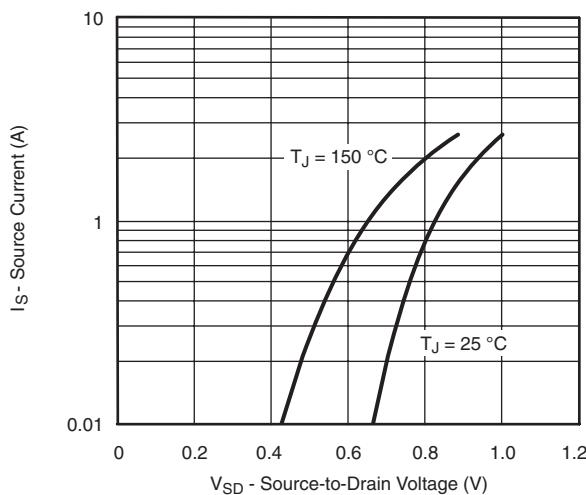
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		32.6		$\text{mV}/^\circ\text{C}$
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			- 4.7		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	1		3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40 \text{ V}$, $V_{GS} = 0 \text{ V}$			- 1	μA
		$V_{DS} = 40 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \leq 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	10			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 3.3 \text{ A}$		0.093	0.112	Ω
		$V_{GS} = 4.5 \text{ V}$, $I_D = 2.6 \text{ A}$		0.137	0.165	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 20 \text{ V}$, $I_D = 3.3 \text{ A}$		6.88		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 20 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		210		pF
Output Capacitance	C_{oss}			33		
Reverse Transfer Capacitance	C_{rss}			17		
Total Gate Charge	Q_g	$V_{DS} = 20 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 3.3 \text{ A}$		4.4	6.6	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = 20 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 3.3 \text{ A}$		2.2	3.3	
Gate-Drain Charge	Q_{gd}			1.2		
Gate Resistance	R_g		$f = 1 \text{ MHz}$		0.8	
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 20 \text{ V}$, $R_L = 7.6 \Omega$ $I_D \geq 2.63 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$		2.7	4.1	Ω
Rise Time	t_r			4	6	ns
Turn-Off Delay Time	$t_{d(\text{off})}$			30	45	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(\text{on})}$			6	9	
Rise Time	t_r			12	18	
Turn-Off Delay Time	$t_{d(\text{off})}$			80	120	
Fall Time	t_f			6	9	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			8.33	A
Pulse Diode Forward Current	I_{SM}				10	
Body Diode Voltage	V_{SD}	$I_S = 3.0 \text{ A}$, $V_{GS} = 0 \text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 3.0 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$		22	33	ns
Body Diode Reverse Recovery Charge	Q_{rr}			18	27	nC
Reverse Recovery Fall Time	t_a			19		ns
Reverse Recovery Rise Time	t_b			3		

Notes:

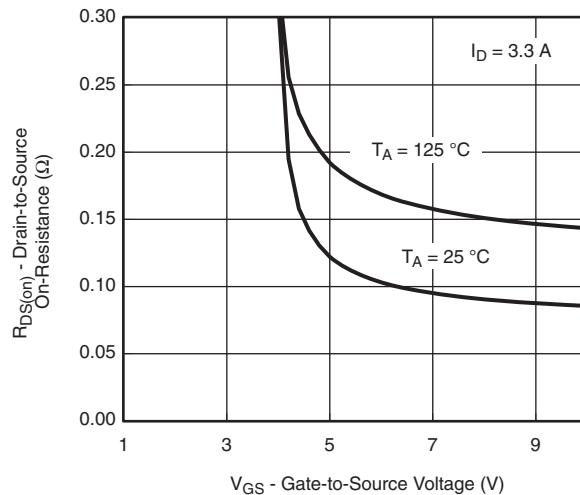
a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

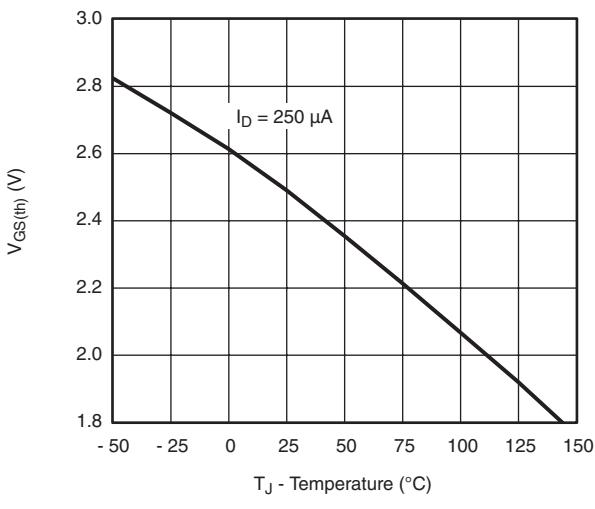
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


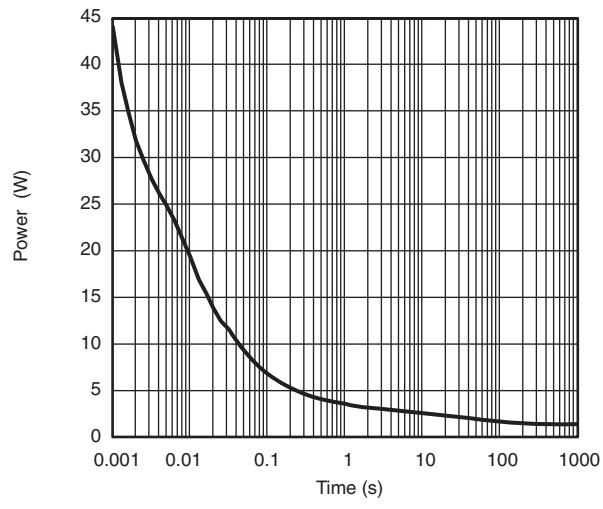
Source-Drain Diode Forward Voltage



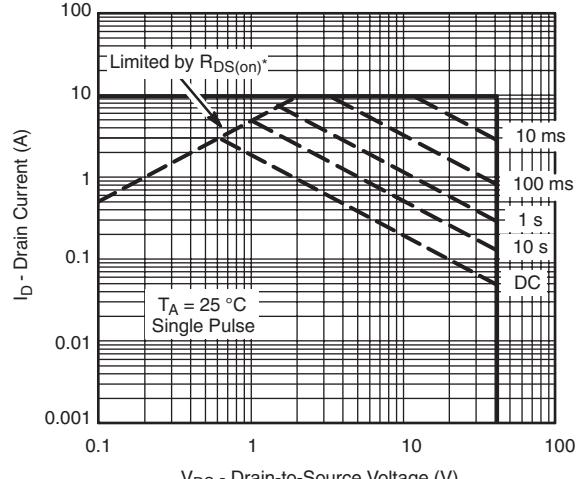
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

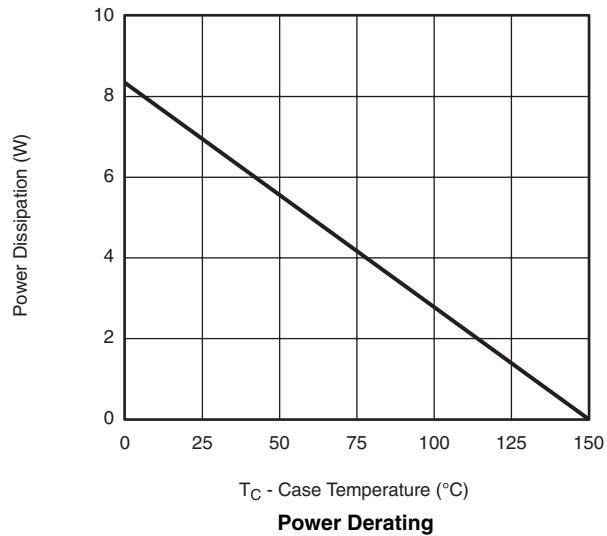
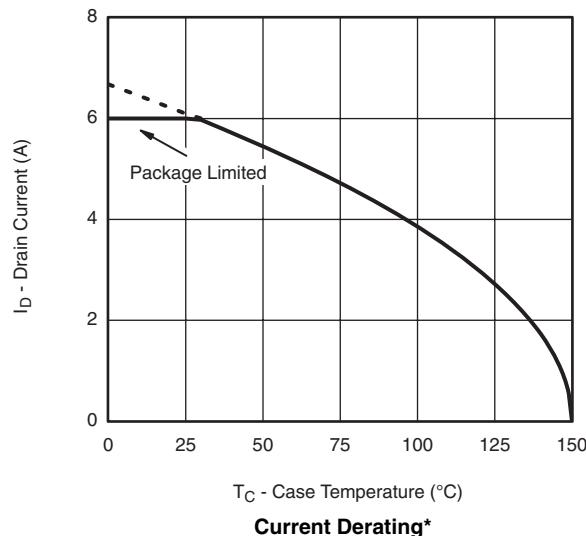


Single Pulse Power, Junction-to-Ambient

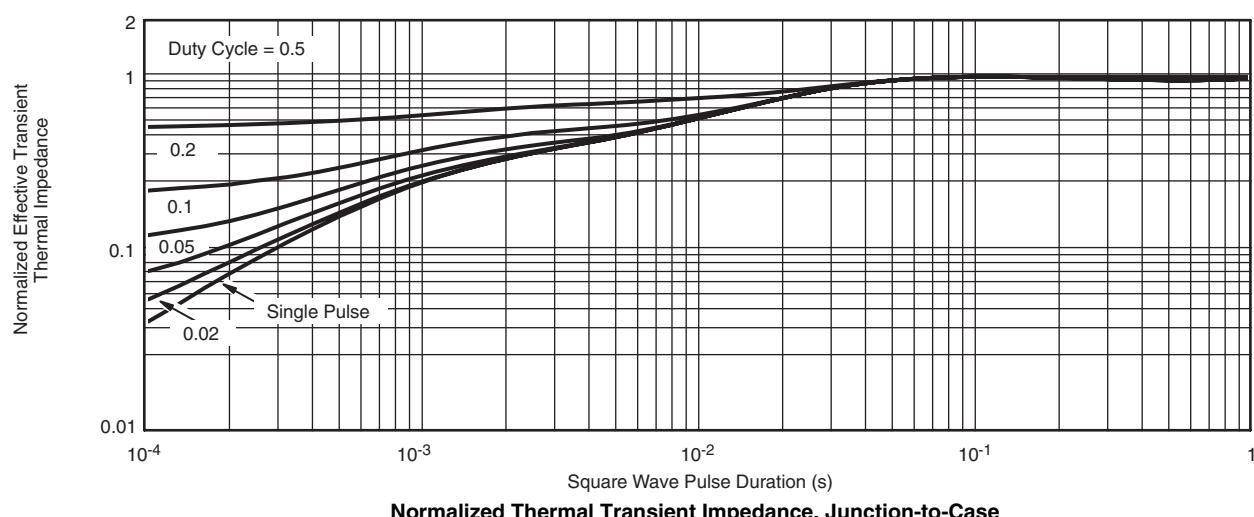
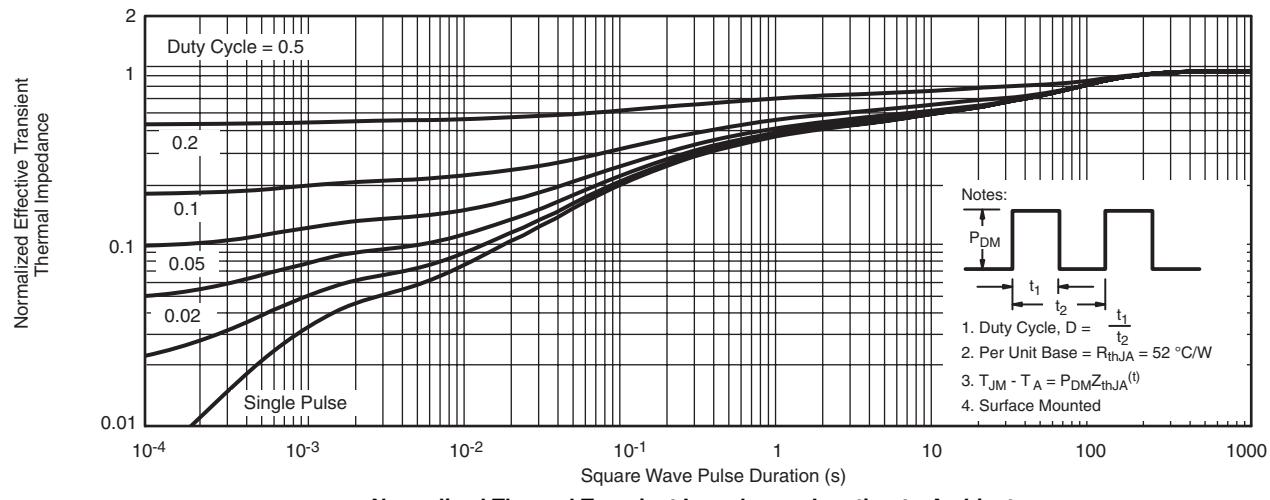


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

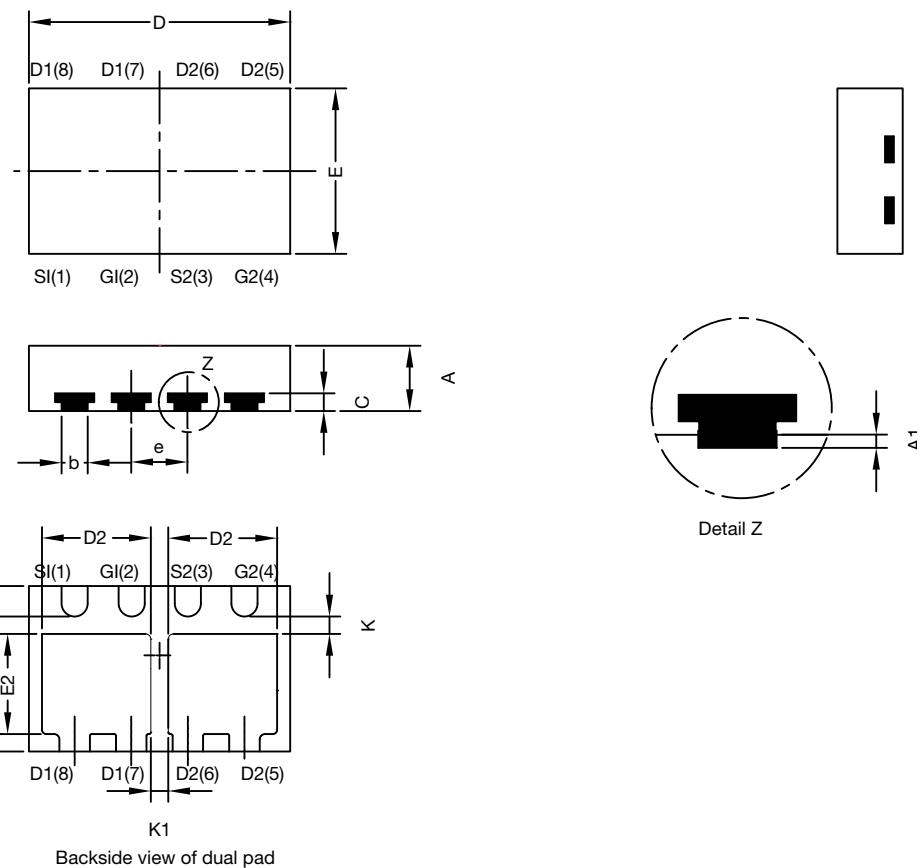
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

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PowerPAK® ChipFET® Dual PAD



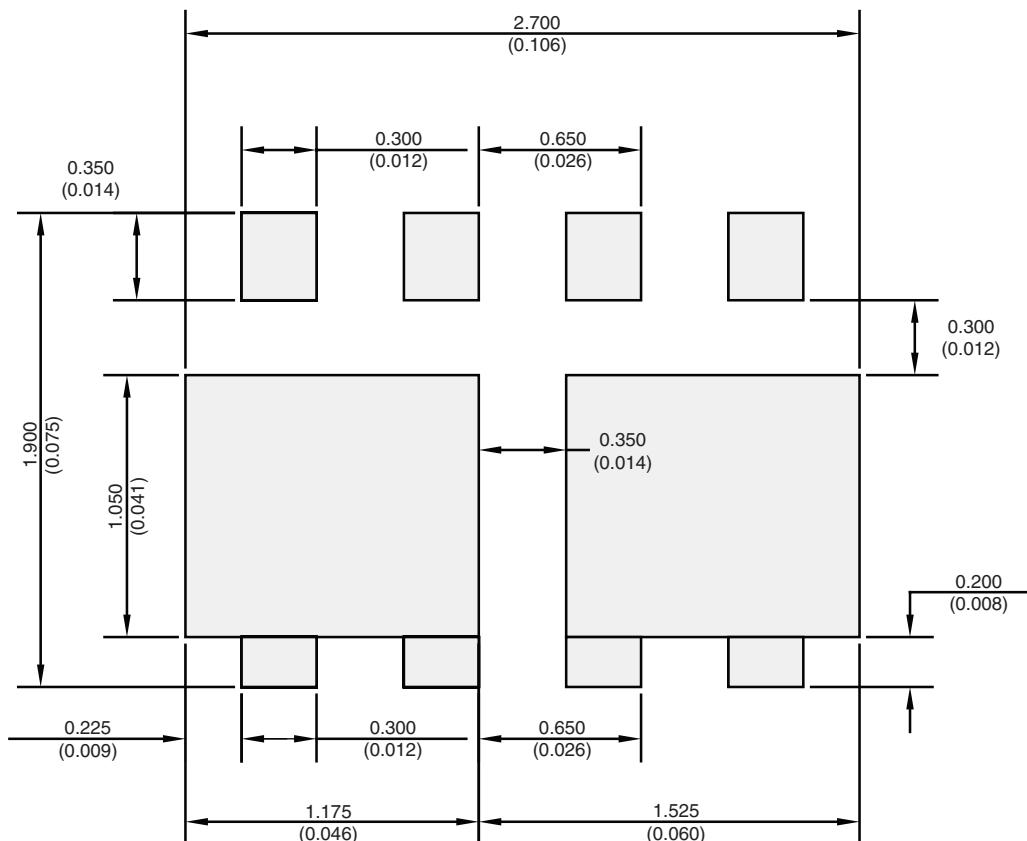
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D2	1.07	1.20	1.32	0.042	0.047	0.062
E	1.82	1.90	1.98	0.072	0.075	0.078
E2	0.92	1.05	1.17	0.036	0.041	0.046
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.20	-	-	0.008	-	-
K1	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016

C14-0307-Rev. D, 05-May-14
DWG: 5940

Note

- Millimeters will govern

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Dual



Recommended Minimum Pads
Dimensions in mm/(Inches)

Note: This is Flipped Mirror Image
Pin #1 Location is Top Left Corner

APPLICATION NOTE

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