4.5-V TO 18-V INPUT VOLTAGE, 6-A/3.5-A DUAL SYNCHRONOUS STEP-DOWN CONVERTER

Check for Samples: TPS65276

FEATURES

- **4.5-V to 18-V Wide Input Voltage Range**
- **Programmable Slew Rate Control for Output Voltage Transition**
- **Up to 6-A Maximum Continuous Output Current in Buck 1 and 3.5-A in Buck 2**
- **Pulse Skipping Mode to Achieve High Efficiency in Light Load**
- **Adjustable Switching Frequency 200 kHz - 1.6 MHz Set by External Resistor**
- **Dedicated Enable and Soft-Start for Each Buck**
- **Peak Current-Mode Control with Simple Compensation Circuit**
- **Cycle-by-Cycle Over Current Protection**

- **180° Out-of-Phase Operation to Reduce Input Capacitance and Power Supply Induced Noise**
- **Over Temperature Protection**
- **Available in 32-Pin Thermally Enhanced HTSSOP (DAP) and 36-Pin QFN 6-mm x 6-mm (RHH) Packages**

APPLICATIONS

- **DTV**
- **TCON**
- **BDVD**
- **Set Top Boxes**
- **Tablet PC**

DESCRIPTION/ORDERING INFORMATION

TPS65276 is a monolithic dual synchronous buck converter with wide 4.5V to 18V operating input voltage range that encompassed most intermediate bus voltage operating off 5-, 9-, 12- or 15-V power bus or battery. The converter with constant frequency peak current mode control is designed to simplify its application while giving the designers options to optimize their usage according to the target applications.

The switching frequency of the converters can be adjustable from 200 KHz to 1.6MHz with an external resistor. Two converters have clock signal with 180° out-of-phase.

TPS65276 features dedicated enable pin when I^{2}C interface is not used. Independent soft-start pin provides flexibility in power up programmability. Constant frequency peak current mode control simplifies the compensation and provides fast transient response. Cycle-by-cycle over current protection and hiccup mode operation limit MOSFET power dissipation in short circuit or over loading fault conditions. Low side reverse over current protection also prevents excessive sinking current from damaging the converter.

TPS65276 also features a light load pulse skipping mode (PSM) that can be controlled by I^{2}C or MODE pin configuration. The PSM mode allows a power loss reduction on the input power supplied to the system to achieve high efficiency at light loading.

The TPS65276 is available in a 32-pin thermally enhanced HTSSOP (DAP) package and 36-pin QFN 6-mm x 6-mm (RHH) package.

ORDERING INFORMATION[1]

T$_A$	PACKAGE[2]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	32-pin HTSSOP (DAP)	TPS65276DAPT	TPS65276
	36-pin QFN (RHH)	TPS65276RHHT	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TYPICAL APPLICATION
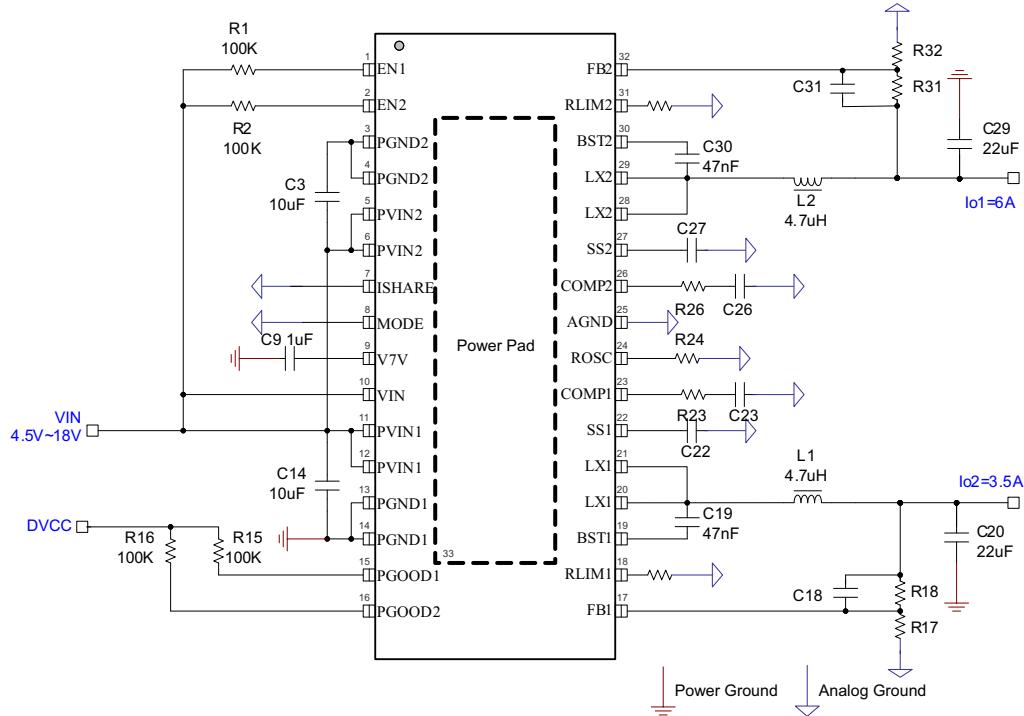
Figure 1. Dual Mode Operation to Deliver 6 A at Buck 1 and 3.5 A at Buck 2

Product Folder Links: *TPS65276*
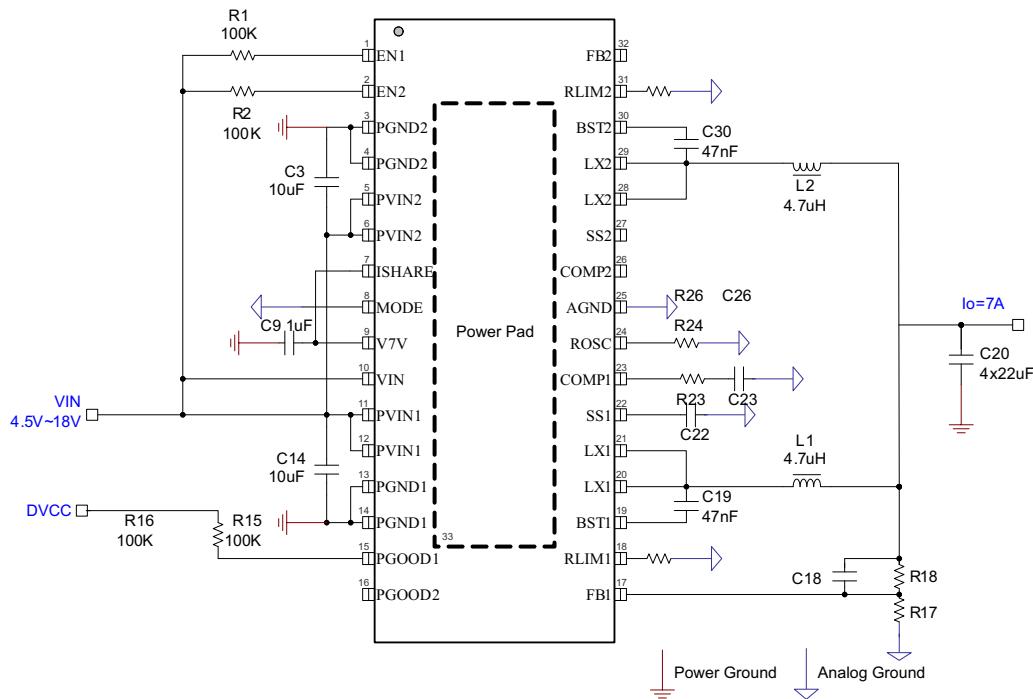
Figure 2. Share Mode Operation to Deliver 7 A

FUNCTIONAL BLOCK DIAGRAM
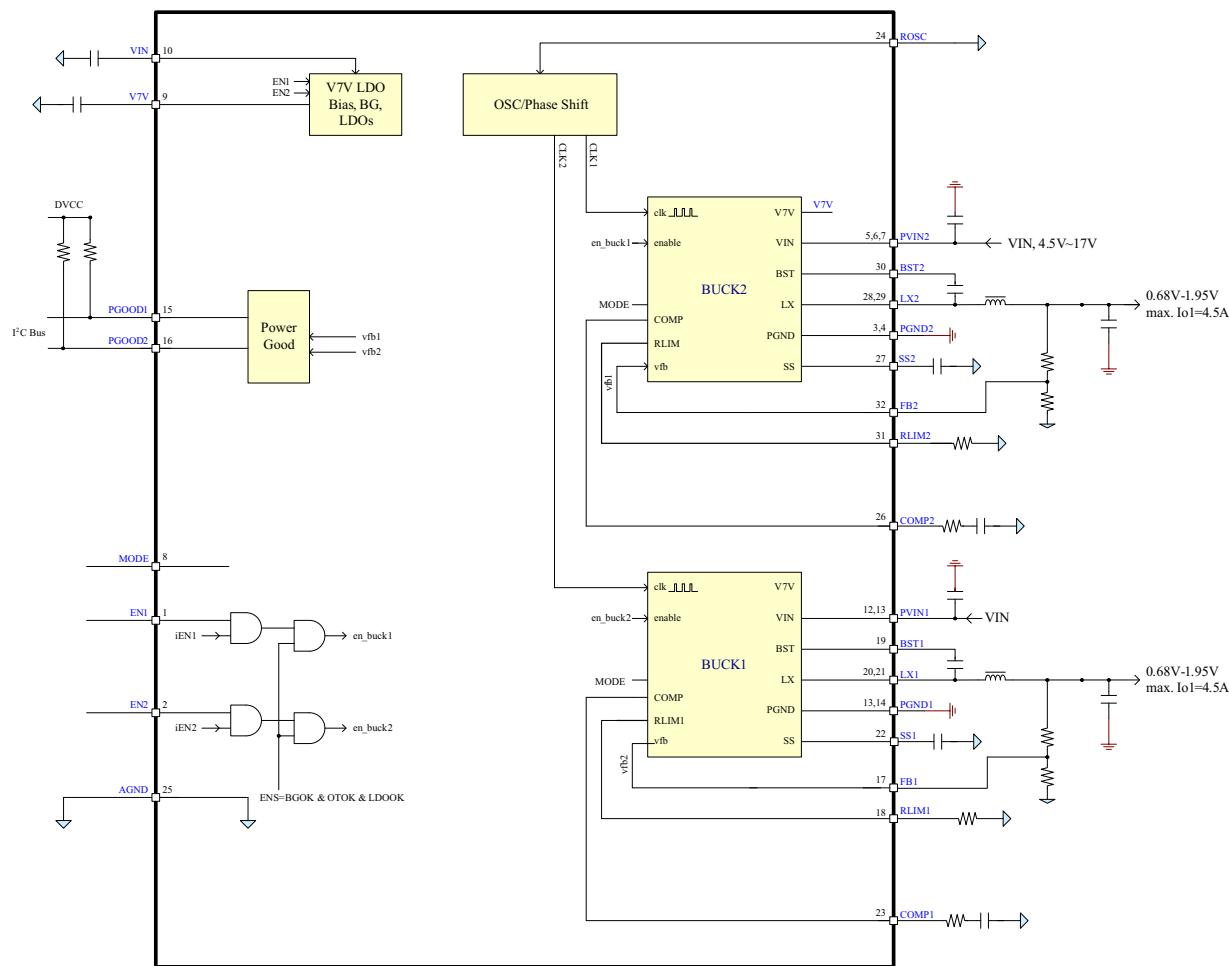
PIN OUT

DAP PACKAGE
(TOP VIEW)

RHH PACKAGE
(TOP VIEW)

Pin	Name
1	PVIN2
2	PVIN2
3	ISHARE
4	MODE
5	V7V
6	VIN
7	PVIN1
8	PVIN1
9	PGND1
10	PGND1
11	PGND1
12	PGOOD1
13	PGOOD2
14	FB1
15	RLIM1
16	BST1
17	LX1
18	LX1
19	LX1
20	SS1
21	COMP1
22	ROSC
23	AGND
24	COMP2
25	SS2
26	LX2
27	LX2
28	LX2
29	BST2
30	RLIM2
31	FB2
32	EN1
33	EN2
34	PGND2
35	PGND2
36	PGND2

Thermal Pad
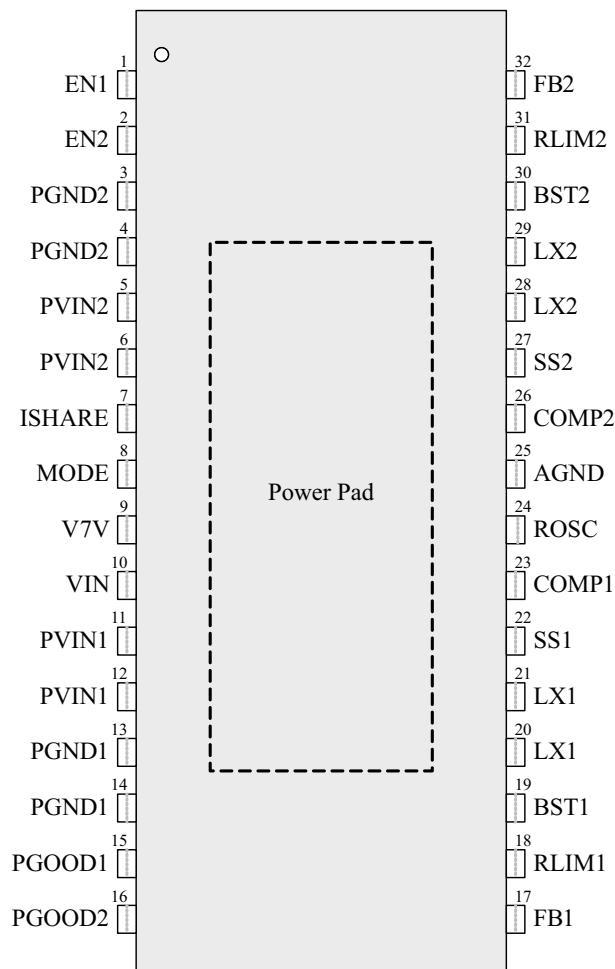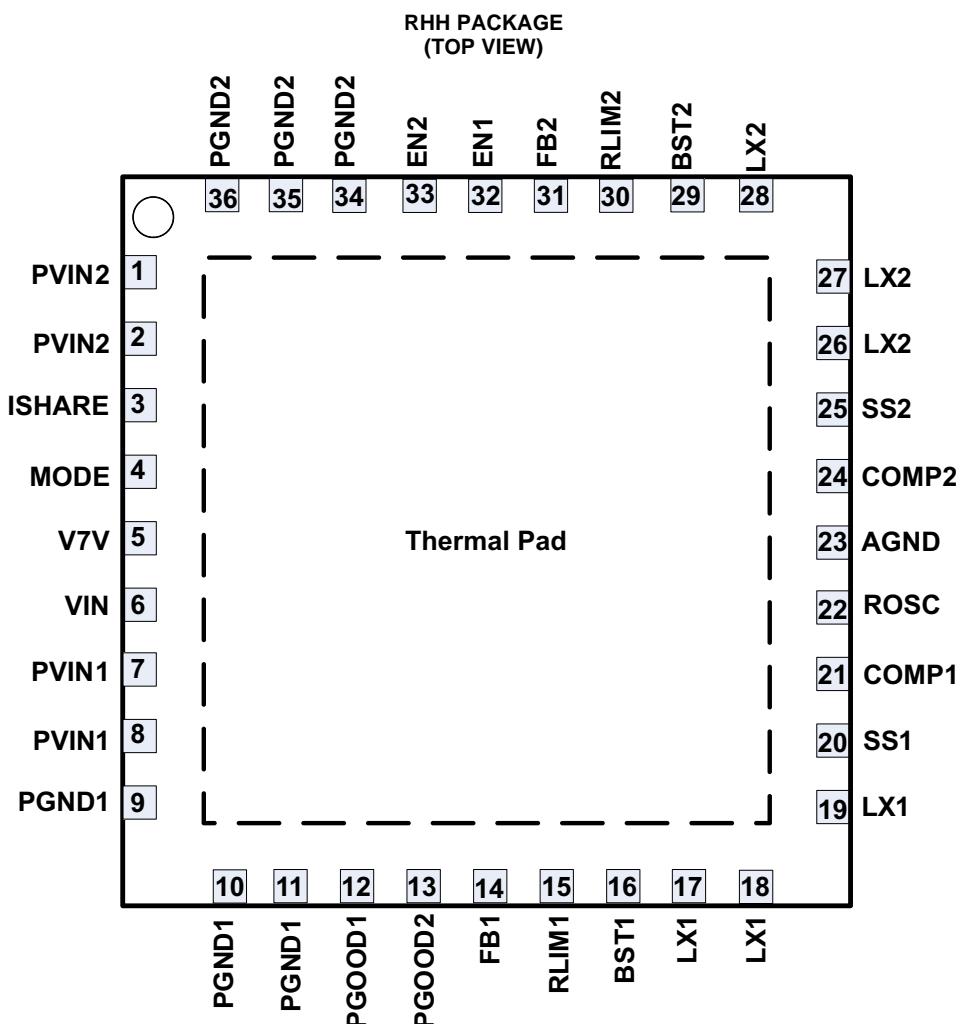
TERMINAL FUNCTIONS

NAME	NO. (HTSSOP)	NO. (QFN)	DESCRIPTION
EN1, EN2	1, 2	32, 33	Enable pin. Adjust the input under-voltage lockout with two resistors.
PGND2	3, 4	34, 35, 36	Power ground of Buck 2, place the input capacitor's ground pin as close as possible to this pin.
PVIN2	5, 6	1, 2	Power input. Input power supply to the power switches of the power converter 2.
ISHARE	7	3	Logic pin to configure current share mode, tie to high to parallel two buck converters, in current share mode, buck 1 will be used; tie to low to run in separate mode.
MODE	8	4	Operation mode control pin. Connect this pin to ground to choose forced PWM mode without current sharing; leave the pin open for pulse skipping mode (PSM) operation at light load condition; connect this pin to V7V to choose forced PWM mode and current sharing with paralleling two bucks.
V7V	9	5	Internal low-drop linear regulator (LDO) output to power internal driver and control circuits. Decouple this pin to power ground with a minimum 1-µF ceramic capacitor. Output regulates to typical 6.3 V for optimal conduction on-resistances of internal power MOSFETs. In PCB design, the power ground and analog ground should have one-point common connection at the (-) terminal of V7V bypass capacitor. If VIN is lower than 6.3 V, V7V will be slightly lower than VIN.
VIN	10	6	Power supply of the internal LDO and controllers
PVIN1	11, 12	7, 8	Power input. Input power supply to the power switches of the power converter 1.
PGND1	13, 14	9, 10, 11	Power ground of Buck 1, place the input capacitor's ground pin as close as possible to this pin.
PGOOD1	15	12	Power Good pin for Buck1, open drain output, when output is within range, output high impedance, a 100-kΩ resistor is recommended to connect to this pin.
PGOOD2	16	13	Power Good pin for Buck2, open drain output, when output is within range, output high impedance, a 100k Ohm resistor is recommended to connect to this pin.
FB1	17	14	Feedback sensing pin for the external feedback resistors in Buck 1. Before I^{2}C controlled VID selection is enabled, an external resistor divider connects to this pin to pre-set the output voltage.
RLIM1	18	15	Current limit threshold set pin for Buck1, connect a resistor between this pin to GND to set the OCP.
BST1	19	16	Add a bootstrap capacitor between BST1 and LX1. The voltage on this capacitor carries the gate drive voltage for the high-side MOSFET.
LX1	20, 21	17, 18, 19	Switching node of Buck 1
SS1	22, 27	20, 25	Soft-start and voltage tracking in Buck 1. An external capacitor connected to this pin sets the internal voltage reference rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing. In current sharing application, this pin serves as the soft-start pin.
COMP1	23	21	Error amplifier output and loop compensation pin for Buck 1. Connect frequency compensation to this pin; In current sharing application, this pin serves as the compensation pin.
ROSC	24	22	Oscillator frequency programmable pin. Connect an external resistor to set the switching frequency. When connected to an external clock, the internal oscillator synchronizes to the external clock.
AGND	25	23	Analog ground of the controllers
COMP2	26	24	Error amplifier output and loop compensation pin for Buck 2. Connect frequency compensation to this pin. In current sharing application, connect this pin to ground.
SS2	27	25	Soft-start and voltage tracking in Buck 2. An external capacitor connected to this pin sets the internal voltage reference rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and power sequencing. In current sharing application, connect this pin to ground.
LX2	28, 29	26, 27, 28	Switching nodes

TERMINAL FUNCTIONS (continued)

NAME	NO. (HTSSOP)	NO. (QFN)	DESCRIPTION
BST2	30	29	Add a bootstrap capacitor between BST2 and LX2. The voltage on this capacitor carries the gate drive voltage for the high-side MOSFET of Buck 2.
RLIM2	31	30	Current limit threshold set pin for Buck2, connect a resistor between this pin to GND to set the OCP.
FB2	32	31	Feedback sensing pin for the external feedback resistors in Buck 2. Before I^{2}C controlled VID selection is enabled, an external resistor divider connects to this pin to pre-set the output voltage.
Exposed Thermal Pad	33	37	Exposed thermal pad of the package. Connect to the power ground. Always solder thermal pad to the board, and have as many vias as possible on the PCB to enhance power dissipation. There is no electric signal down bonded to the thermal pad inside the IC package.

ABSOLUTE MAXIMUM RATINGS [1]

over operating free-air temperature range (unless otherwise noted)

	Voltage range at VIN, PVIN1,PVIN2	–0.3 to 20	V
	Voltage range at LX1, LX2 (maximum withstand voltage transient < 20 ns)	–4.5 to 20	V
	Voltage at BST1, BST2, referenced to LX1, LX2 pin	–0.3 to 7	V
	Voltage at V7V, EN1, EN2, RLIM1, RLIM2, PGOOD1, PGOOD2, MODE, ISHARE	–0.3 to 7	V
	Voltage at SS1, SS2, FB1, FB2, COMP1, COMP2	–0.3 to 3	V
	Voltage at ROSC	–0.3 to 7	
	Voltage at AGND, PGND1, PGND2	–0.3 to 0.3	V
T_J	Operating virtual junction temperature range	–40 to 125	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC		TPS65276		UNITS
		DAP	RHH	
		32 PINS	36 PINS	
θ_{JA}	Junction-to-ambient thermal resistance[1]	35	30.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[2]	17.7	18.8	
θ_{JB}	Junction-to-board thermal resistance[3]	19	6	
ψ_{JT}	Junction-to-top characterization parameter[4]	0.5	0.2	
ψ_{JB}	Junction-to-board characterization parameter[5]	18.9	6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[6]	1.3	0.7	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		18	V
T_A	Ambient temperature	−40		85	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model (HBM)	1000		V
Charge device model (CDM)	500		V

ELECTRICAL CHARACTERISTICS

T_J = 25°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input Voltage range	VIN1 and VIN2	4.5		18	V
IDD_{SDN}	Shutdown supply current	EN1 = EN2 = low		10		µA
IDD_{Q_NSW}	Switching quiescent current with no load at DCDC output	EN1 = EN2 = 3.3 V Without bucks switching		1.2		mA
IDD_{Q_SW}	Switching quiescent current with no load at DCDC output, Buck switching	EN1 = EN2 = 3.3 V With bucks switching		10		mA
UVLO	V_{IN} under voltage lockout	Rising V_{IN}		4.25	4.50	V
		Falling V_{IN}	3.5	3.75		
		Hysteresis		0.5		
V_{7V}	6.3 V LDO	V_{7V} load current = 0 A, V_{IN} = 12 V	6.10	6.3	6.5	V
I_{OCP_7V}	Current limit of V7V LDO			200		mA
ENABLE						
V_{ENR}	Enable threshold			1.21	1.26	V
V_{ENF}	Enable threshold		1.10	1.17		V
I_{ENR}	Enable Input current	EN = 1 V		3		µA
I_{ENF}	Enable hysteresis current	EN = 1.5 V		3		µA
OSCILLATOR						
F_{SW}	Switching frequency		200		1600	kHz
		R_{OSC} = 100 kΩ (1%)	340	400	460	
T_{SYNC_w}	Clock sync minimum pulse width			20		ns
V_{SYNC_HI}	Clock sync high threshold				2	V
V_{SYNC_LO}	Clock sync low threshold		0.8			V
V_{SYNC_D}	Clock falling edge to LX rising edge delay			66		ns
F_{SYNC}	Clock sync frequency range		200		1600	kHz

ELECTRICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK 1, BUCK 2 CONVERTERS						
$V_{ref(min)}$	Voltage reference	0 A < I_{OUT1} < 6 A, 0 A < I_{OUT2} < 3.5 A	0.594	0.6	0.606	V
$V_{LINEREG3}$	Line regulation-DC	I_{OUT} = 2 A		0.5		%/V
$V_{LOADREG3}$	Load regulation-DC	I_{OUT} = (10-90%) x I_{OUT_max}		0.5		%/A
G_{m_EA3}	Error amplifier trans-conductance	-2 µA < I_{COMP} < 2 µA		1350		µs
G_{m_SRC3}	COMP voltage to inductor current Gm	I_{LX} = 0.5 A		10		A/V
I_{SSx}	Soft-start pin charging current	SS1, SS2		6		µA
I_{LIMIT1}	Buck 1 peak inductor current limit			8		A
I_{LIMIT2}	Buck 2 peak inductor current limit			5		A
$I_{LIMITLSx}$	Low side sinking current limit			-2.6		A
R_{dsonx_HS}	On resistance of high side FET	V7V = 6.3 V		31		mΩ
R_{dsonx_LS}	On resistance of low side FET	V_{IN} = 12 V		23		mΩ
T_{minon}	Minimum on time			94		ns
V_{bootUV}	Boot-LX UVLO			2.1	3	V
$T_{hiccupwait}$	Hiccup wait time			512		cycles
T_{hiccup_re}	Hiccup time before re-start			16384		cycles
PGOOD						
V_{PGOOD}	PGOOD trip levels	Feedback lower voltage rising (with respect to 0.6 V)		94		%
		Feedback lower voltage falling (with respect to 0.6 V)		92.5		
		Feedback upper voltage rising (with respect to 0.6 V)		107.5		
		Feedback upper voltage falling (with respect to 0.6 V)		105.5		
THERMAL SHUTDOWN						
T_{TRIP}	Thermal protection trip point	Rising temperature		160		°C
T_{HYST}	Thermal protection hysteresis			20		°C

Product Folder Links: *TPS65276*

TYPICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)
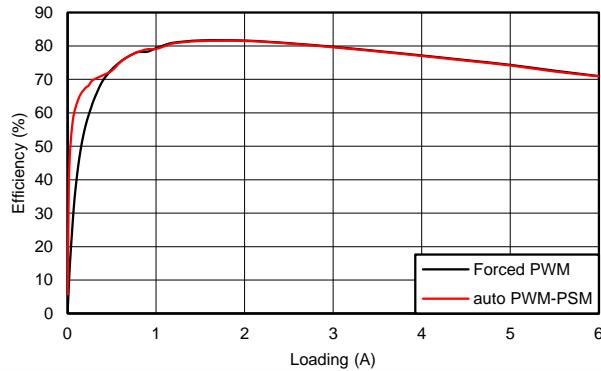
Figure 3. 0.8-V Efficiency
V_{IN} = 12 V, V_{OUT} = 0.8 V
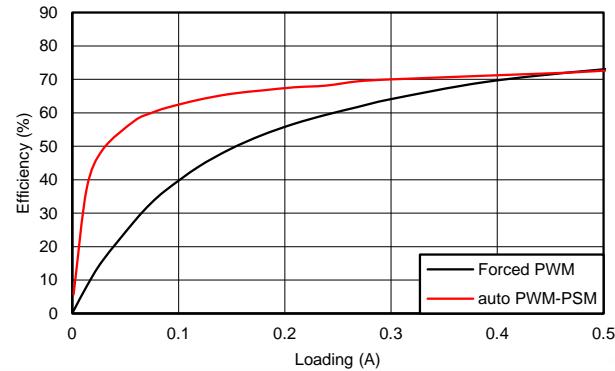
Figure 4. 0.8-V Efficiency, Light Load
V_{IN} = 12 V, V_{OUT} = 0.8 V
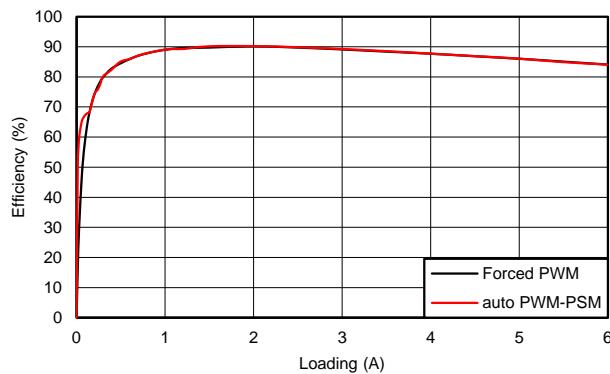
Figure 5. 1.8-V Efficiency
V_{IN} = 12 V, V_{OUT} = 1.8 V
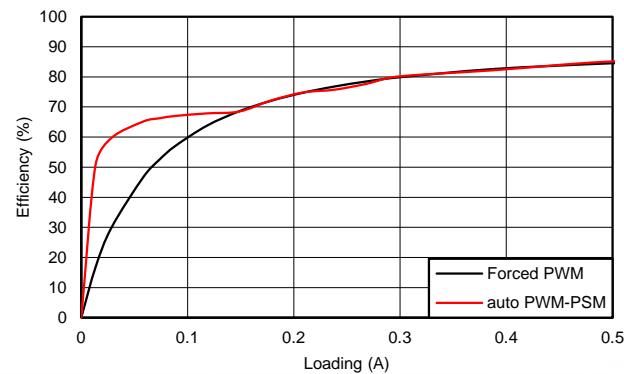
Figure 6. 1.8-V Efficiency, Light Load
V_{IN} = 12 V, V_{OUT} = 1.8 V
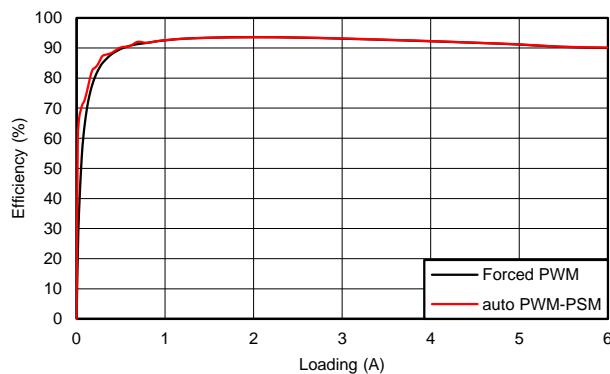
Figure 7. 3.3-V Efficiency
V_{IN} = 12 V, V_{OUT} = 3.3 V
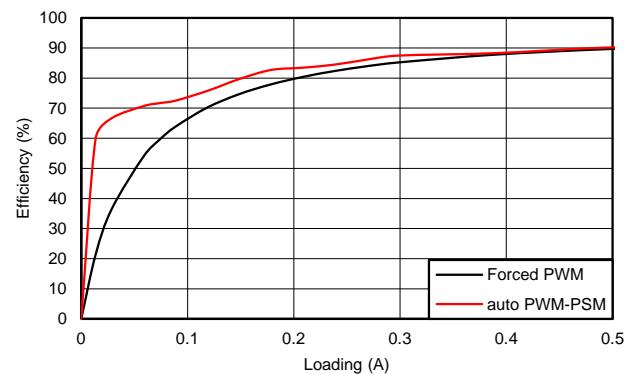
Figure 8. 3.3-V Efficiency, Light Load
V_{IN} = 12 V, V_{OUT} = 3.3 V

Product Folder Links: *TPS65276*

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)
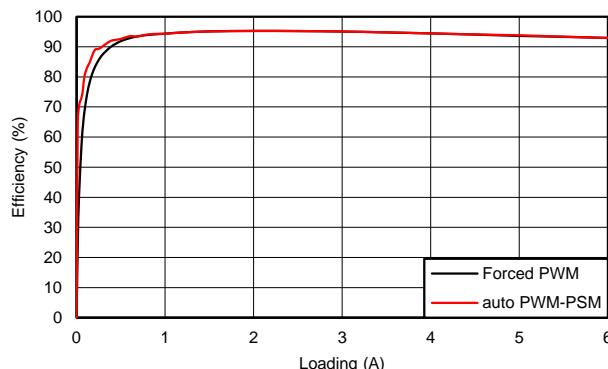

Figure 9. 5-V Efficiency
V_{IN} = 12 V, V_{OUT} = 5 V
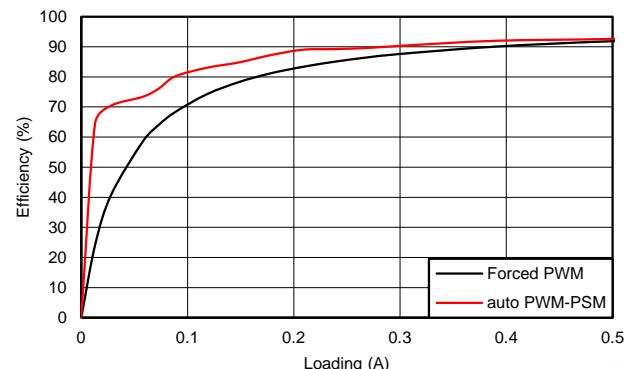
Figure 10. 5-V Efficiency, Light Load
V_{IN} = 12 V, V_{OUT} = 5 V
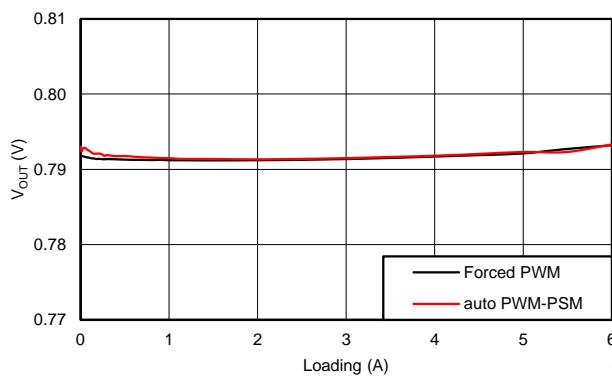
Figure 11. 0.8-V Load Regulation
V_{IN} = 12 V, V_{OUT} = 0.8 V
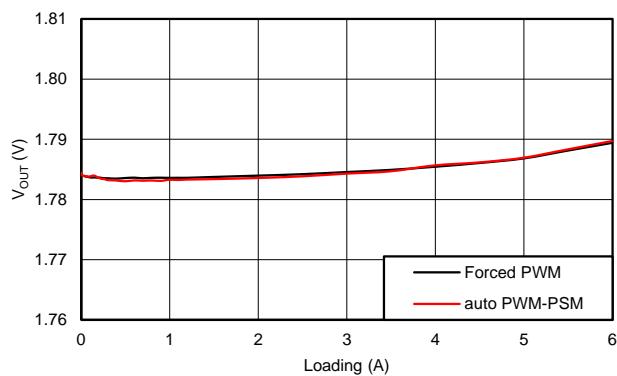
Figure 12. 1.8-V Load Regulation
V_{IN} = 12 V, V_{OUT} = 1.8 V
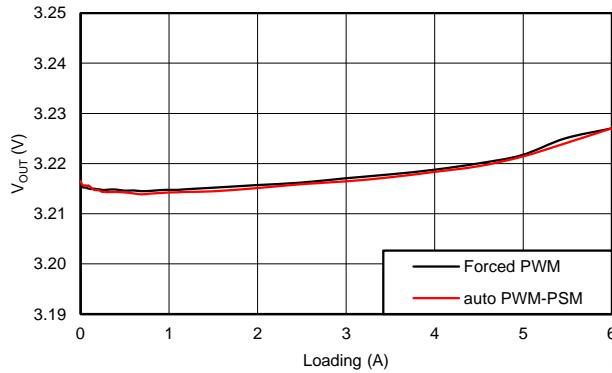
Figure 13. 3.3-V Load Regulation
V_{IN} = 12 V, V_{OUT} = 3.3 V
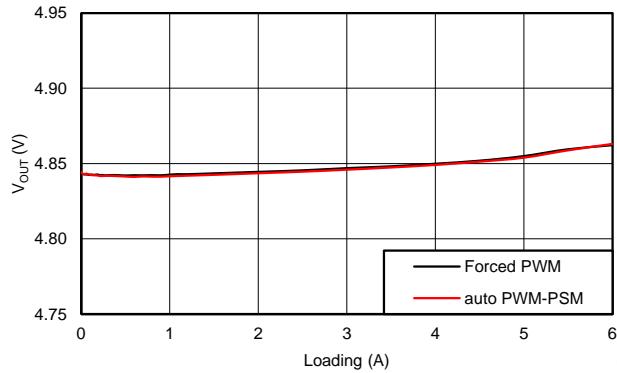
Figure 14. 5-V Load Regulation
V_{IN} = 12 V, V_{OUT} = 5 V

Product Folder Links: *TPS65276*

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)
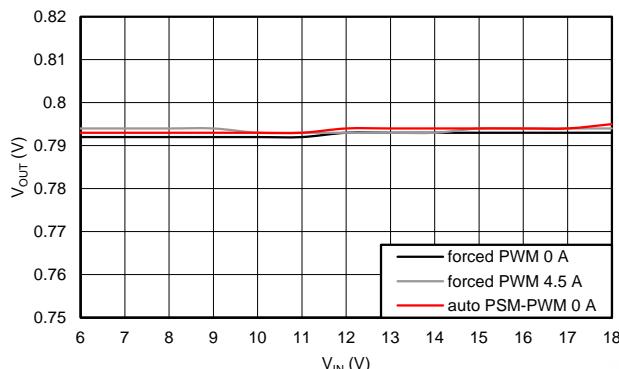
Figure 15. 0.8-V Line Regulation
V_{OUT} = 0.8 V
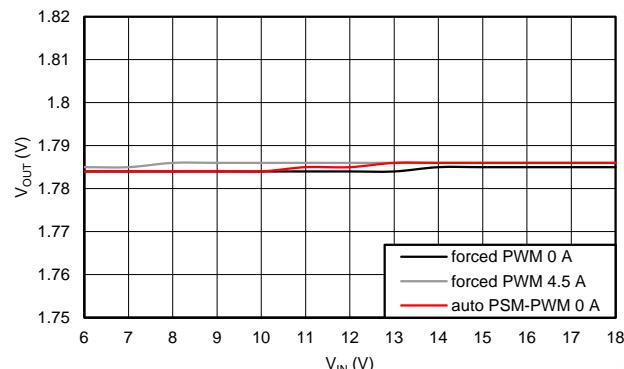
Figure 16. 1.8-V Line Regulation
V_{OUT} = 1.8 V
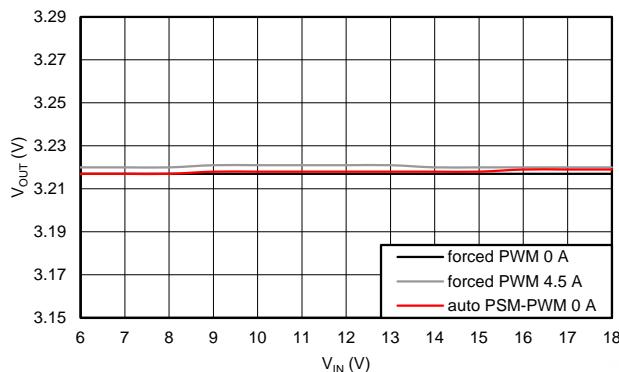
Figure 17. 3.3-V Line Regulation
V_{OUT} = 3.3 V
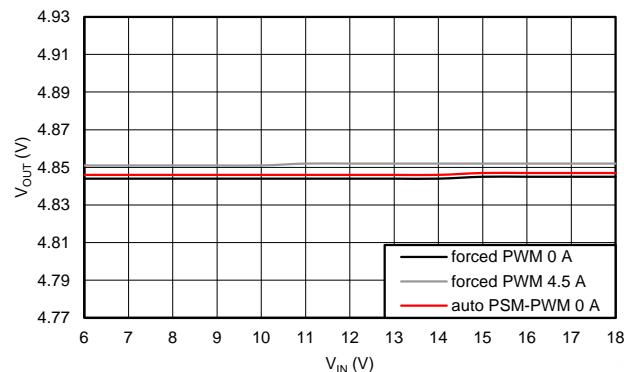
Figure 18. 5-V Line Regulation
V_{OUT} = 5 V
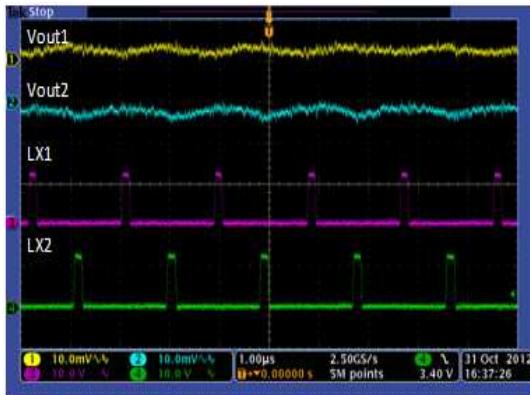
Figure 19. Output Ripple at 0 A, Forced PWM
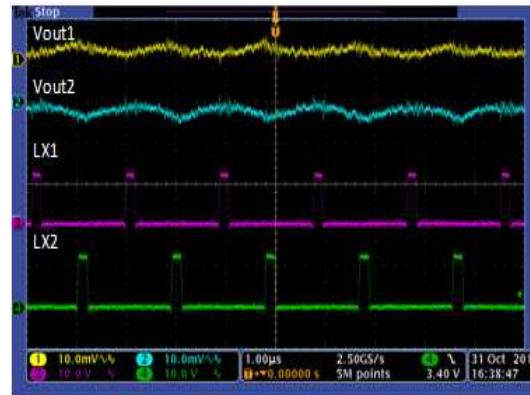
Figure 20. Output Ripple at 3.5 A, Forced PWM

Product Folder Links: *TPS65276*

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)
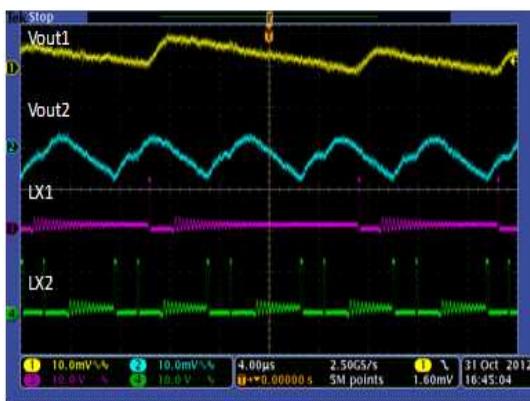
**Figure 21. Output Ripple, Buck1 at 0.05 A,
Buck 2 at 0.2 A Auto PSM-PWM Mode**
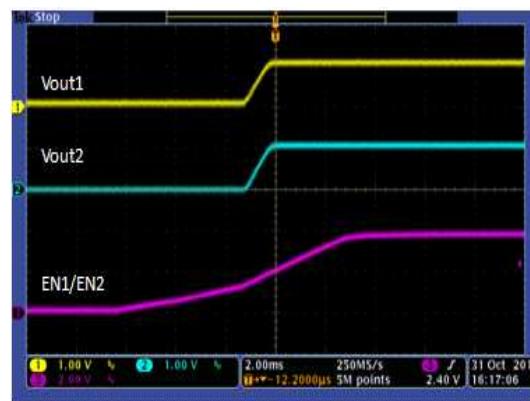
Figure 22. Startup With Enable
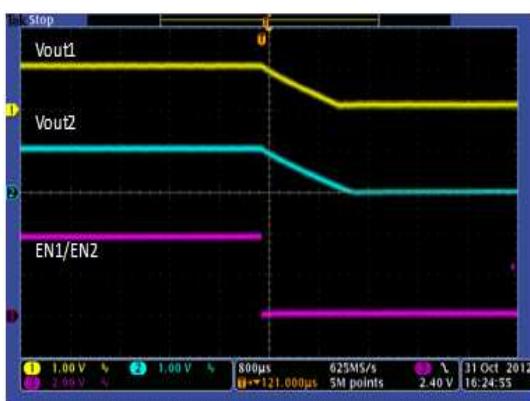
Figure 23. Shutdown With Enable
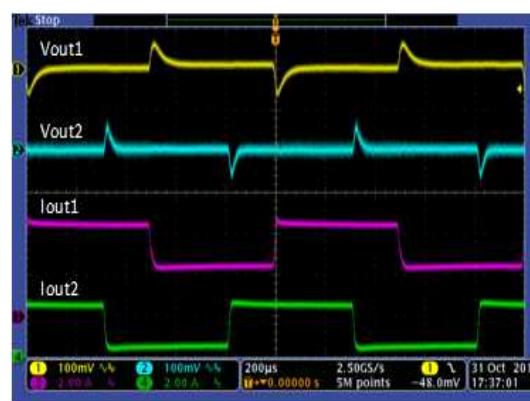
**Figure 24. Load Transient, Buck 1 2.5 A - 4.5 A,
Buck2 0.5 A - 2.5 A**
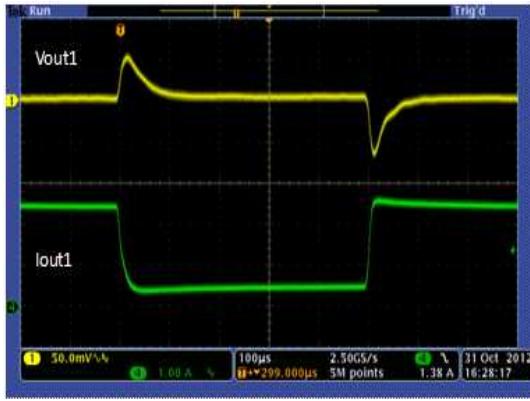
Figure 25. Load Transient, Buck 1 (0.5 A - 2.5 A)
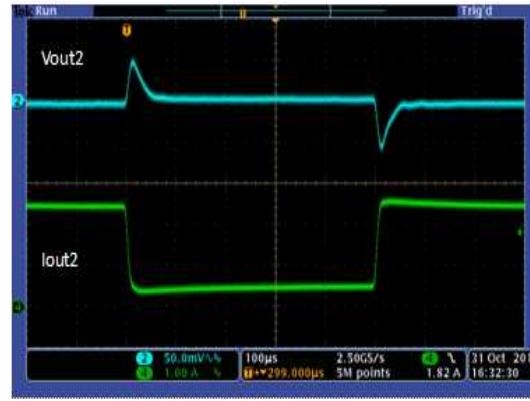
Figure 26. Load Transient, Buck 2 (0.5 A - 2.5 A)

Product Folder Links: *TPS65276*

TYPICAL CHARACTERISTICS (continued)

$T_A = 25°C$, $V_{IN} = 12$ V, $f_{SW} = 625$ kHz (unless otherwise noted)
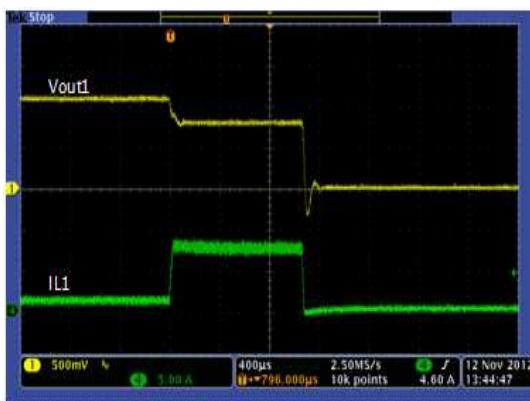
Figure 27. Over Current Protection Buck 1
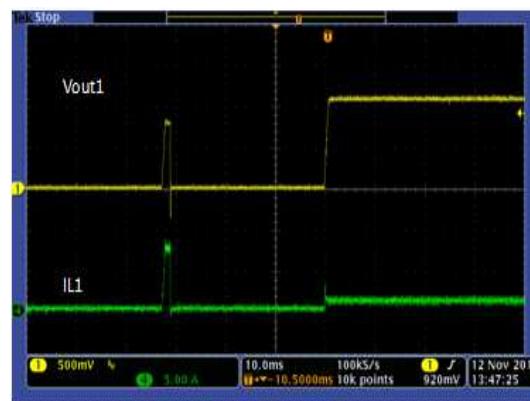
Figure 28. Hiccup Recover, Buck 1
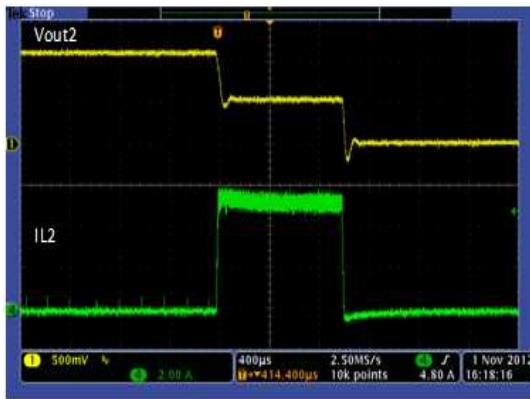
Figure 29. Over Current Protection, Buck 2

Figure 30. Hiccup Recover, Buck 2
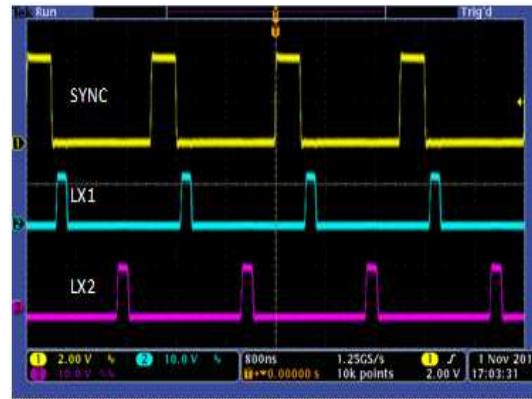
Figure 31. Synchronization at 500 kHz

Product Folder Links: *TPS65276*

OVERVIEW

TPS65276 is a dual 6-A/3.5-A output current, synchronous step-down (buck) converter with integrated n-channel MOSFETs. A wide 4.5-V to 18-V input supply range to buck encompasses most intermediate bus voltages operating off 9-V, 12-V or 15-V power bus.

TPS65276 implements a constant frequency, peak current mode control which simplifies external frequency compensation. The wide switching frequency of 200 kHz to 1600 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency can be adjusted with an external resistor to ground on the ROSC pin. The TPS65276 also has an internal phase lock loop (PLL) controlled by the ROSC pin that can be used to synchronize the switching cycle to the falling edge of an external system clock. 180° out-of-phase operation between two channels reduces input filter and power supply induced noise.

TPS65276 has been designed for safe monotonic startup into pre-biased loads. The default start up is when VIN is typically 4.5 V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for automatically starting up the TPS65276 with the internal pull up current.

The integrated MOSFETs of each channel allow for high efficiency power supply designs with continuous output currents up to 6 A and 3.5 A respectively. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

The TPS65276 reduces the external component count by integrating the boot recharge circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and LX pins. The boot capacitor voltage is monitored by a BOOT to LX UVLO (BOOT-LX UVLO) circuit allowing LX pin to be pulled low to recharge the boot capacitor. The TPS65276 can operate at 100% duty cycle as long as the boot capacitor voltage is higher than the preset BOOT-LX UVLO threshold which is typically 2.1 V.

The TPS65276 has a power good comparator (PWRGD) with hysteresis which monitors the output voltage through internal feedback voltage. I^{2}C can read the power good status with commanding register.

The SS (soft start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor or resistor divider should be coupled to the pin for soft start or critical power supply sequencing requirements.

The TPS65276 is protected from output overvoltage, overload and thermal fault conditions. The TPS65276 minimizes excessive output overvoltage transients by taking advantage of the power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the internal feedback voltage is lower than 108% of the 0.6-V reference voltage. The TPS65276 implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections which help control the inductor current and avoid current runaway. If the over current condition has lasted for more than the hiccup wait time, the TPS65276 will shut down and re-start after the hiccup time. The TPS65276 also shuts down if the junction temperature is higher than thermal shutdown trip point. When the junction temperature drops 20°C typically below the thermal shutdown trip point, the built-in thermal shutdown hiccup timer is triggered. The TPS65276 will be restarted under control of the soft start circuit automatically after the thermal shutdown hiccup time is over.

Furthermore, if the over-current condition has lasted for more than the hiccup wait time which is programmed for 512 switching cycles, the TPS65276 will shut down itself and re-start after the hiccup time which is set for 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe over-current conditions.

The TPS65276 operates at any load conditions unless the COMP pin voltage drops below the COMP pin start switching threshold which is typically 0.25 V.

When PSM mode operation is enabled, the TPS65276 monitors the peak switch current of the high-side MOSFET. Once the peak switch current is lower than typically 1 A, the device stops switching to boost the efficiency until the peak switch current is higher than typically 1 A again.

DETAILED DESCRIPTION

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node (VOUT) to the FB pin. It is recommended to use 1% tolerance or better divider resistors.
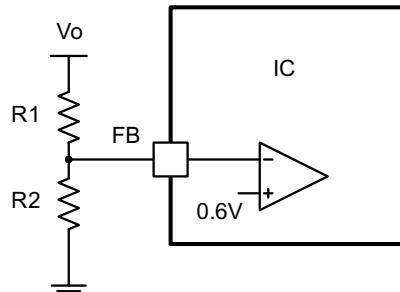
Figure 32. Voltage Divider Circuit

$$R2 = R1 \cdot \left(\frac{0.6V}{V_{OUT} - 0.6V} \right)$$

(1)

Start with a 40.2-kΩ for R1 and use Equation 1 to calculate R2. To improve efficiency at light loads consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

The minimum output voltage and maximum output voltage can be limited by the minimum on time of the high-side MOSFET and bootstrap voltage (BOOT-PH voltage) respectively. More discussions are located in Minimum Output Voltage and Bootstrap Voltage (BOOT) and Low Dropout Operation.

Enable and Adjusting Under-Voltage Lockout

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state.

The EN pin has an internal pull-up current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 500mV.

If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVIN, in split rail applications, then the EN pin can be configured as shown in Figure 33.

When using the external UVLO function it is recommended to set the hysteresis to be greater than 500 mV.

The EN pin has a small pull-up current I_P which sets the default state of the pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function since it increases by Ih once the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 2 and Equation 3.
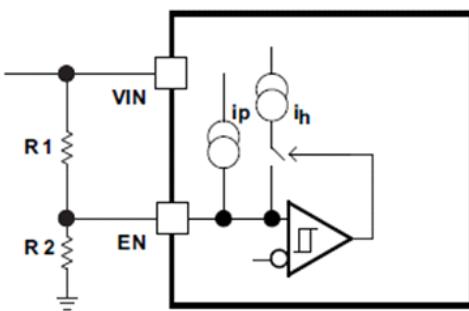
Figure 33. Adjustable VIN Under-Voltage Lockout

$$R_1 = \frac{V_{START}(\frac{V_{ENFALLING}}{V_{ENRISING}}) - V_{STOP}}{I_P(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}) + I_h}$$

(2)

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_1(I_h + I_p)}$$

(3)

Where I_h = 3 µA, I_P = 3 µA, $V_{ENRISING}$ = 1.21 V, $V_{ENFALLING}$ = 1.17 V.

Adjustable Switching Frequency and Synchronization

The ROSC pin can be used to set the switching frequency of the device in two mode. The resistor mode is to connect a resistor between ROSC pin and GND. The switching frequency of the device is adjustable from 200 kHz to 1600 kHz. The other mode called synchronization mode is to connect an external clock signal directly to the ROSC pin. The device is synchronized to the external clock frequency with PLL.

Synchronization mode overrides the resistor mode. The device is able to detect the proper mode automatically and switch from synchronization mode to resistor mode.

Adjustable Switching Frequency (Resistor Mode)

To determine the ROSC resistance for a given switching frequency, use Equation 4 or the curve in Figure 34. To reduce the solution size one would set the switching frequency as high as possible, but tradeoffs of the supply efficiency and minimum controllable on time should be considered.
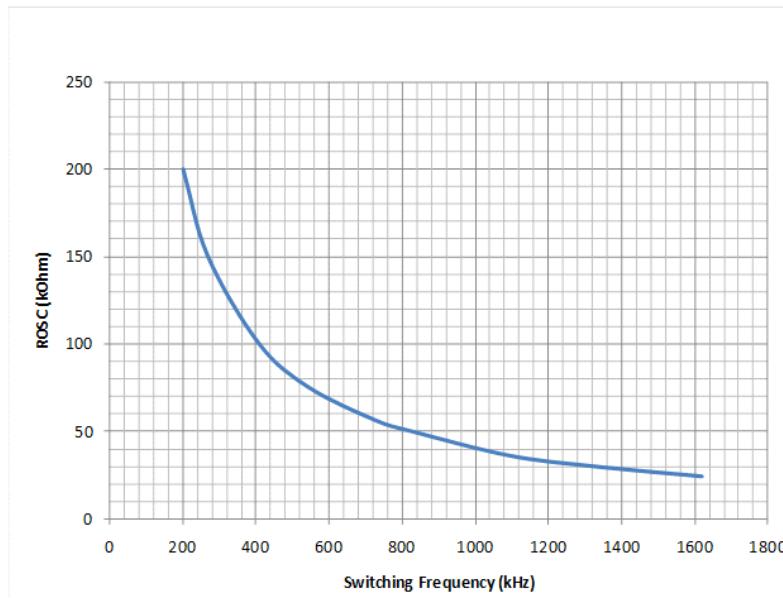
Figure 34. ROSC vs Switching Frequency

$$R_{osc}(k\Omega) = 45580 \cdot f_{sw}^{-1.019}(kHz) \tag{4}$$

Synchronization

An internal phase locked loop (PLL) has been implemented to allow synchronization between 200 kHz and 1600 kHz, and to easily switch from Resistor mode to Synchronization mode.

To implement the synchronization feature, connect a square wave clock signal to the ROSC pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.8 V and higher than 2 V. The start of the switching cycle is synchronized to the falling edge of ROSC pin.

In applications where both Resistor mode and Synchronization mode are needed, the device can be configured as shown in Figure 35. Before the external clock is present, the device works in Resistor mode and the switching frequency is set by ROSC resistor. When the external clock is present, the Synchronization mode overrides the Resistor mode. The first time the ROSC pin is pulled above the ROSC high threshold (2 V), the device switches from the Resistor mode to the Synchronization mode and the ROSC pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from the Synchronization mode back to the Resistor mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by ROSC resistor.
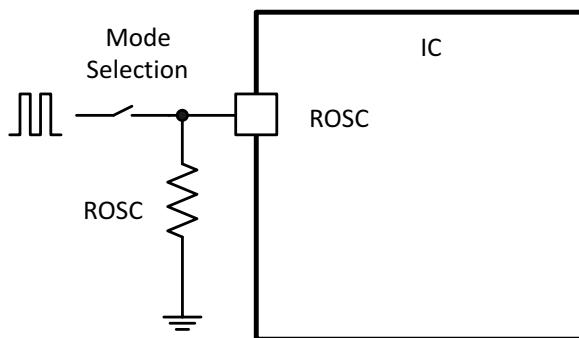
Figure 35. Resistor Mode and Synchronization Mode

Product Folder Links: *TPS65276*

Soft Start Time

The start-up of buck output is controlled by the voltage on the respective SS pin. When the voltage on the SS pin is less than the internal 0.6-V reference, the TPS65276 regulates the internal feedback voltage to the voltage on the SS pin instead of 0.6 V. The SS pin can be used to program an external soft-start function or to allow output of buck to track another supply during start-up. The device has an internal pull-up current source of 6 µA that charges an external soft-start capacitor to provide a linear ramping voltage at SS pin. The TPS65276 regulates the internal feedback voltage according to the voltage on the SS pin, allowing VOUT to rise smoothly from 0 V to its final regulated voltage. The total soft-start time will be calculated approximately:

$$Tss(ms) = Css(nF) \cdot \left(\frac{0.6 \cdot V}{6 \cdot \mu A} \right)$$

(5)

Out-of-Phase Operation

In order to reduce input ripple current, Buck 1 and Buck 2 operate 180° out-of-phase. This enables the system having less input ripple, then to lower component cost, save board space and reduce EMI.

Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

Bootsrap Voltage (BOOT) and Low Dropout Operation

The device has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and LX pins to provide the gate drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than VIN and BOOT-LX voltage is below regulation. The value of this ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

To improve drop out, the device is designed to operate at 100% duty cycle as long as the BOOT to LX pin voltage is greater than the BOOT-LX UVLO threshold which is typically 2.1 V. When the voltage between BOOT and LX drops below the BOOT-LX UVLO threshold the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged. In applications with split input voltage rails.

100% duty cycle operation can be achieved as long as (VIN – PVIN) > 4 V.

Over Current Protection

The device is protected from over current conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

High-Side MOSFET Over Current Protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle by cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference the high-side switch is turned off.

TPS65276 features adjustable over current protection trip point. The peak current limit can be set by external resistors connected between pin RLIM1/2 to ground. By setting lower current limit, lower current rating inductor can be used to reduce system cost.
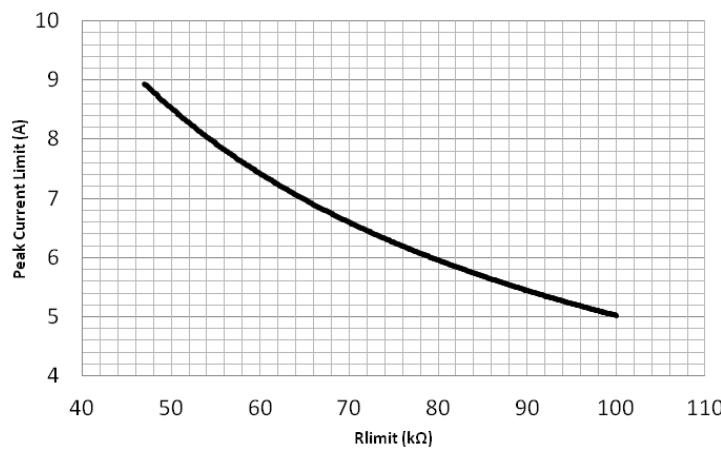
Figure 36. Peak Current Limit vs. R$_{limit}$

Ilim (A) = 168.98 x Rlimit (kΩ)$^{-0.763}$ (6)

Low-Side MOSFET Over Current Protection

While the low-side MOSFET is turned on its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time which is programmed for 512 switching cycles, the device will shut down itself and restart after the hiccup time of 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions. When one channel is in OCP, the other channel is not impacted and remains independent.

Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. Once the junction temperature drops below 140°C typically, the internal thermal hiccup timer will start to count. The device reinitiates the power up sequence after the built-in thermal shutdown hiccup time (16384 cycles) is over.

Product Folder Links: *TPS65276*

APPLICATION INFORMATION

Output Inductor Selection

To calculate the value of the output inductor, use Equation 18. LIR is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, LIR is normally from 0.1 to 0.3 for the majority of applications.

$$L = \frac{V_{inmax} - V_{out}}{I_o \cdot LIR} \cdot \frac{V_{out}}{V_{inmax} \cdot f_{sw}}$$

(7)

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 9 and Equation 10.

$$I_{ripple} = \frac{V_{inmax} - V_{out}}{L} \cdot \frac{V_{out}}{V_{inmax} \cdot f_{sw}}$$

(8)

$$I_{Lrms} = \sqrt{I_O^2 + \frac{(\frac{V_{out} \cdot (V_{inmax} - V_{out})}{V_{inmax} \cdot L \cdot fsw})^2}{12}}$$

(9)

$$I_{Lpeak} = I_{out} + \frac{I_{ripple}}{2}$$

(10)

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 11 shows the minimum output capacitance necessary to accomplish this.

$$C_o = \frac{2 \cdot \Delta I_{out}}{f_{sw} \cdot \Delta V_{out}}$$

(11)

Where ΔI_{OUT} is the change in output current, f_{SW} is the regulators switching frequency and ΔV_{OUT} is the allowable change in the output voltage. For this example, the transient load response is specified as a 5% change in V_{OUT} for a load step of 3 A. For this example, ΔI_{OUT} = 3 A and ΔV_{OUT} = 0.05 x 3.3 = 0.165 V. Using these numbers gives a minimum capacitance of 75.8 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 12 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{SW} is the switching frequency, $V_{oripple}$ is the maximum allowable output voltage ripple, and $I_{oripple}$ is the inductor ripple current.

$$C_o > \frac{1}{8 \cdot f_{sw}} \cdot \frac{1}{\dfrac{V_{oripple}}{I_{oripple}}}$$

(12)

Equation 13 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification.

$$R_{esr} < \frac{V_{oripple}}{I_{oripple}}$$

(13)

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases this minimum value.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Equation 14 can be used to calculate the RMS ripple current the output capacitor needs to support.

$$I_{corms} = \frac{V_{out} \cdot (V_{inmax} - V_{out})}{\sqrt{12} \cdot V_{inmax} \cdot L \cdot f_{sw}}$$

(14)

Input Capacitor Selection

The TPS65276 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10-µF of effective capacitance on the PVIN input voltage pins. In some applications additional bulk capacitance may also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS65276. The input ripple current can be calculated using Equation 15.

$$I_{inrms} = I_{out} \cdot \sqrt{\frac{V_{out}}{V_{inmin}} \cdot \frac{(V_{inmin} - V_{out})}{V_{inmin}}}$$

(15)

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. TPS65276 may operate from a single supply. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 16.

$$\Delta V_{in} = \frac{I_{outmax} \cdot 0.25}{C_{in} \cdot f_{sw}}$$

(16)

Loop Compensation

Integrated buck DC/DC converter in TPS65276 incorporates a peak current mode control scheme. The error amplifier is a transconductance amplifier with a gain of 1350 µA/V. A typical type II compensation circuit adequately delivers a phase margin between 60° and 90°. C_b adds a high frequency pole to attenuate high frequency noise when needed. To calculate the external compensation components, follow the following steps.

1. Select switching frequency f_{sw} that is appropriate for application depending on L and C sizes, output ripple, EMI, and etc. Switching frequency between 500 kHz to 1 MHz gives best trade off between performance and cost. To optimize efficiency, lower switching frequency is desired.

2. Set up cross over frequency, f_c, which is typically between 1/5 and 1/20 of f_{sw}.

3. R_C can be determined by:

$$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$$

Where is the error amplifier gain (1350 µA/V) is the power stage voltage to current conversion gain (10 A/V).

4. Calculate C_C by placing a compensation zero at or before the dominant pole:

$$(\text{fp} = \frac{1}{C_O \cdot R_L \cdot 2\pi}) \cdot s \qquad (17)$$

$$C_C = \frac{R_L \cdot Co}{R_C} \qquad (18)$$

5. Optional C_b can be used to cancel the zero from the ESR associated with C_O.

$$C_b = \frac{R_{ESR} \cdot Co}{R_C} \qquad (19)$$
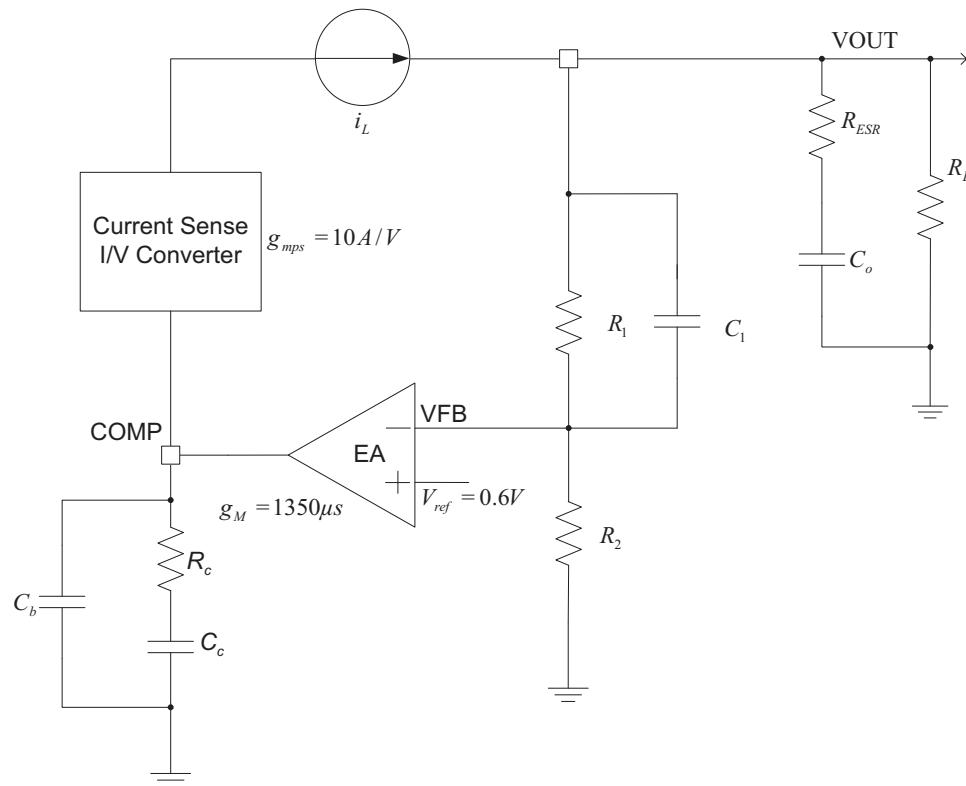
Figure 37. DC/DC Loop Compensation

Product Folder Links: *TPS65276*

PCB Layout Guideline

TPS65276 can be layout on 2-layer PCB illustrated below.

Layout is a critical portion of good power supply design. See Figure 38 for a PCB layout example. The top layer contains the main power traces for VIN, VOUT, and VLX. Also on the top layer are connections for the remaining pins of the TPS65276 and a large top side area filled with ground. The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS65276 device to provide a thermal path from the exposed thermal pad land to ground. The bottom layer acts as ground plane connecting analog ground and power ground.

The GND pin should be tied directly to the power pad under the IC and the power pad. For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the PVIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections. The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric.

Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground should use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The additional external components can be placed approximately as shown.
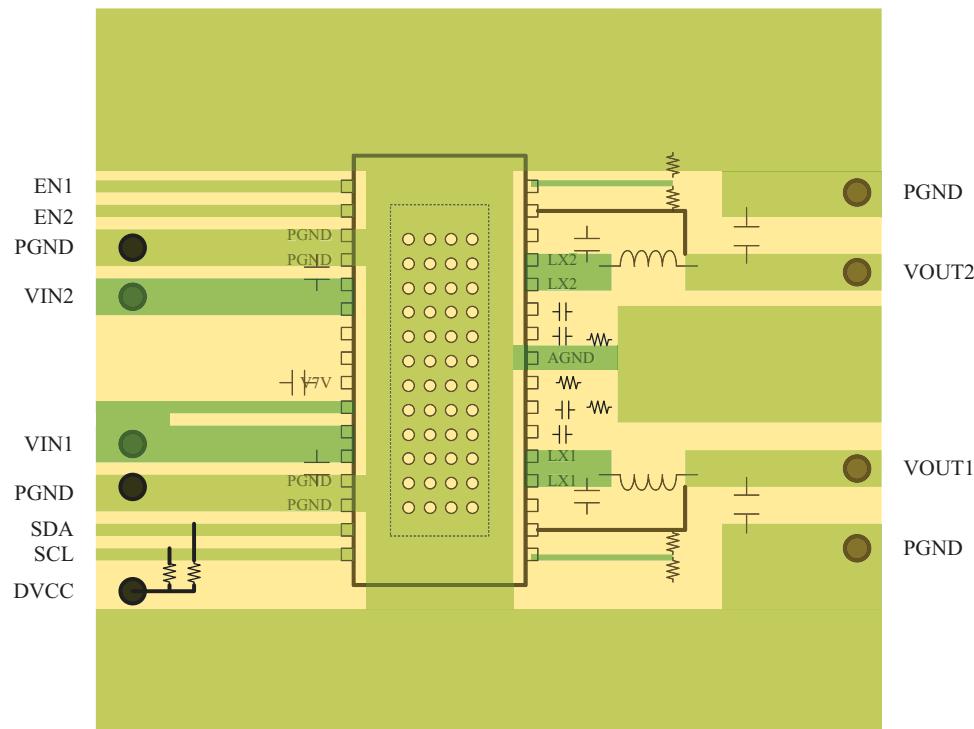

Figure 38. TPS65276 Layout on 2-layer PCB

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65276DAPR	PREVIEW	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS65276	
TPS65276DAPT	PREVIEW	HTSSOP	DAP	32		TBD	Call TI	Call TI	-40 to 125		
TPS65276RHHR	PREVIEW	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65276	
TPS65276RHHT	PREVIEW	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65276	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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DAP (R−PDSO−G32)   PowerPAD™ PLASTIC SMALL−OUTLINE PACKAGE

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

$\dfrac{11,10}{10,90}$

$\dfrac{6,20}{6,00}$

$\dfrac{8,30}{7,90}$

32   17

1   16

0,65

$\dfrac{0,19}{0,30}$

⊕ 0,10 Ⓜ

0,15 NOM

Gauge Plane

0°−8°

0,25

$\dfrac{0,75}{0,50}$

1,20 MAX

$\dfrac{0,15}{0,05}$

Seating Plane

⌒ 0,10
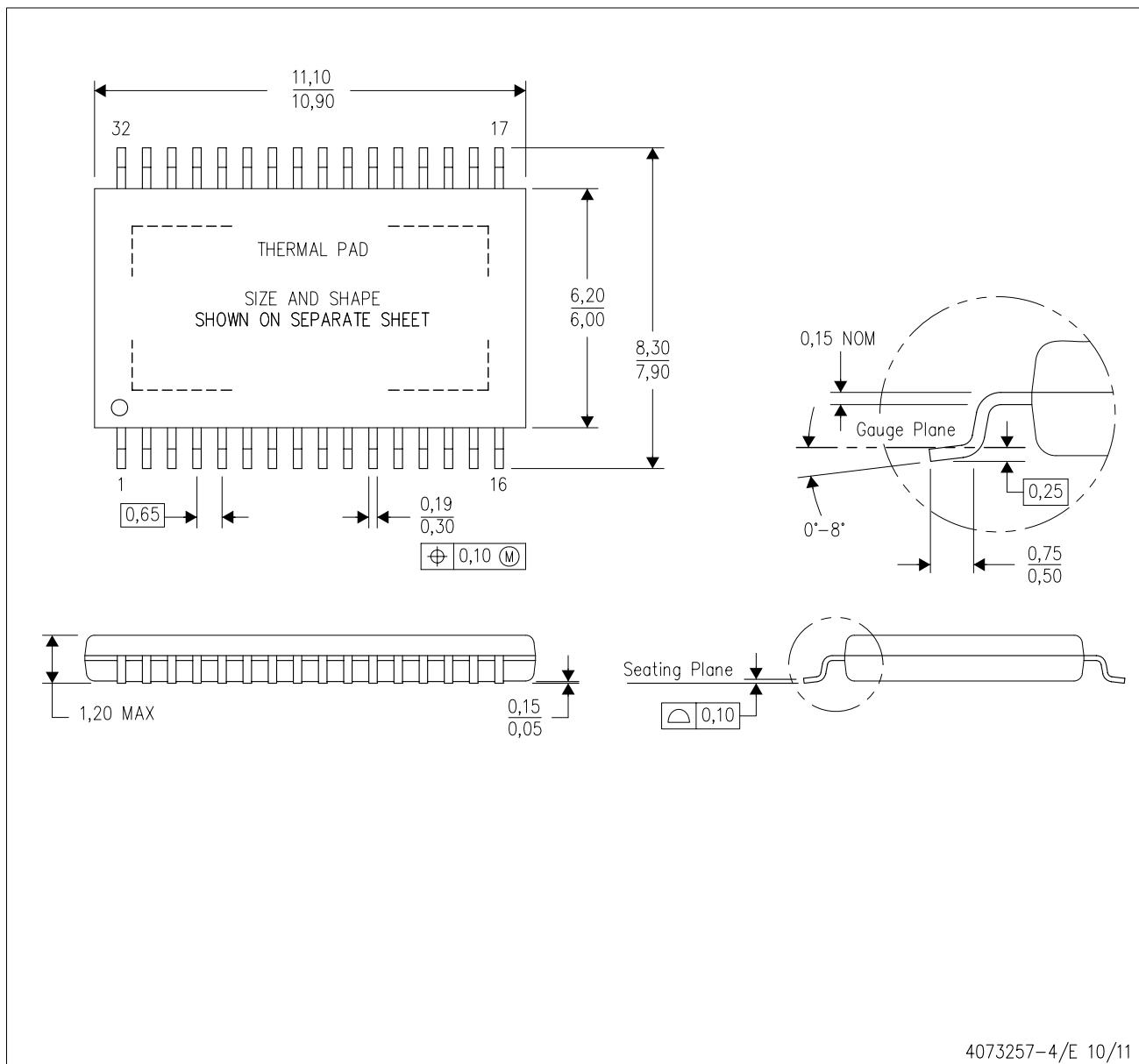
4073257−4/E 10/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
              Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
              recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
         F.   Falls within JEDEC MO−153 Variation DCT.

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TEXAS INSTRUMENTS
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RHH (S—PVQFN—N36)　　　　　　　PLASTIC QUAD FLATPACK NO—LEAD

PIN 1
INDEX AREA

1,00 / 0,80

0,20 REF

0,08 C

SEATING PLANE

0,05 MAX

1

36

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

0,50

36X 0,65 / 0,45

36X 0,30 / 0,18

| 0,10 | M | C | A | B |
| 0,05 | M | C | | |

4205094/E 06/11
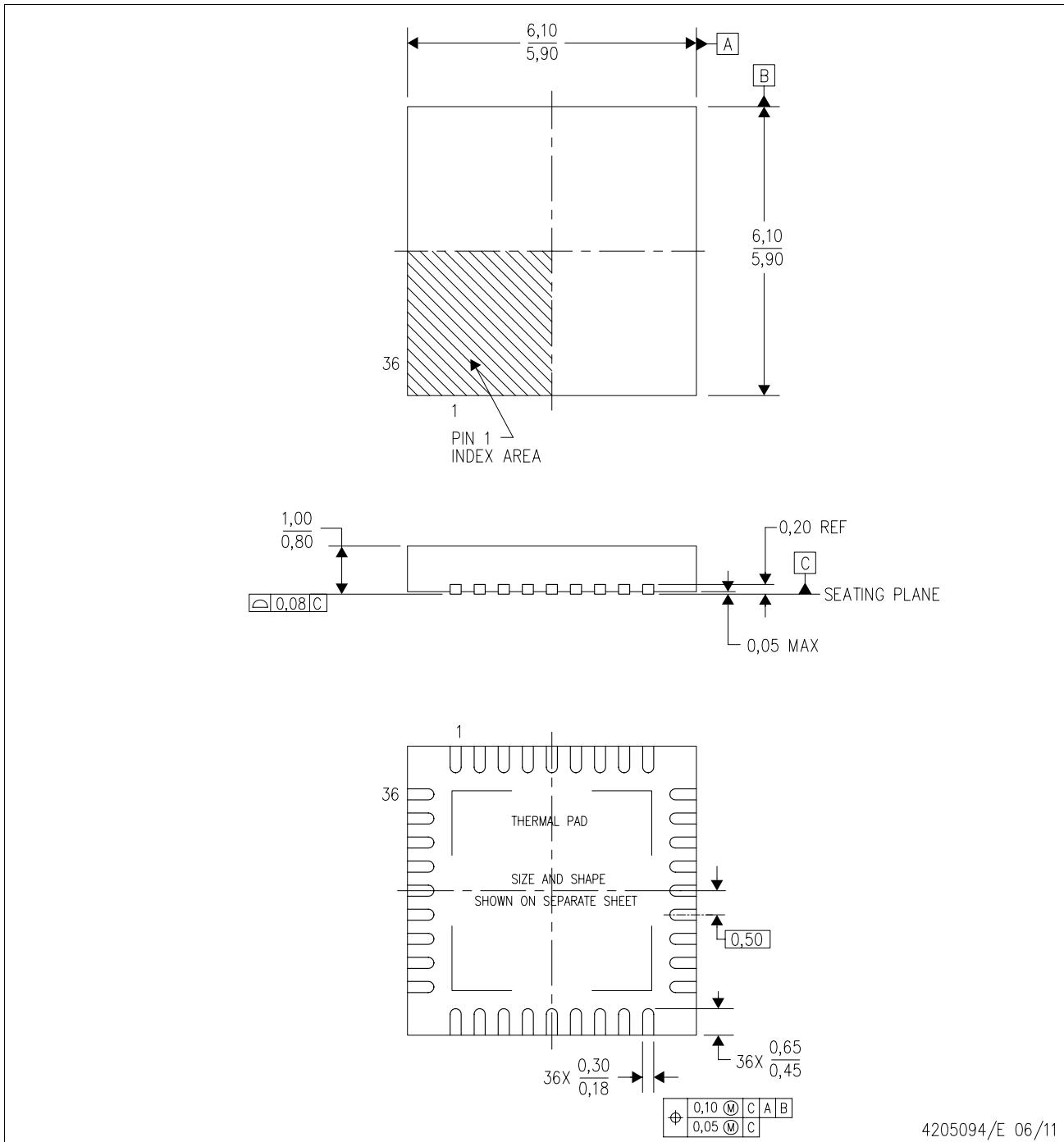
NOTES:　A.　All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　QFN (Quad Flatpack No—Lead) Package configuration.
　　　　　D.　The package thermal pad must be soldered to the board for thermal and mechanical performance.
　　　　　E.　See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
　　　　　F.　Falls within JEDEC MO—220.

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