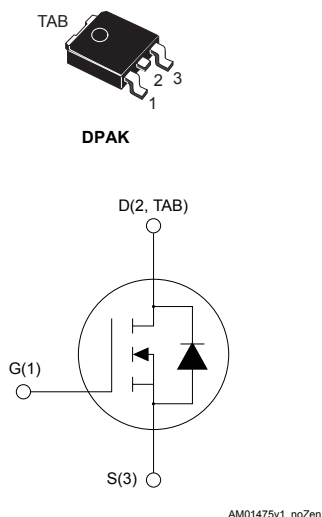


N-channel 500 V, 400 mΩ typ., 8.5 A MDmesh II Power MOSFET in a DPAK package



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD11NM50N	500 V	470 mΩ	8.5 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.



Product status link

[STD11NM50N](#)

Product summary

Order code	STD11NM50N
Marking	11NM50N
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	8.5	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	6	
$I_{DM}^{(1)}$	Drain current (pulsed)	34	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	70	W
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max)	3	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	150	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 8.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.79	$^{\circ}\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	50	$^{\circ}\text{C}/\text{W}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	500			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			100	
I_{GSS}	Gate body leakage current	$V_{GS} = \pm 25\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 4.5\text{ A}$		400	470	m Ω

1. Specified by design, not tested in production.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	547	-	pF
C_{oss}	Output capacitance		-	42	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }400\text{ V}$	-	210	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	5.8	-	Ω
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 8.5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	19	-	nC
Q_{gs}	Gate-source charge		-	3.7	-	nC
Q_{gd}	Gate-drain charge		-	9.6	-	nC

1. $C_{oss\text{ eq.}}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$, $I_D = 4.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	8	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time		-	33	-	ns
t_f	Fall time		-	10	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		34	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8.5 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 8.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	230		ns
Q_{rr}	Reverse recovery charge		-	2.1		μC
I_{RRM}	Reverse recovery current		-	18		A
t_{rr}	Reverse recovery time	$I_{SD} = 8.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	275		ns
Q_{rr}	Reverse recovery charge		-	2.5		μC
I_{RRM}	Reverse recovery current		-	18		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

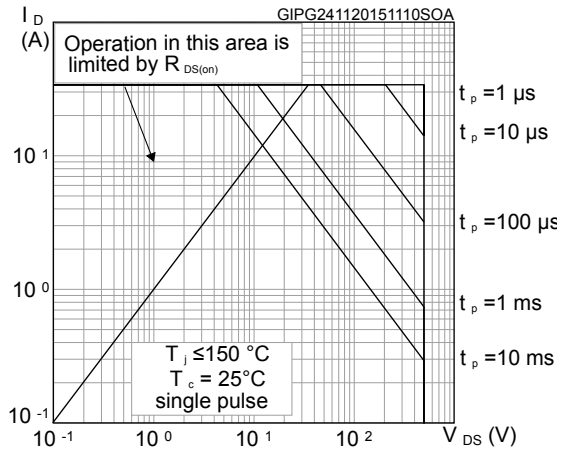


Figure 2. Normalized transient thermal impedance

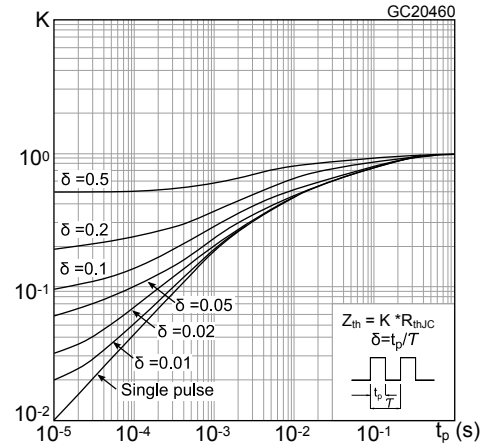


Figure 3. Typical output characteristics

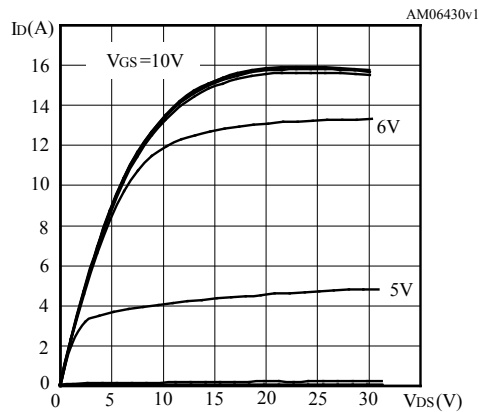


Figure 4. Typical transfer characteristics

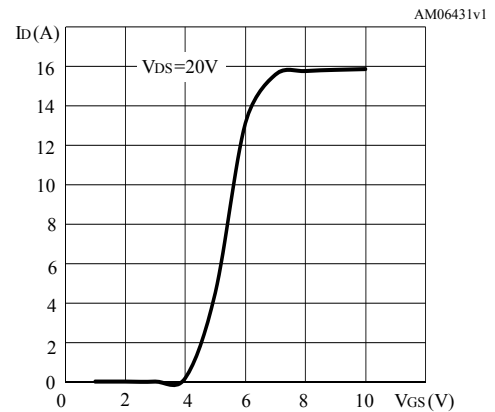


Figure 5. Typical gate charge characteristics

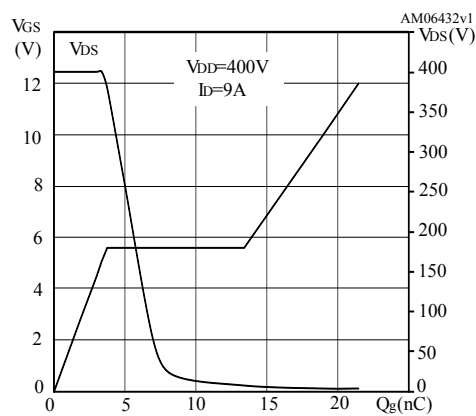


Figure 6. Typical drain-source on-resistance

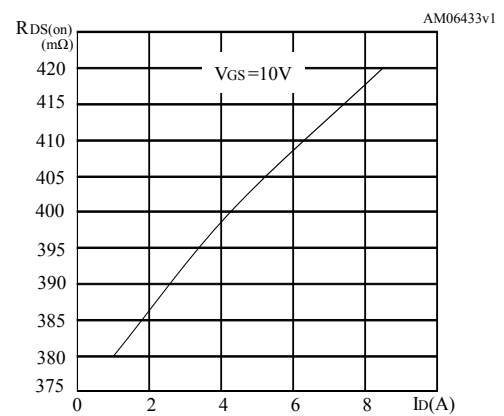


Figure 7. Typical capacitance characteristics

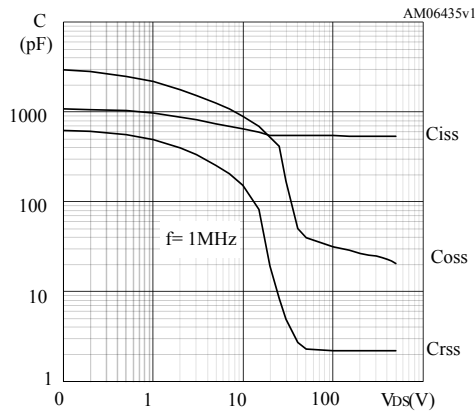


Figure 8. Output capacitance stored energy

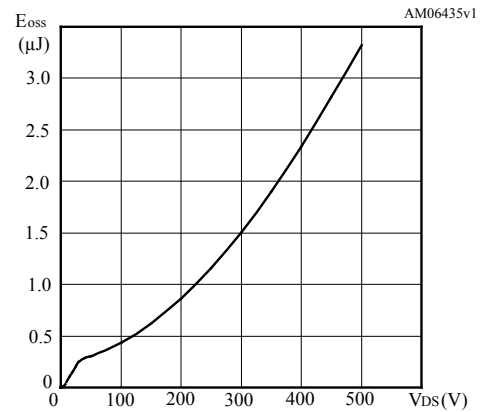


Figure 9. Normalized gate threshold vs temperature

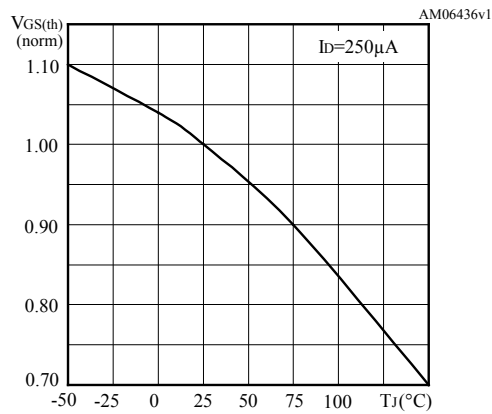


Figure 10. Normalized on-resistance vs temperature

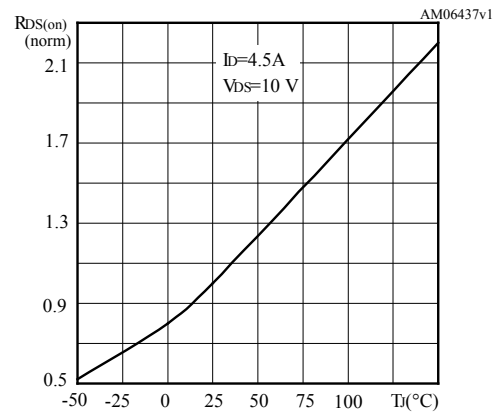
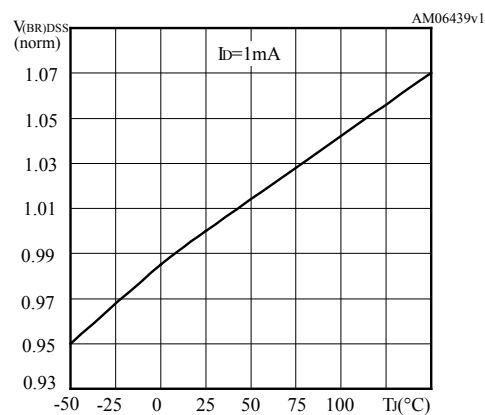
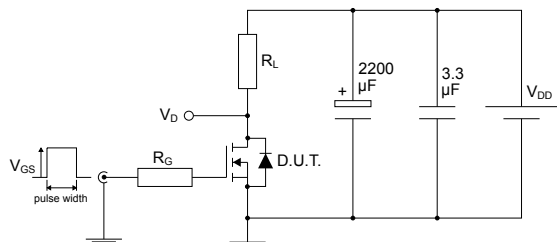


Figure 11. Normalized breakdown voltage vs temperature



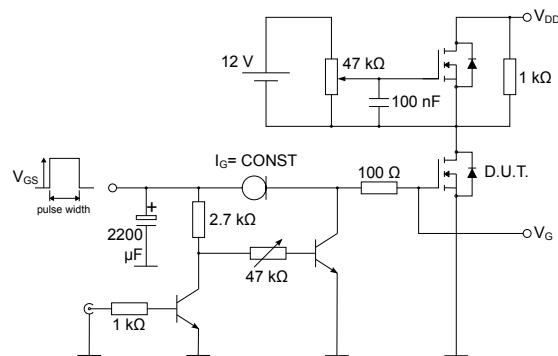
3 Test circuits

Figure 12. Test circuit for resistive load switching times



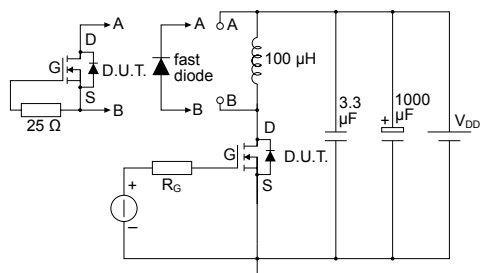
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Figure 13. Test circuit for gate charge behavior



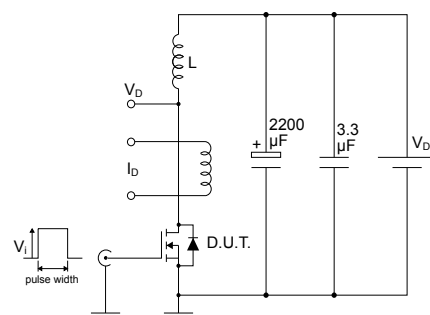
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Figure 14. Test circuit for inductive load switching and diode recovery times



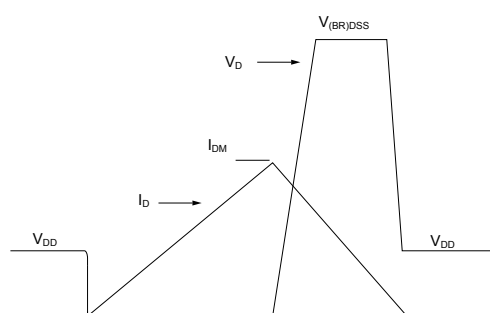
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Figure 15. Unclamped inductive load test circuit



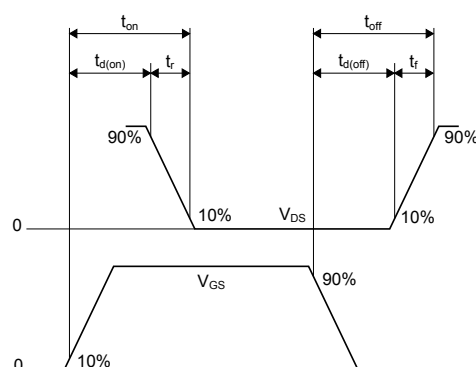
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Figure 16. Unclamped inductive waveform



AM01472v1

Figure 17. Switching time waveform



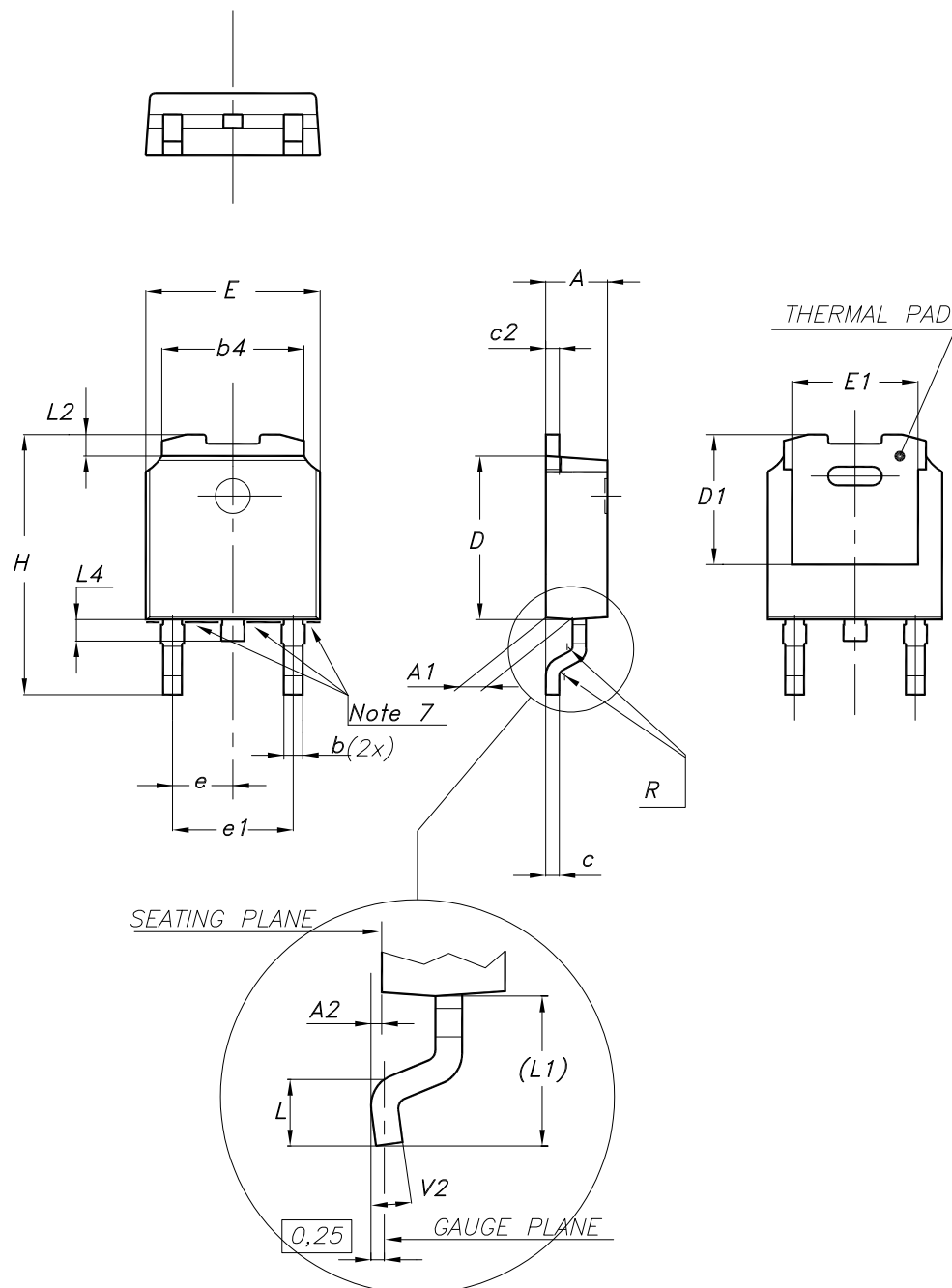
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 18. DPAK (TO-252) type A package outline



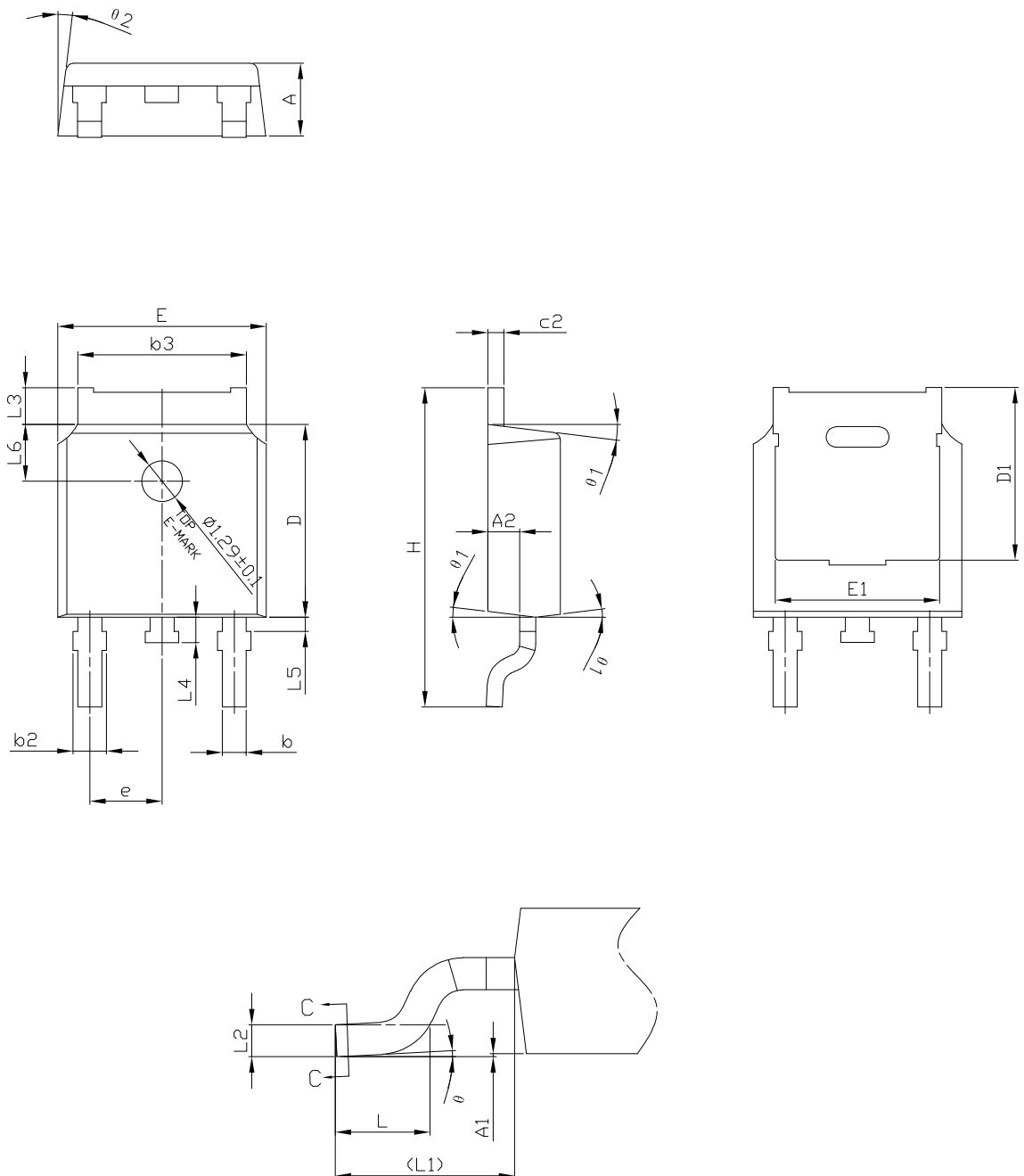
0068772_A_34

Table 7. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C3 package information

Figure 19. DPAK (TO-252) type C3 package outline

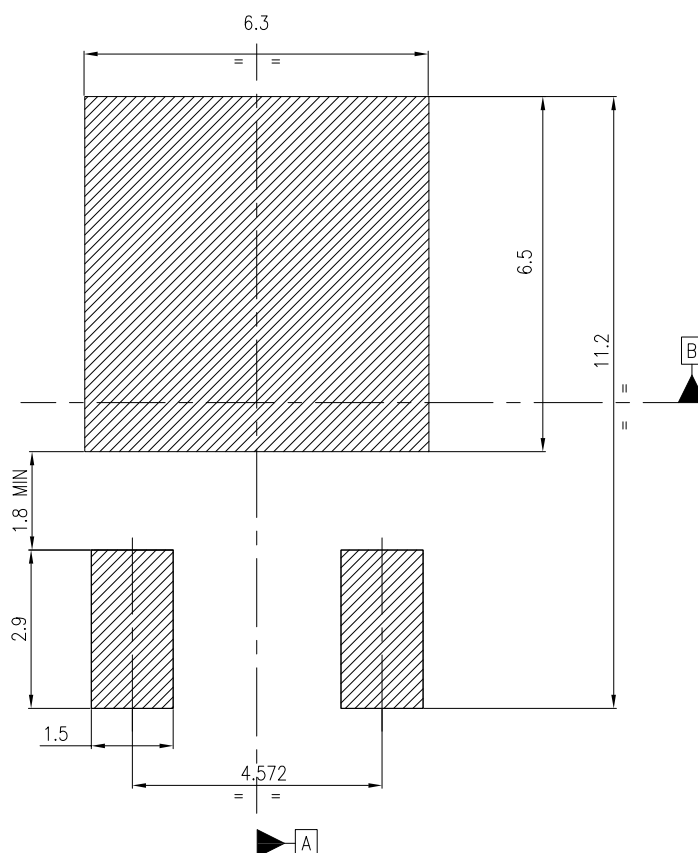


0068772_type-C3_rev34

Table 8. DPAK (TO-252) type C3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.00		0.10
A2	0.90	1.01	1.10
b	0.72		0.85
b2	0.72		1.10
b3	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.20	5.45	5.70
E	6.50	6.60	6.70
E1	5.00	5.20	5.40
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.51 BSC		
L3	0.90		1.25
L4	0.60	0.80	1.00
L5	0.15		0.75
L6	1.80 REF		
θ	0°		8°
θ1	5°	7°	9°
θ2	5°	7°	9°

Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)



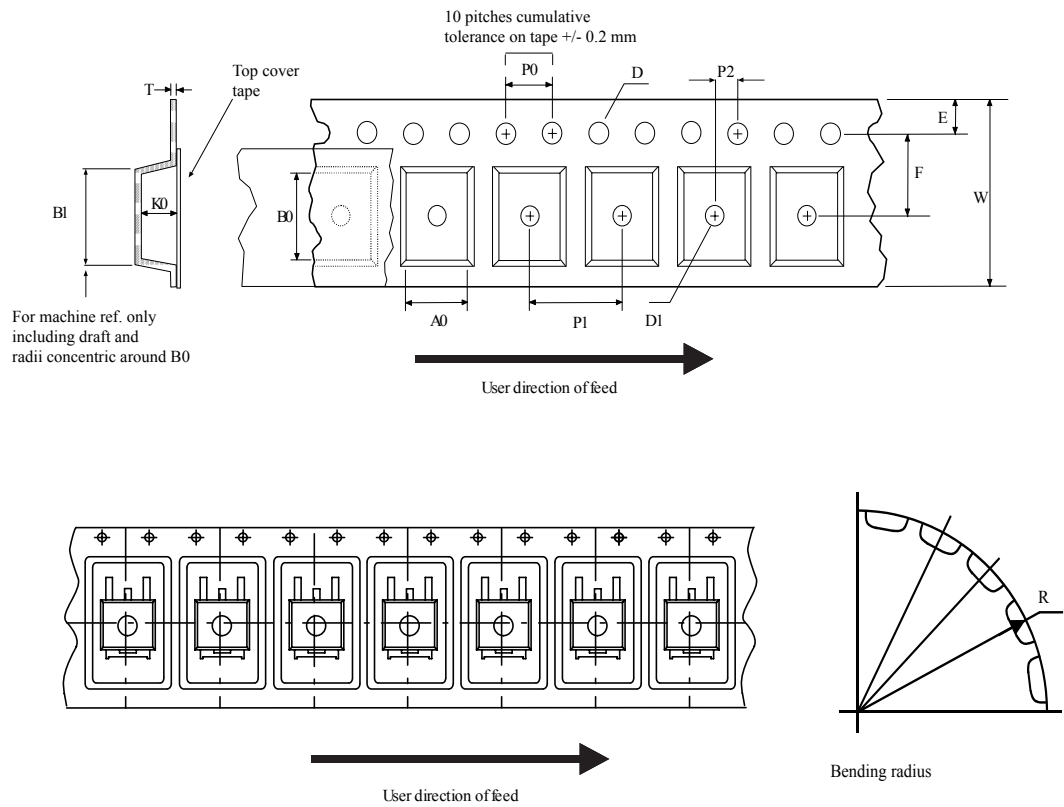
Notes:

- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within $\Phi 0.05$ A B

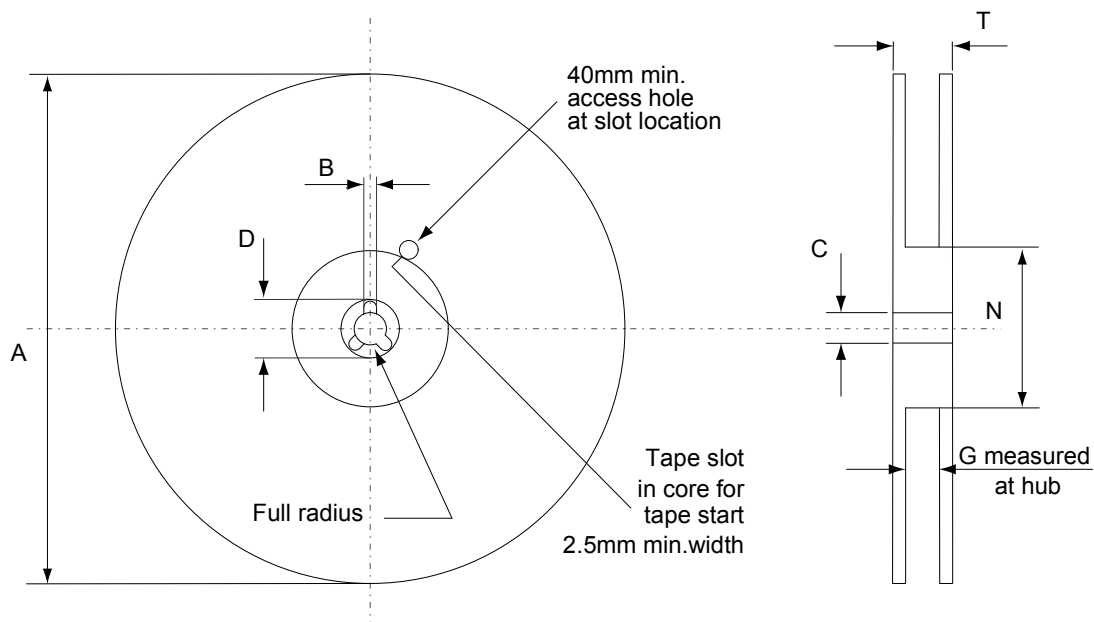
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4.3 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline



AM08852v1

Figure 22. DPAK (TO-252) reel outline


AM06038v1

Table 9. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 10. Document revision history

Date	Version	Changes
25-Nov-2015	1	First release. Part number previously included in datasheet DocID17156
15-Jun-2023	2	Updated the entire Section 4 Package information . Minor text changes.

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