IRF244, IRF245, IRF246, IRF247

File Number **2209**

Avalanche-Energy-Rated N-Channel Power MOSFETs

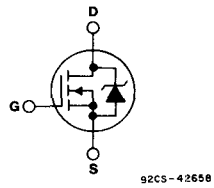
14 A and 13 A, 275 V and 250 V
$r_{DS}(on)$ = 0.28 Ω and 0.34 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *275, 250V dc rated - 120V ac line system operation*

The IRF244, IRF245, IRF246 and IRF247 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

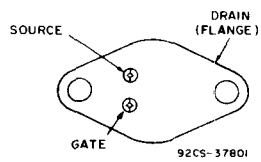
The IRF-types are supplied in the JEDEC TO-204AA steel package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

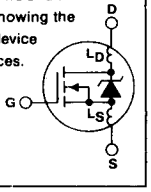
ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRF244	IRF245	IRF246	IRF247	UNITS
Drain-Source Voltage ①	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	250	250	275	275	V
Continuous Drain Current	I_D @ T_C = 25°C	14	13	14	13	A
Continuous Drain Current	I_D @ T_C = 100°C	8.8	8.0	8.8	8.0	A
Pulsed Drain Current ②	I_{DM}	56	52	56	52	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	125				W
Linear Derating Factor		1.0				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	550				mj
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. (1.6 mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS, At T_C = 25°C (Unless Otherwise Specified)

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRF246 IRF247	275	—	—	V	V_{GS} = 0 V
		IRF244 IRF245	250	—	—	V	I_D = 250 μA
Gate Threshold Voltage	$V_{GS}(th)$	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_D(on)$	IRF244 IRF246	14	—	—	A	V_{DS} > $I_D(on)$ x $r_{DS}(on)$ max., V_{GS} = 10 V
		IRF245 IRF247	13	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS}(on)$	IRF244 IRF246	—	0.20	0.28	Ω	V_{GS} = 10 V, I_D = 10 A
		IRF245 IRF247	—	0.24	0.34	Ω	
Forward Transconductance ②	g_{fs}	ALL	6.7	10	—	S (℧)	V_{DS} > $I_D(on)$ x $r_{DS}(on)$ max., I_D = 10 A
Input Capacitance	C_{iss}	ALL	—	1300	—	pF	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	320	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	69	—	pF	
Turn-On Delay Time	$t_d(on)$	ALL	—	16	24	ns	V_{DD} = 90 V, I_D = 10 A, Z_O = 4.7 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	67	100	ns	
Turn-Off Delay Time	$t_d(off)$	ALL	—	53	80	ns	
Fall Time	t_f	ALL	—	49	74	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	39	59	nC	V_{GS} = 10 V, I_D = 22 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	6.6	9.9	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	20	30	nC	
Internal Drain Inductance	L_D	ALL	—	4.5	—	nH	Measured from the drain lead, 6 mm (0.25 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	7.5	—	nH	Measured from the source lead, 6 mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

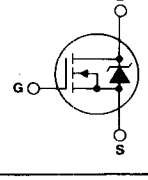


THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$	ALL	—	—	1.0	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	0.5	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	80	°C/W	Free air operation.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRF244 IRF246	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF245 IRF247	—	—	13	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRF244 IRF246	—	—	56	A	
		IRF245 IRF247	—	—	52	A	
Diode Forward Voltage ②	V_{SD}	ALL	—	—	1.8	V	T_C = 25°C, I_S = 14 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	150	300	640	ns	T_J = 150°C, I_F = 14 A, di_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	1.6	3.4	7.2	μC	T_J = 150°C, I_F = 14 A, di_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.

② Pulse Test: Pulse width ≤ 300 μs. Duty Cycle ≤ 2%

③ Repetitive Rating: Pulse width limited by max. junction temperature See Transient Thermal Impedance Curve (Fig. 5).

④ V_{DD} = 50 V, Starting T_J = 25°C, L = 4.5 mH, R_G = 25 Ω, Peak I_L = 14 A (See Figs. 14 & 15).

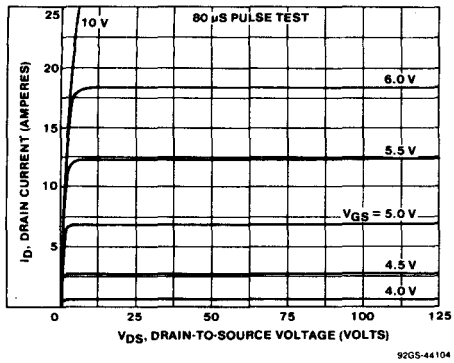


Fig. 1 - Typical output characteristics.

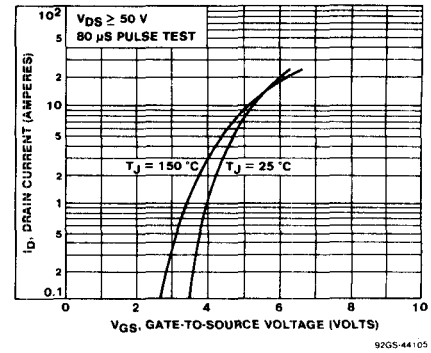


Fig. 2 - Typical transfer characteristics.

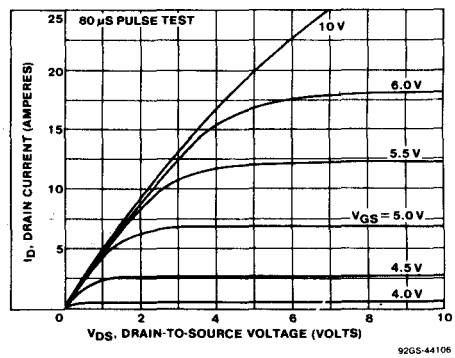


Fig. 3 - Typical saturation characteristics.

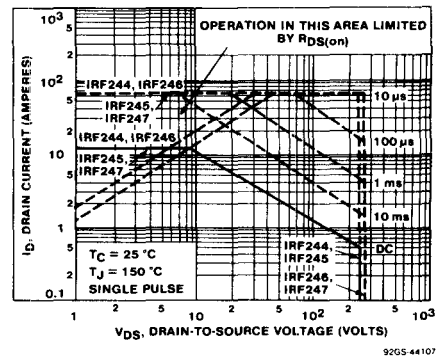


Fig. 4 - Maximum safe operating area.

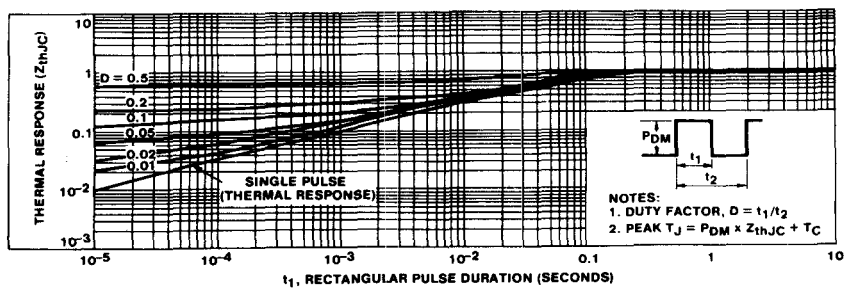


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

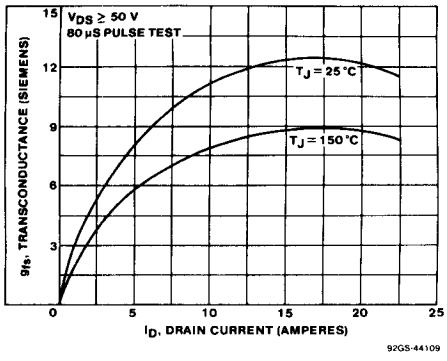


Fig. 6 - Typical transconductance vs. drain current.

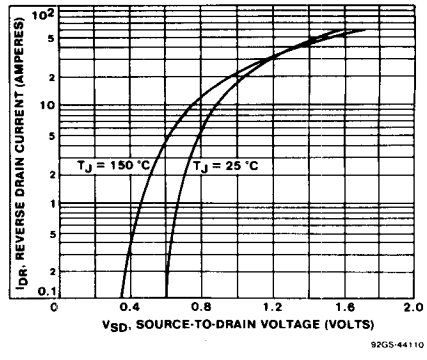


Fig. 7 - Typical source-drain diode forward voltage.

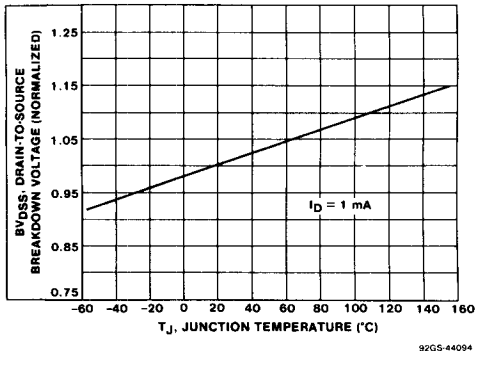


Fig. 8 - Breakdown voltage vs. temperature.

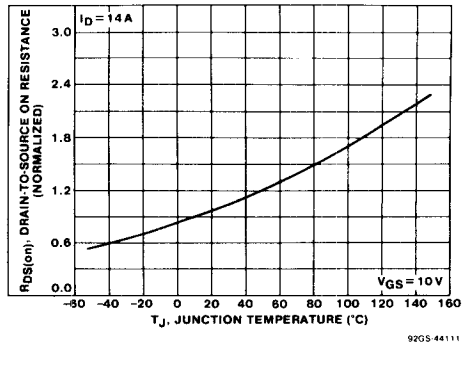


Fig. 9 - Normalized on-resistance vs. temperature.

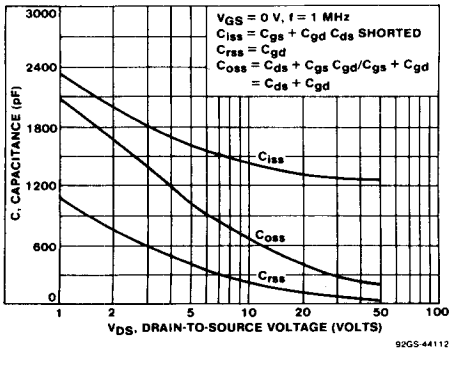


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

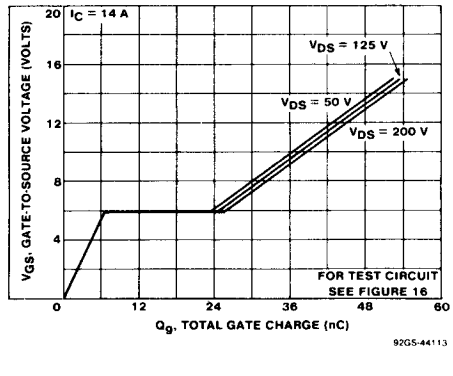


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

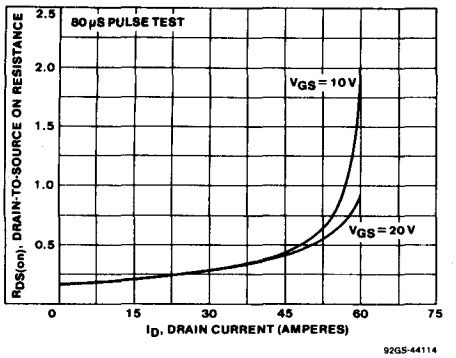


Fig. 12 - Typical on-resistance vs. drain current.

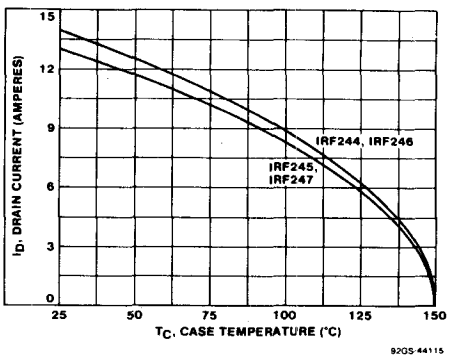


Fig. 13 - Maximum drain current vs. case temperature.

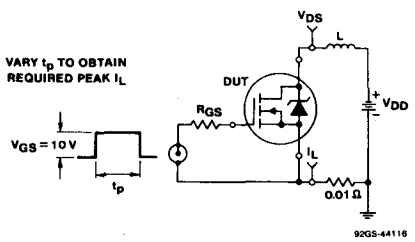


Fig. 14 - Unclamped energy test circuit.

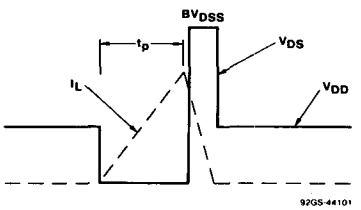


Fig. 15 - Unclamped energy waveforms.

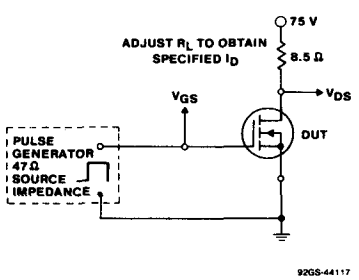


Fig. 16 - Switching time test circuit.

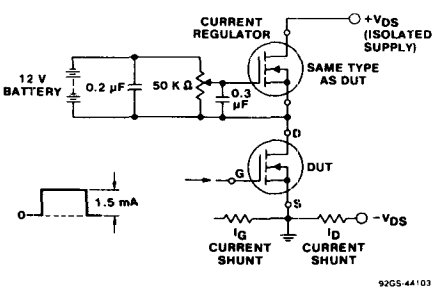


Fig. 17 - Gate charge test circuit.