- **3.125 Gbps Per Port Providing 10-Gbps Data Throughput**
- **Support Transmit Only, Receiver Only, Transceiver and Repeater Functions in a Single Chip Through Configuration Pins**
- **Selectable Independent Channel or Channel Sync Operation**
- **On-Chip Termination for LVDS and PECL Compatible Interface**
- **On-Chip 8-Bit/10-Bit Coding**
- **Hot Plug Protection**
- **Interfaces to Backplane, Copper Cables, or Optical Modules**
- **Receiver Differential Input Thresholds 150 mV Min**
- **PECL Compatible Differential Signaling for Serial Interface With Programmable Preemphasis**
- **ESD Protection 2 kV**
- **Low Power 4-Bit LVDS Parallel Interface**
- **Typical Power Consumption < 675 mW/Port at 3.125 Gbps Under Transceiver Mode**
- **CMOS Technology**
- **Able to Operate With a Single 2.5-V Power Supply**
- **Low Cost 289 Ball PBGA Package**
- **No External Filter Capacitors Required**
- **On-Chip PRBS Generation and Verification**
- **JTAG Test Support**
- **Flow Through Pinout**

description

The TLK3104SCGNT is a flexible four-channel serial backplane transceiver, delivering high-speed bidirectional point-to-point data and transmissions providing up to 10 Gbps of data transmission capacity. The TLK3104SCGNT supports an operating range of serial data rates from 3.1 Gbps to 3.125 Gbps. The primary application of this device is to provide building blocks for developing point-to-point baseband data transmission over controlled impedance media of approximately 50 Ω. The transmission media can be printed-circuit board traces, copper cables, or fiber-optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The TLK3104SCGNT performs the parallel-to-serial, serial-to-parallel conversion, and clock extraction functions for a physical layer interface. The TLK3104SCGNT also provides an 8-bit/10-bit (8-b/10-b) encode/decode function. The serial transmitter and receiver use differential PECL compatible signalings. The parallel interface supports a low voltage differential signaling (LVDS) interface. The purpose of the interface is to provide a simple, inexpensive, and easy-to-implement interconnection between the controller and PHY. The LVDS interface supports independent 4-bit wide transmit and receive data paths for full-duplex operation.

The TLK3104SCGNT provides a comprehensive series of built-in tests for self-test purposes including internal serial loopback and PRBS generation and verification. An IEEE 1149.1 JTAG port is also supported. TLK3104SCGNT also has an MDIO/MDC serial port to provide certain control functions.

The TLK3104SCGNT operates with a single 2.5-V supply and dissipates less than 3 W. The device is packaged in a 19 × 19 mm, 289 pin plastic ball grid array (PBGA) package and is characterised for operation from −40°C to 75°C.

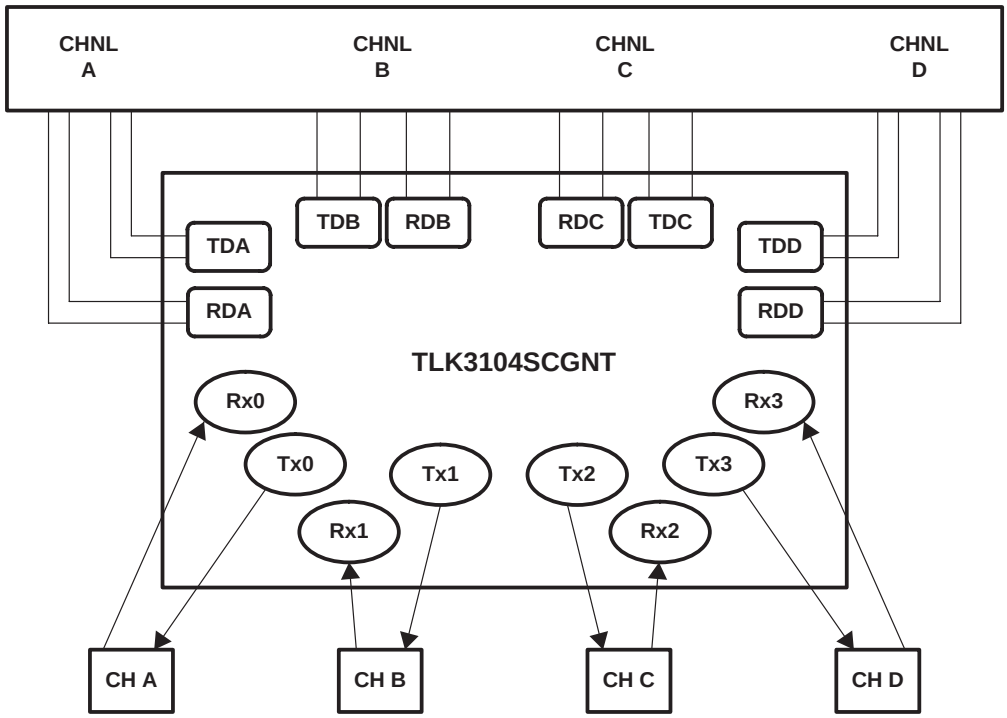
pin assignments

Pin Out
(Top View)

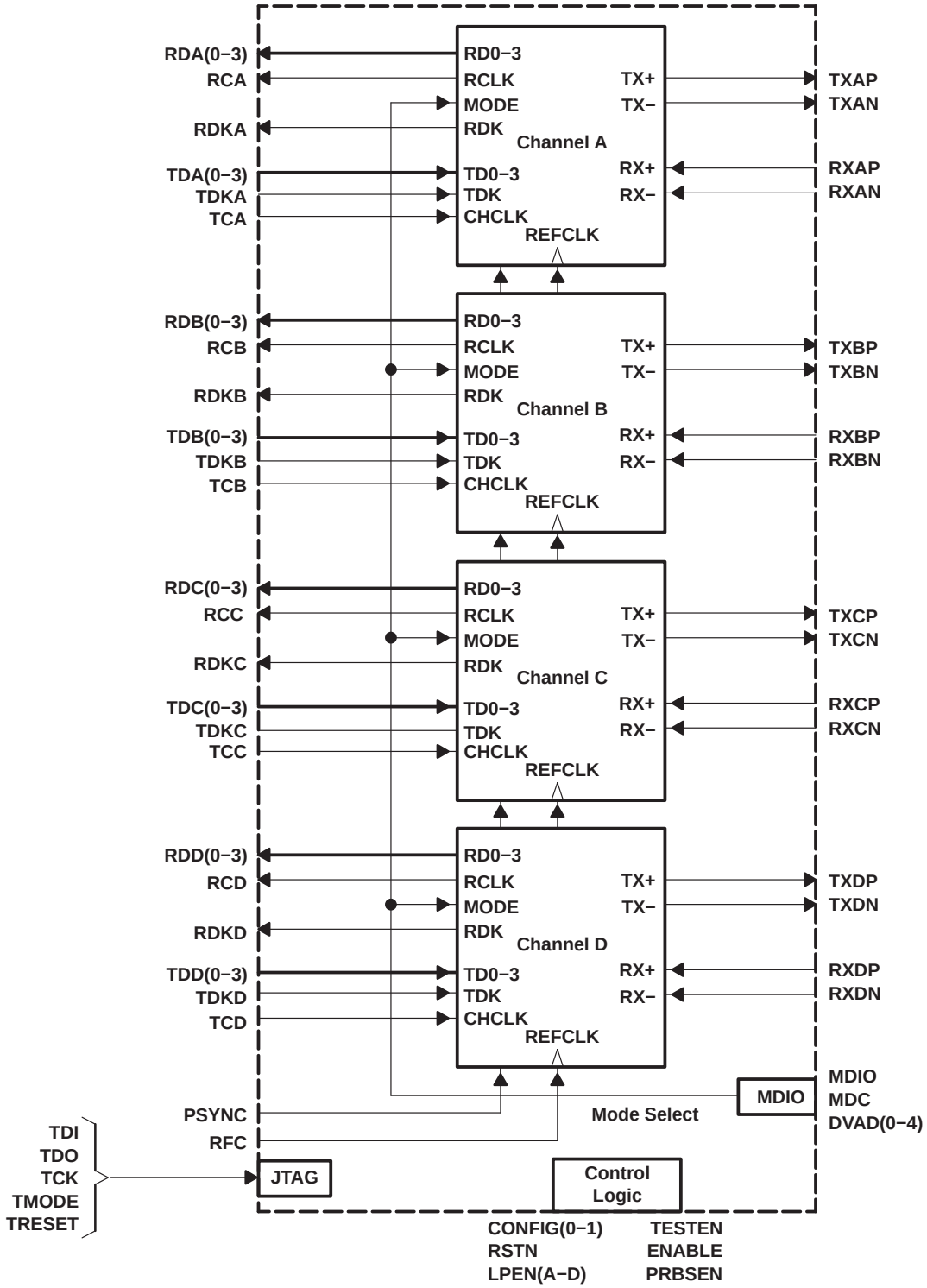
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	
17	VDDIO	GND	TDB3P	VDDIO	GND	RDB0P	VDDIO	GND	RDKCP	GND	VDDIO	RDC0P	GND	VDDIO	TDC3P	GND	VDDIO	17
16	TDB1P	TDB1N	TDB3N	TCBP	TCBN	RDB0N	RDB1P	RCBP	RDKCN	RCCP	RDC1P	RDC0N	TCCN	TCCP	TDC3N	TDC1N	TDC1P	16
15	VDDIO	GND	TDB2P	TDB2N	TDKBP	TDKBN	RDB1N	RCBN	VDDIO	RCCN	RDC1N	TDKCN	TDKCP	TDC2N	TDC2P	GND	VDDIO	15
14	TDA2P	TDA0P	TDA0N	VDDIO	GND	RDB2P	VDDIO	GND	RDKBP	GND	VDDIO	RDC2P	GND	VDDIO	TDD0N	TDD0P	TDD2P	14
13	TDA2N	TDA1P	TDA1N	TDB0P	TDB0N	RDB2N	RDB3P	RDB3N	RDKBN	RDC3N	RDC3P	RDC2N	TDC0N	TDC0P	TDD1N	TDD1P	TDD2N	13
12	VDDIO	GND	TCAP	TDA3P	TDA3N	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	TDD3N	TDD3P	TCDP	GND	VDDIO	12
11	TDKAP	TDKAN	TCAN	VDDIO	GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	GND	VDDIO	TCDN	TDKDN	TDKDP	11
10	RDA0P	RDA0N	RDA1P	RDA1N	RDA2P	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	RDD2P	RDD1N	RDD1P	RDD0N	RDD0P	10
9	VDDIO	GND	RCAP	RCAN	RDA2N	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	RDD2N	RCDN	RCDP	GND	VDDIO	9
8	RDA3P	RDA3N	RDKAP	RDKAN	GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	GND	RDKDN	RDKDP	RDD3N	RDD3P	8
7	VDDA	GNDA	GNDA	VDD	GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	GND	VDD	GNDA	GNDA	VDDA	7
6	VDDA	RXAN	VDDA	TXAN	GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	GND	TXDN	VDDA	RXDN	VDDA	6
5	VDDA	RXAP	VDDA	TXAP	GND	GNDA	GNDA	GND	GND	GND	GNDA	GNDA	GND	TXDP	VDDA	RXDP	VDDA	5
4	GNDA	GNDA	GNDA	VDD	VDD	TXBP	TXBN	VDD	VDD	VDD	TXCN	TXCP	VDD	VDD	GNDA	GNDA	GNDA	4
3	TCLK	TDI	LPENA	LPENB	GNDA	VDDA	VDDA	GND	RFCP	GND	VDDA	VDDA	GNDA	LPENC	LPEND	DVAD2	MDIO	3
2	TDO	TMS	CONFIG1	CONFIG0	GNDA	RXBP	RXBN	GND	RFCN	GND	RXCN	RXCP	GNDA	TESTEN	DVAD4	DVAD3	MDC	2
1	TRSTN	RSTN	PSYNC	SYNCEN	GNDA	VDDA	VDDA	VDD	CODE	VDD	VDDA	VDDA	GNDA	PRBSEN	DVAD0	DVAD1	ENABLE	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	

flow-through pin out

The TLK3104SCGNT provides a flow-through pinout that allows easy board signal trace routing without need to cross either high-speed differential serial pins or parallel LVDS pins. This flow-through pinout allows for optimum signal integrity without the need for additional board layers to isolate crossing signals. The following figure displays the flow-through pinout of the TLK3104SCGNT.

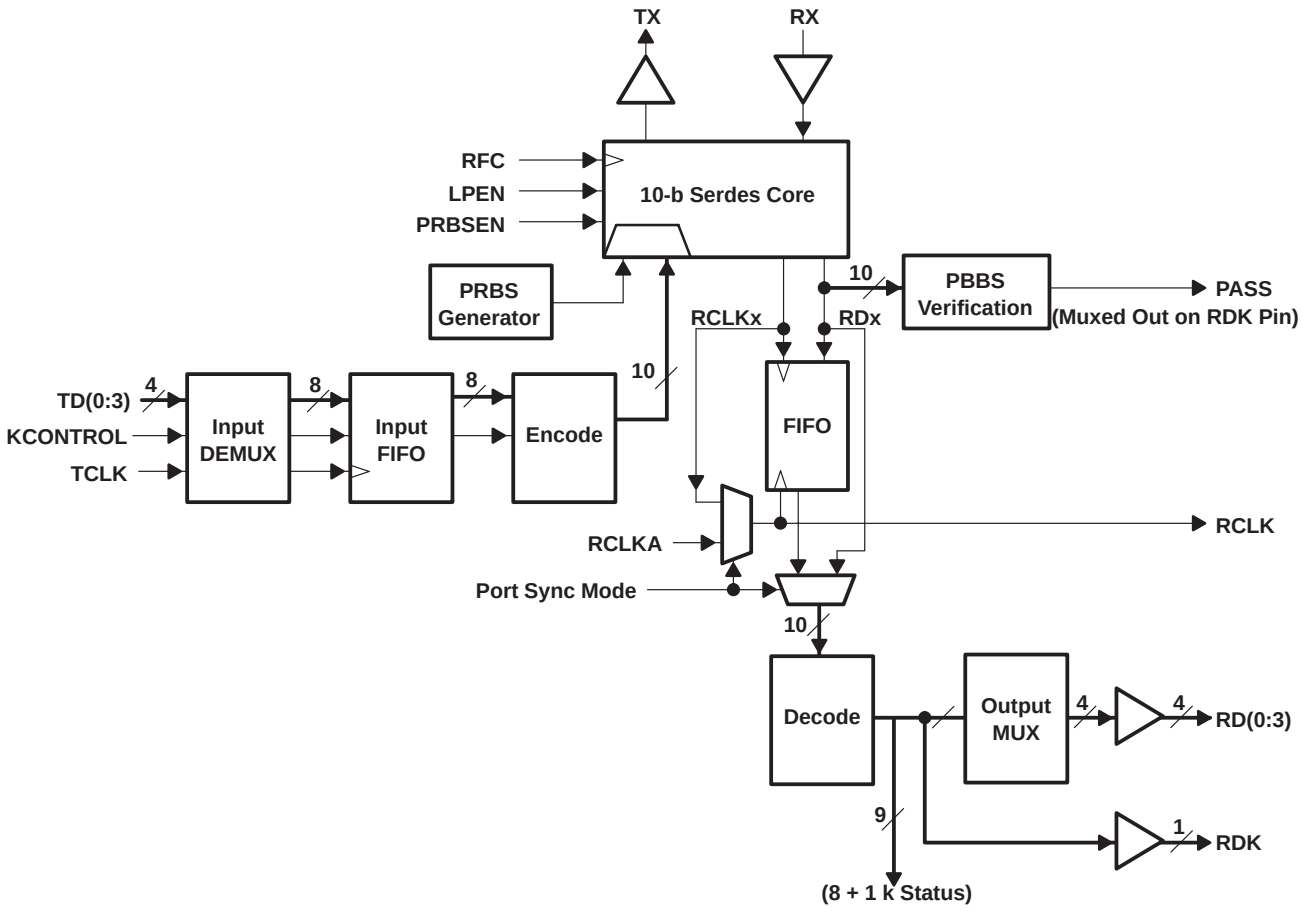


TLK3104SCGNT block diagram



detailed block diagram of individual channel

The following is a more detailed block diagram description of each channel core.



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
Clock Pins			
RFCP/RFCN	J3, J2	LVDS/LVPECL Compatible	Differential reference input clock. It could accept LVDS or LVPECL signals. When interfaced with 3.3-V LVPECL, ac coupling is required. A 100-Ω on-chip termination resistor is placed differentially.
TCAP/N, TCBP/N, TCCP/N, TCDP/N	C12, C11, D16, E16, P16, N16, R12, R11	LVDS Input	Transmit data clock, channels A−D. The data on TDx(0:3) is latched on the rising edges of the transmit clocks.
RCAP/N, RCBP/N, RCCP/N, RCDP/N	C9, D9, H16, H15, K16, K15, R9, P9	LVDS Output	Receive data clock, channels A−D. When PSYNC=low, the data on RDx(0 :3) is output on the rising edges of the receive clocks. When PSYNC = high, RCAP/N are used to clock out the data for all channels, and RCB/C/D are identical copies of RCA.
Serial Side Data Pins			
TXAP/TXAN TXBP/TXBN TXCP/TXCN TXDP/TXDN	D5, D6, F4, G4, M4, L4, P5, P6	PECL compatible output	Transmit differential pairs, channel A−D, high-speed serial outputs.
RXAP/RXAN RXBP/RXBN RXCP/RXCN RXDP/RXDN	B5, B6, F2, G2, M2, L2, T5, T6	Input	Receive differential pairs, channel A−D, high-speed serial inputs.
Parallel Side Data Pins			
TDA(0:3) P/N	B14, C14, B13, C13, A14, A13, D12, E12	LVDS Input	Transmit data pins, channel A−D, parallel data on this bus is clocked on the rising edge of TCx.
TDB(0:3) P/N	D13, E13, A16, B16, C15, D15, C17, C16		
TDC(0:3)P/N	P13, N13, U16, T16, R15, P15, R17, R16		
TDD(0:3)P/N	T14, R14, T13, R13, U14, U13, P12, N12		
TDKAP/N TDKBP/N TDKCP/N TDKDP/N	A11, B11, E15, F15, N15, M15, U11, T11	LVDS Input	K code control, channel A−D
RDA(0:3)P/N	A10, B10, C10, D10, E10, E9, A8, B8	LVDS Output	Receive data pins, channel A−D, parallel data on this bus is valid on the rising edge of RCx.
RDB(0:3)P/N	F17, F16, G16, G15, F14, F13, G13, H13		
RDC(0:3)P/N	M17, M16, L16, L15, M14, M13, L13, K13		
RDD(0:3)P/N	U10, T10, R10, P10, N10, N9, U8, T8		
RDKAP/N RDKBP/N RDKCP/N RDKDP/N	C8, D8, J14, J13, J17, J16, R8, P8	LVDS Output	Decode status, channel A−D, when PRBSEN is asserted, these pins report the PRBS test result of channel A−D.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
JTAG Interface			
TCLK	A3	TTL input	JTAG clock. TCLK is used to clock state information and test data into and out of the device during the operation of the test port.
TDI	B3	TTL input (with pullup)	JTAG input data. TDI is used to serially shift test data and test instructions into the device during the operation of the test port.
TDO	A2	TTL output	JTAG output data. TDO is used to serially shift test data and test instructions out of the device during operation of the test port.
TMS	B2	TTL input (with pullup)	JTAG mode select. TMS is used to control the state of the internal test-port controller.
TRSTN	A1	TTL input (with pullup)	JTAG reset. TRSTN is used to reset the internal JTAG controller.
Management Data Interface			
DVAD(0−4)	R1, T1, T3, T2, R2	TTL input	Management address
MDC	U2	TTL input	Management interface clock. MDC is the clock reference for the transfer of management data to and from the protocol device.
MDIO	U3	TTL I/O	Management address/data I/O. MDIO is the bidirectional serial data path for the transfer of management data to and from the protocol device.
Control Pins			
CODE	J1	TTL input (with pullup)	8-b/10-b enable. When this pin is asserted high, the on chip 8-b/10-b encoder/decoder is enabled. For testing purpose, the 8-b/10-b endec could be bypassed by driving the pin low. If intended to use bypass mode under normal operation, an 8-b/10-b or equivalent coding scheme is needed to encode the random data before it enters the TLK3104SCGNT.
CONFIG0, CONFIG1	D2, C2	TTL input (with pulldown)	Configuration pins. Put the device under one of the four operation modes: TX only, RX only, transceiver, and repeater mode.
ENABLE	U1	TTL Input (with pullup)	Standby enable. When this pin is held low, the device is disabled for IDDQ testing. When high, the device operates normally.
LPEN(A−D)	C3, D3, P3, R3	TTL input (with pulldown)	Internal loop enable, channels A−D. When high, the serial output for each channel is internally looped back to its serial input.
PRBSEN	P1	TTL input (with pulldown)	PRBS testing enable. When this pin is asserted high, the device is put into the PRBS testing mode.
PSYNC	C1	TTL input (with pulldown)	Channel synchronization enable. When PSYNC = high, the channel synchronization FIFO at the receive data path is enabled. All four channels are clocked by RCA.
RSTN	B1	TTL input (with pullup)	Chip reset. Pulsing this pin low for at least 8 RFC cycles resets the logic states for the whole chip.
SYNCEN	D1	TTL input (with pullup)	Comma detect enable. When this pin is asserted high, the comma detect circuit for byte alignment is turned on.
TESTEN	P2	TTL input (with pulldown)	Test mode enable should be left unconnected or tied low. This is for production test only.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
Voltage Supply and Reference Pins			
GND	B17, B15, B12, B9, E17, E14, E11, E8−E5, H17, H14, H5, H3, H2, J5, K17, K14, K5, K3, K2, N5−N8, N11, N14, N17, T17, T15, T12, T9	Ground	Digital logic ground. Supply reference for core logic.
GNDA	A4, B4, B7, C4, C7, E1−E3, F5, G5, L5, M5, N1−N3, R4, R7, T4, T7, U4	Ground	Analog ground. Provides ground for analog circuitry.
T−GND	F6−F12, G6−G12, H6−H12, J6−12, K6−K12, L6−L12, M6−M12	Ground	Thermal grounds. Electrically connected to GND, these pins provide a thermal path for heat dissipation.
VDD	D4, D7, E4, H1, H4, J4, K1, K4, N4, P4, P7	Supply	Core supply (2.5 V), digital logic power. Provides power for all digital circuitry.
VDDA	A5−A7, C5, C6, F1, F3, G1, G3, L1, L3, M1, M3, R5, R6, U5−U7	Supply	Analog voltage supply (2.5 V). Provides power for all analog circuitry.
VDDIO	A9, A12, A15, A17, D11, D14, D17, G14, G17, J15, L14, L17, P11, P14, P17, U9, U12, U15, U17	Supply	LVDS supply voltage (2.5 V)

detailed description

The TLK3104SCGNT has four operational modes controlled by the two configuration pins. These operational modes are listed in Table 1. When the device is put in a certain mode, unused circuit blocks are powered down to conserve the system power.

While the transceiver mode, transmit only mode, and receive only mode are straightforward, the repeater mode of operation is shown in Figure 1. The receive serial data is recovered by the extracted clock and is then sent back out on the transmit serial outputs. The data eye opens both vertically and horizontally in this process.

Table 1. Operational Modes

MODE	CONFIG0	CONFIG1	DESCRIPTION
1	0	0	Full duplex transceiver mode
2	0	1	Transmit only mode
3	1	0	Receive only mode
4	1	1	Repeater mode

detailed description (continued)

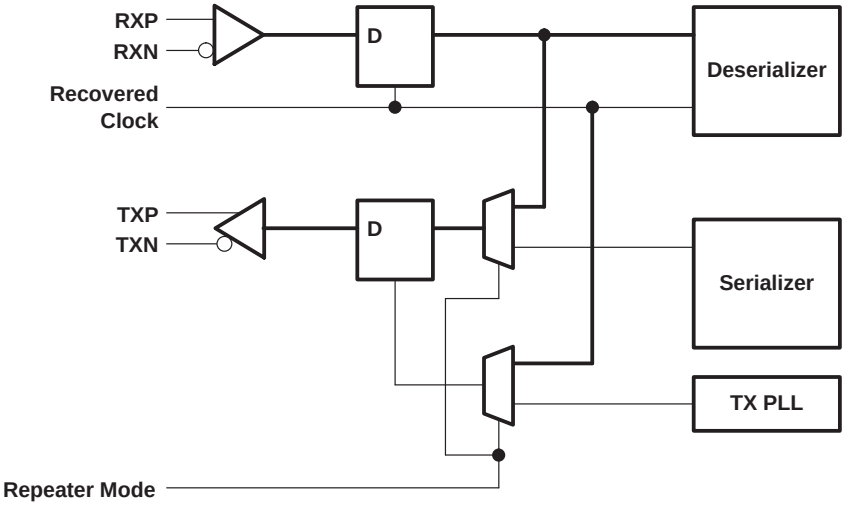


Figure 1. Repeater Mode Block Diagram

transmit interface

An external reference clock, RFCP/N is needed for the on-chip PLL and the clock/data recovery loop. A data FIFO is placed in the transmit data path to resolve any phase difference between the TCx and RFC.

The transmitter portion registers the incoming 4-bit wide data (TDx[0:3]) on the rising edge of the TCx. The parallel data is then demuxed into an 8-bit wide data bus. After going through the FIFO, which decouples the clock domain to the RFC, the 8-bit data is encoded into 10-bit data with the K code control bit, TDKx using an 8-b/10-b encoder. The data is then serialized and transmitted sequentially over the differential high-speed I/O channel. The clock multiplier multiplies the parallel data rate by a factor of five, providing the high-speed clock, which is fed to the parallel-to-serial shift register. Data is transmitted LSB (D0) first.

parallel transmit data bus

The transmit bus interface accepts 4-bit wide LVDS parallel data at the TD[0:3]x pins. A 100-Ω on-chip termination resistor is placed differentially at each LVDS input pair. The rising edge of TCx is used to latch the data (see Figure 2). Special code words, like comma, could be sent through the control of the TDKx pin. The internal demultiplexing converts the 4-bit data bus plus the TDK control bit into an 8-bit data bus plus one control bit. Figure 3 shows the data mapping used by the demux function. The byte boundary is defined by the TDK signal. When it is asserted, only the first half of the 8-bit word is pulsed, which is used to group the correct 8 bits into a byte. Table 2 shows the K codes supported by the TLK3104SCGNT.

Each LVDS input pair also supports a fail-safe operation in case that the link is broken or the LVDS driver on the other end is disabled. Under such circumstances, the LVDS input forces its output to be low until the link is reconnected or the LVDS driver is reactivated. This prevents noise from being amplified through the LVDS input circuit while there is no active data on the line.

parallel transmit data bus (continued)

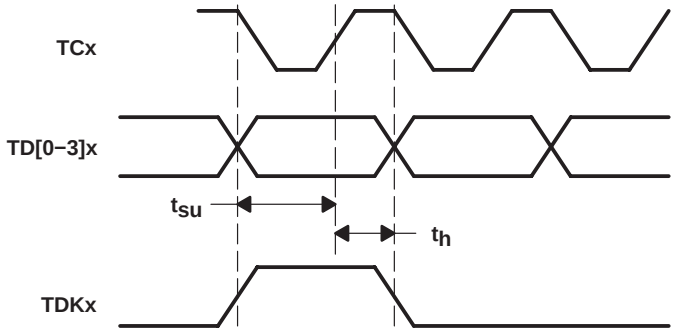


Figure 2. Transmit Timing Waveform

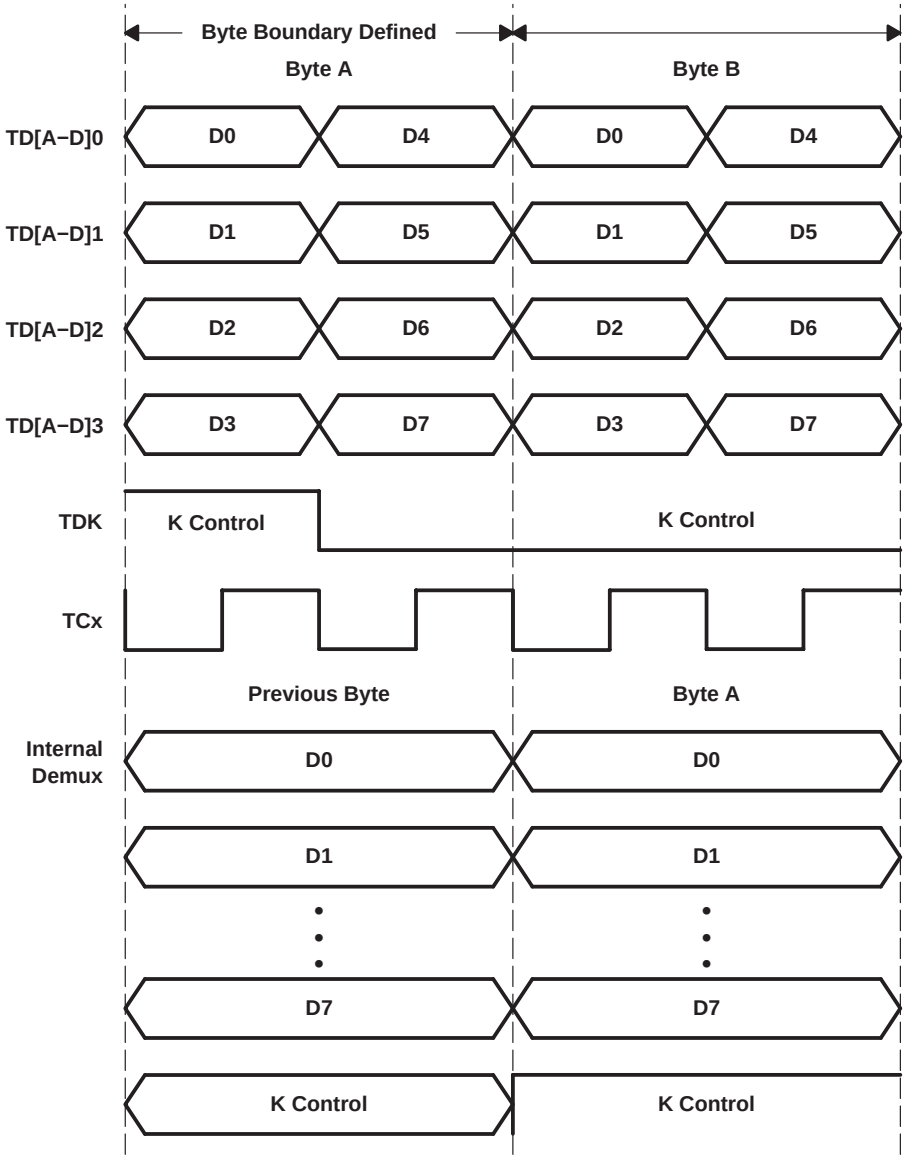


Figure 3. Transmit Data Mapping

parity error detection

The TLK3104SCGNT provides a parity checking function for the LVDS transmit data bus. The detection results are sent to a register accessible through the MDIO interface. The system can monitor the parity error detection bits via MDIO and easily isolates any link problem in the LVDS interface. The parity checker performs its function on each TDx[0:3] independently, thus 4 bits of error detection are defined in MDIO per channel. The parity checker resets when the TDKx pins are asserted high and starts to count parity one byte(8 bits) after it is reset. A parity byte is sent at the end of the data payload for even parity. Figure 4 illustrates the operation of the parity checker function.

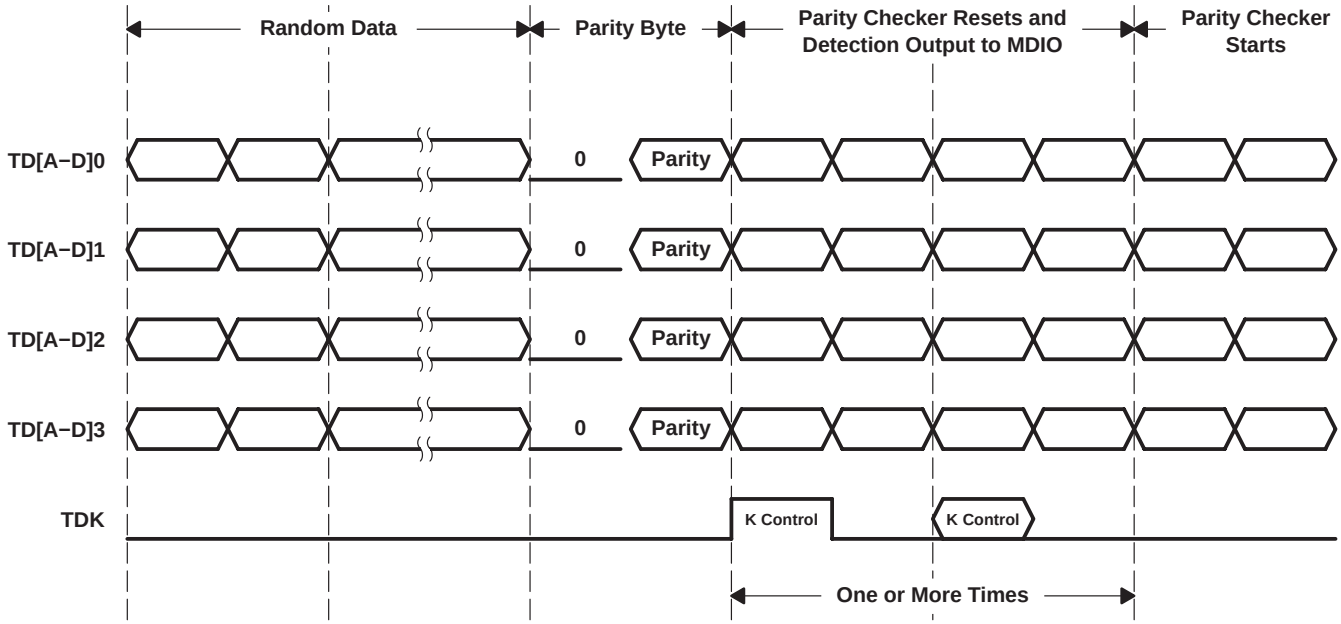
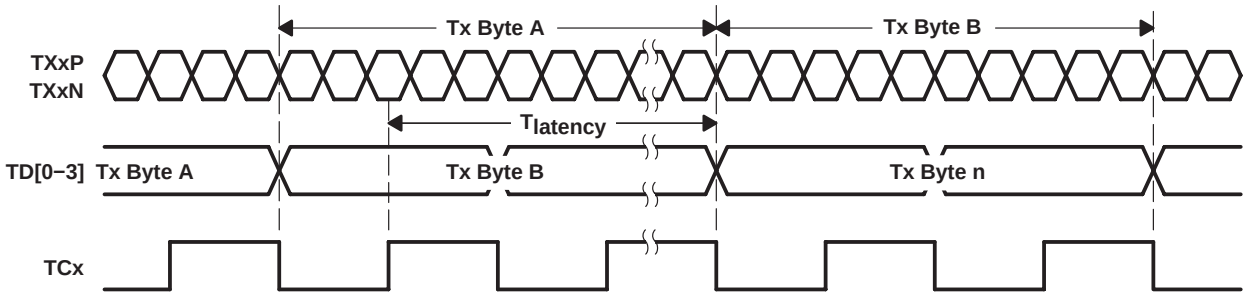


Figure 4. Parity Error Detection

transmit latency

The data transmission latency of the TLK3104SCGNT is defined as the delay from the first rising edge of TCx within a byte boundary to the serial transmission of bit 0 of the encoded 8-b/10-b byte. The minimum latency is 89 bit times; the maximum is 109 bit times.



NOTE: This figure is for illustration only.

Figure 5. Transmitter Latency

8-b/10-b encoder

All true serial interfaces require a method of encoding to insure minimum transition density so that the receiving PLL has a minimal number of transitions in which to stay locked on. The encoding scheme maintains the signal dc balance by keeping the number of ones and zeros the same. This provides good transition density for clock recovery and improves error checking. The TLK3104SCGNT uses the 8-b/10-b encoding algorithm that is used by Fibre Channel and Gigabit Ethernet. This is transparent to the user as the TLK3104SCGNT internally encodes and decodes the data such that the user reads and writes actual 8-bit data. The user controls the encoder through the TDK pin.

Table 2. Transmit Data Controls

D[7:0]	K-CONTROL	DESCRIPTION	K CODE TRANSMITTED
XX	0	Normal data transmission	X
BC	1	IdleE/not busy	K28.5
F7	1	IdleO/not busy	K23.7
3C	1	IdleE/busy	K28.1
1C	1	IdleO/busy	K28.0
FB	1	SOP(S)	K27.7
FD	1	EOP(T)	K29.7
FE	1	Error	K30.7
FC	1	Violation	K28.7

NOTE: See Figure 3 for the data-mapping diagram.

channel clock to serial transmit clock synchronization

The TLK3104SCGNT employs a FIFO in the parallel transmit data path on each channel to compensate for clock phase tolerance differences between the data aligned to the transmit data clock and the reference clock (RFCP/RFCN). This FIFO has a depth of four bytes.

The reference clock is an external clock that synchronizes the transmit data to the serial transmit output. The reference clock and the transmit data clocks are assumed to be from a common source and only phase misaligned due to different path delays as shown in Figure 6. The reference clock is multiplied in frequency 2.5x to produce the internal serialization clock, which is used to clock out the serial transmit data.

channel clock to serial transmit clock synchronization (continued)

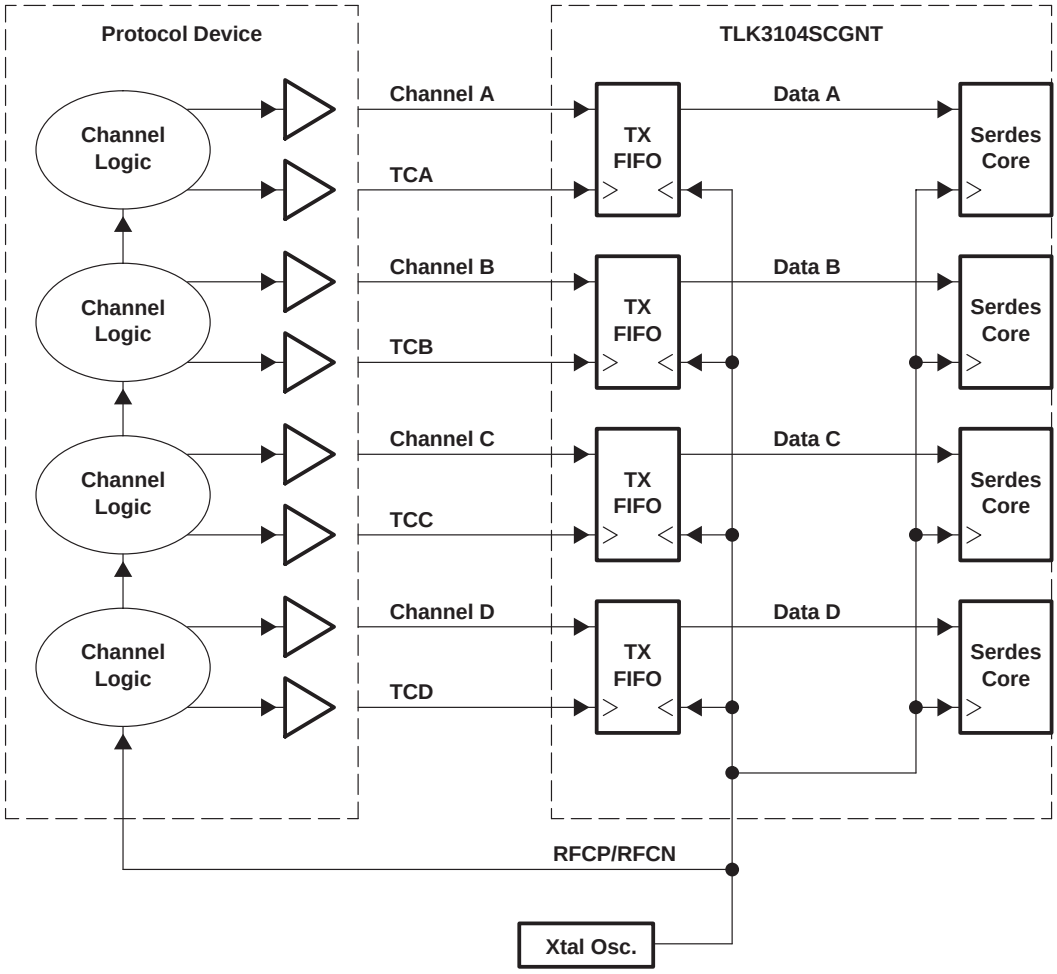


Figure 6. Transmit and Reference Clock Relationship

PRBS generator and verifier

The TLK3104SCGNT has a built-in 2^7-1 pseudo-random bit stream (PRBS) self-test function available on each channel. The generator has a polynomial equation of $1 + x^6 + x^7$. When the self-test function is enabled via the MDIO or by asserting the PRBSEN pin high, the PRBS pattern is generated and fed into the 10-bit parallel-to-serial converter. Data from the normal input source is ignored during the self-test mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a bit error rate tester (BERT), the receiver of another TLK3104SCGNT channel, or can be looped back to the receive input of the particular channel. Since the PRBS is not really random but a predetermined sequence of ones and zeroes, the data can be captured and checked for errors by a BERT.

Result reporting of the self-test is available on the RDKx pins and MDIO registers when this test mode is enabled. Through a mux controlled by PRBSEN, one bit test result (pass or fail) is sent to the RDKx pin. A high state on these pins under this test mode indicates an error free link. MDIO register 22.4 to 22.7 are also for the PRBS test indicating the status of the test and they can be accessed through the MDIO interface.

When the PRBS testing is enabled through the PRBSEN pin or MDIO, the SYNCEN pin is used for production testing only. The user needs to make sure this pin is grounded for proper PRBS testing.

parallel-to-serial shift register

The parallel-to-serial shift register takes in 10-bit wide data multiplexed from the 8-b/10-b encoder and converts it to a serial stream. The shift register is clocked by the internally generated bit clock, which is 2.5 times the RFCP/RFCN input frequency. The LSB (D0) is transmitted first.

high-speed data output driver

The high-speed data output driver consists of a PECL compatible differential pair for a 50-Ω impedance environment. The line can be directly coupled or ac-coupled. See Figure 21 and Figure 22 for termination details.

The PECL output also provides preemphasis for compensating ac loss when driving a cable or PCB backplane over long distance. The level of the preemphasis is programmable via MDIO/MDC interface. Users can software control the strength of the preemphasis to optimize for a specific system requirement. There are two control bits in the user-defined registers of MDIO to set the preemphasis level.

receive interface

The receiver portion of the TLK3104SCGNT accepts 8-b/10-b encoded differential serial data. A 100-Ω on-chip termination resistor is placed differentially at the input of the receiver. The interpolator and clock recovery circuit lock to the data stream and extract the bit rate clock. This recovered clock is used to retime the input data stream. The serial data is then aligned to the 10-bit word boundary, 8-b/10-b decoded, and output on the internal 8-bit wide parallel bus synchronized to the extracted receive clock. A K code status bit is also generated, RDKx. A 2:1 mux is placed at the end of the receive data path to convert the 8-bit data into a 4-bit data bus.

parallel data bus

The receive bus interface drives 4-bit wide LVDS parallel data at the RDx[0...3] pins. Data is valid on the rising edge of RCx. The RCx is used as the byte clock. The data and clock signals are aligned as shown in Figure 7.

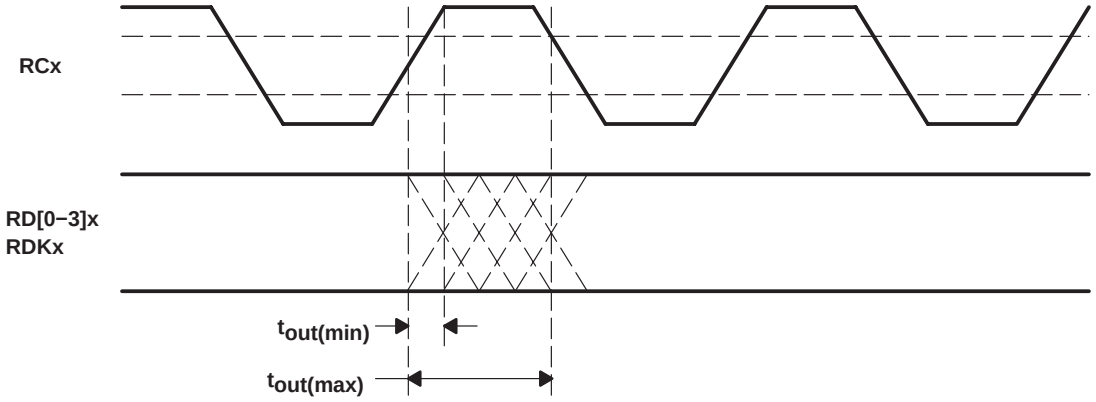


Figure 7. Receive Timing Waveform

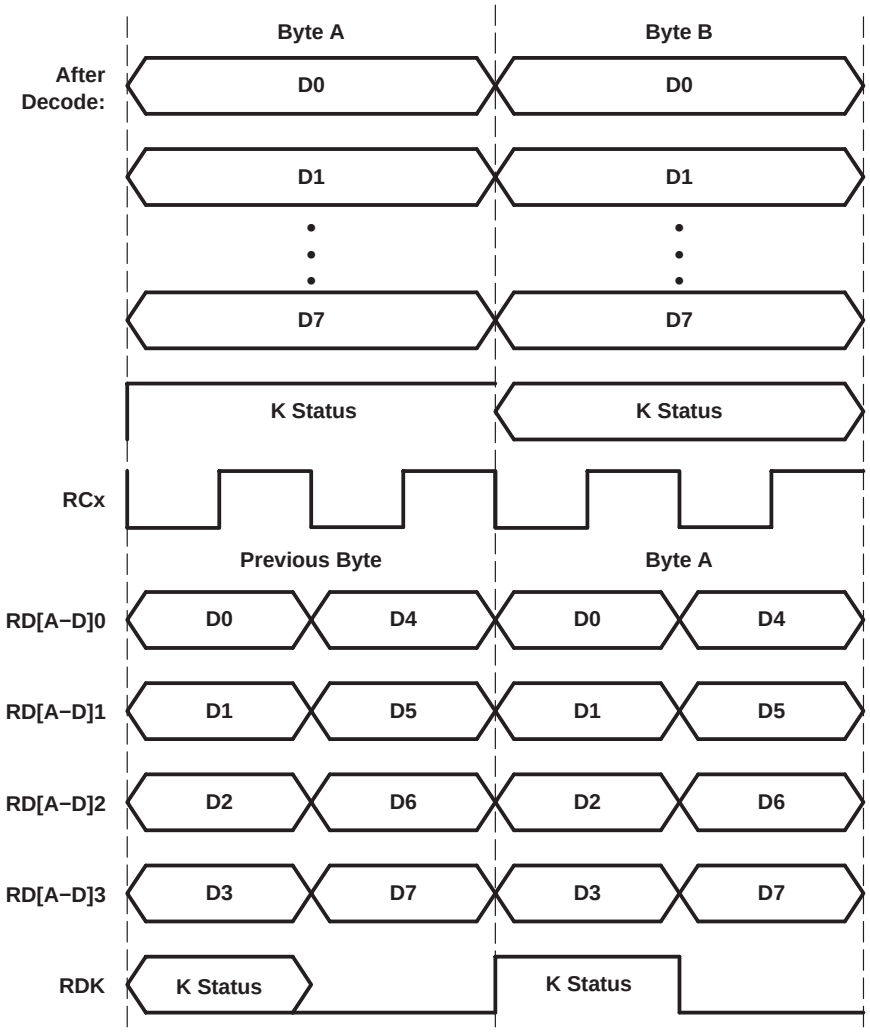
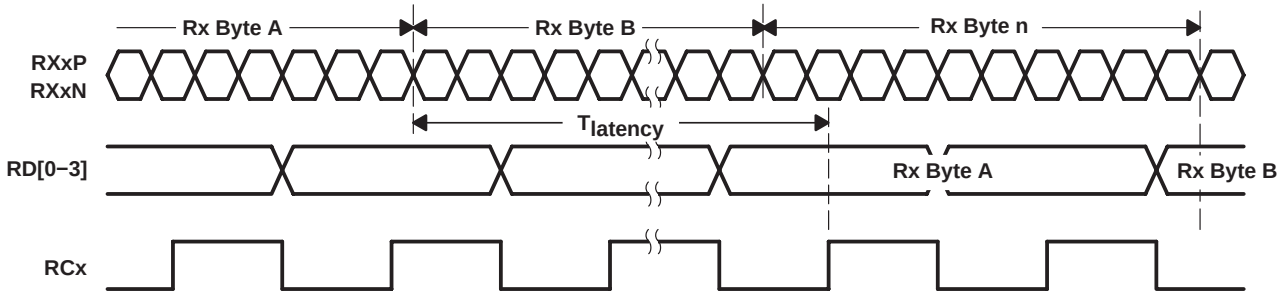


Figure 8. Receive Data Mapping

data reception latency

The serial-to-parallel data latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word with RDx0 received as first bit. The minimum latency ($T_{latency}$) is 69 bit times; the maximum is 139 bit times, with PSYNC enabled.



NOTE: This figure is for illustration only.

Figure 9. Receiver Latency

serial to parallel

For each channel, serial data is received on the RXxP, RXxN pins. The interpolator and clock recovery circuit locks to the data stream if the clock to be recovered is within ±200 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. The 10-bit wide parallel data is then fed into 8-b/10-b decoders. If the TLK3104SCGNT is configured in the channel sync mode, the parallel data for each channel is fed into a FIFO buffer where the output is synchronized to RCA. If the TLK3104SCGNT is configured in the independent channel mode, the parallel data for each channel is output synchronized to each channel's recovered clock.

comma detect and 8-b/10-b decoding

The 8-b/10-b decoder converts 10-bit encoded data back into 8 bits. The comma detect circuit is designed to provide for byte synchronization to an 8-b/10-b transmission code. When parallel data is clocked into a parallel-to-serial converter, the byte boundary that was associated with the parallel data is now lost in the serialization of the data. When the serial data is received and converted to parallel format again, a way is needed to be able to recognize the byte boundary again. This is accomplished through the use of a synchronization pattern. This is generally a unique pattern of 1s and 0s that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. The 8-b/10-b encoding contains a character called the comma (b'0011111'), which is used by the comma detect circuit to align the received serial data back to its original byte boundary. The decoder detects the comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding. It then converts the data back into 8-bit data and 1-bit control. Table 3 shows the decoding on this 8-bit data, one control bit parallel bus. This bus then goes through a 2 to 1 multiplexer to form a 4-bit data, 1-bit control to the LVDS interface. The data mapping diagram for the mux function is shown in Figure 8.

loss of signal detection (LOS)

The TLK3104SCGNT has a loss of signal detection circuit for conditions where the incoming signal no longer has a sufficient voltage level to keep the clock recovery circuit in lock. The signal detection circuit indicates gross signal error conditions such as a detached cable or no signal being transmitted. It is not an indication of signal coding health. The TLK3104SCGNT reports this condition by asserting RDx to a zero state and the MDIO bits (register 22) are also set accordingly. The LOS reporting function at the RDx can be disabled by setting MDIO bit 8 of register 16−20.

loss of signal detection (LOS) (continued)

Table 3. Receive Data Controls

RDKx	RECEIVE DATA BUS (RDx[7:0])	EVENT
0	XX	Normal data
1	Valid K code (see Table 4)	Normal K-character
1	00	Loss of signal (LOS)
1	FF	Code word error or running disparity error

Table 4. Valid K Characters

K CHARACTER	RECEIVE DATA BUS (RDx[7:0])
K28.0	000 11100
K28.1	001 11100
K28.2	010 11100
K28.3	011 11100
K28.4	100 11100
K28.5	101 11100
K28.6	110 11100
K28.7	111 11100
K23.7	111 10111
K27.7	111 11011
K29.7	111 11101
K30.7	111 11110

channel-to-channel synchronization and skew compensation

The TLK3140SC can be configured in channel sync mode or channel independent mode for its receive parallel bus. This is controlled by the PSYNC pin.

Table 5. Receive Parallel Data Bus Clocking Modes

PSYNC	OPERATION
0	Channel independent mode. Each channel is operated as an individual.
1	Channel Sync mode. A FIFO is used to deskew the four receive channels.

When the TLK3104SCGNT is configured in channel sync mode, a FIFO is enabled in the parallel receive data path on each channel to compensate for channel skew and clock phase differences between the recovered clocks for each channel and the receive output clock RCA as shown in Figure 10. RCA is used to clock out the data for all four channels. RCB/C/D, the receive clock for channel B/C/D, are the same as the RCA. The FIFO is designed to resolve the skew between the four serial channels up to 10-serial bit times and align the data bits to the RCA clock.

channel to channel synchronization and skew compensation (continued)

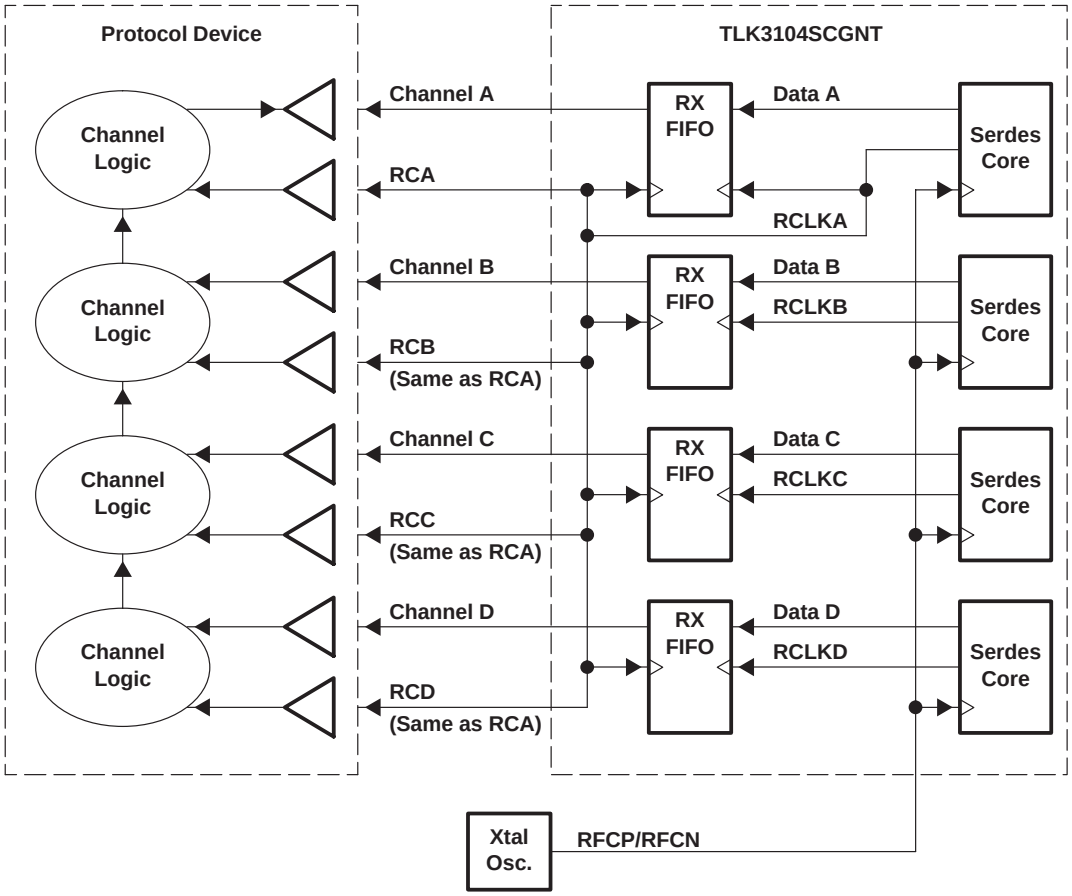


Figure 10. Receive and Reference Clock Relationship (Channel Sync Mode)

channel-to-channel synchronization and skew compensation (continued)

When the TLK3104SCGNT is configured in the independent channel mode, the recovered clocks for each channel are used to output the received data on the parallel interface. Thus, as is shown in Figure 11, in the independent channel modes, no FIFO is enabled.

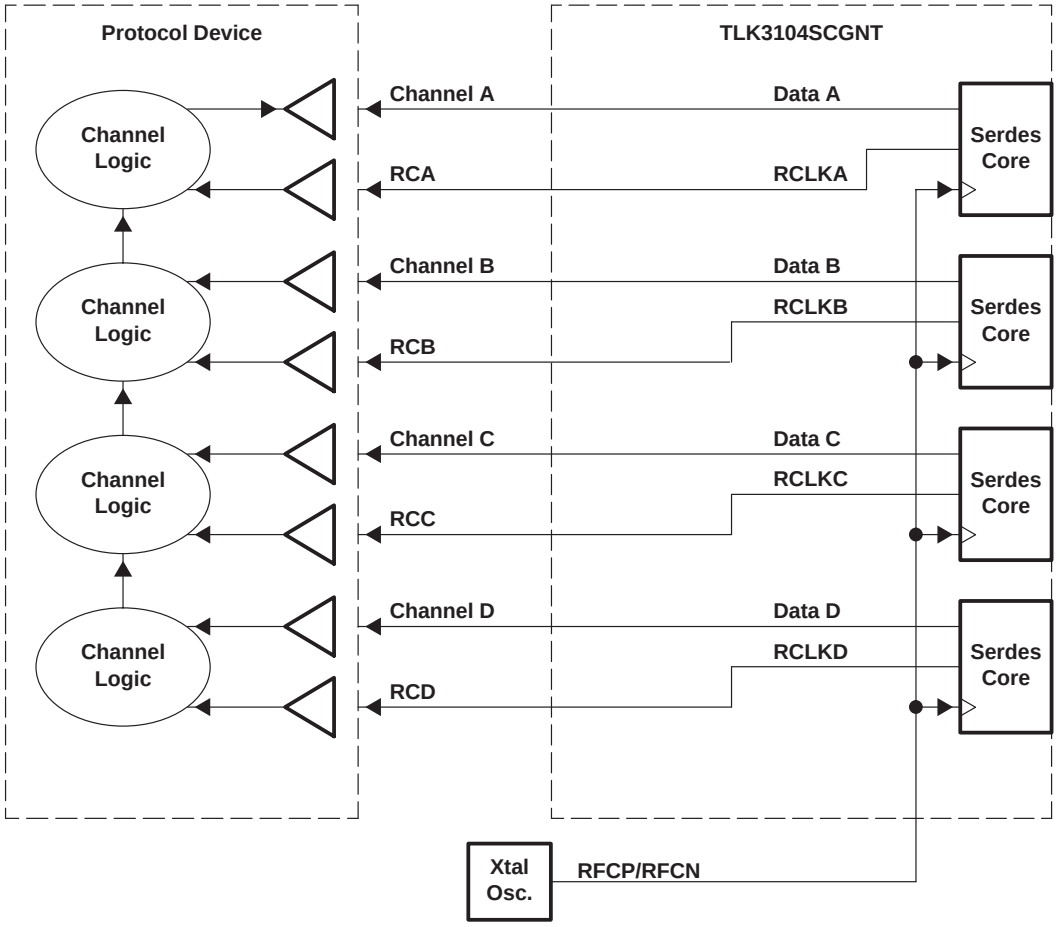


Figure 11. Receive and Reference Clock Relationship (Independent Channel Modes)

DIS/SEL functions

The DIS/SEL functions enable the system designers to configure the TLK3104SC into a two-port device with full redundancy for system reliability. Under the DIS (distribution) mode, the transmit parallel data of channel A, TDA(0:3) and TDKA, is serialized and sent to both serial sides of channel A and channel B. The transmit parallel data of channel D, TDD(0:3) and TDKD, is also processed and distributed to both serial sides of channel C and channel D. Figure 12 illustrates how the data flows under the DIS mode.

The SEL (selection) function is for the receive side. Under this mode, system designers can select which serial ports get passed to the parallel receive outputs. The serial data of channel A or channel B could be selected, and the recovered data is sent to the parallel side of channel A, RDA(0:3) and RDKA. Meanwhile, the users can choose between channel C and channel D for serial data, and the recovered data is sent to the parallel side of channel D, RDD(0:3) and RDKD. The serial data of the unselected port is still processed and the user can monitor the data by checking decode error status and LOS status via MDIO. Figure 13 shows how this function works.

The DIS/SEL functions are controlled by MDIO register bits. There are four bits allocated for this function. Details on register assignment can be found in the MDIO section.

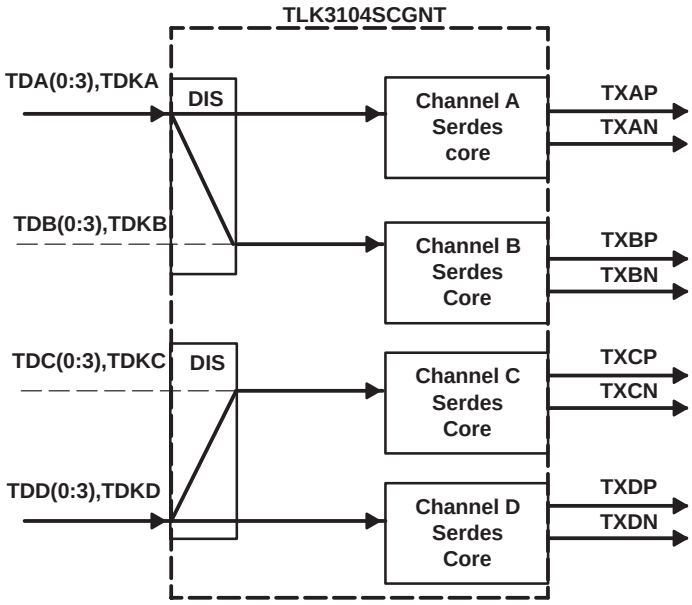


Figure 12. DIS Mode Operation

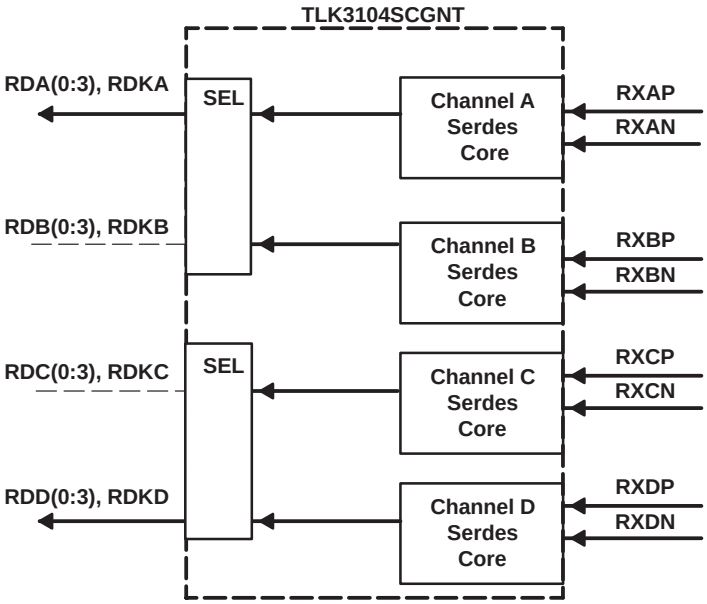


Figure 13. SEL Mode Operation

MDIO/MDC management interface

The TLK3104SCGNT supports the management interface (MDIO) as defined in clause 22 of the IEEE 802.3 Ethernet specification. The MDIO allows register-based management and control of the serial links. Normal operations of the TLK3104SCGNT are possible without use of this interface since all of the essential signals necessary for operations are accessible via the device pins. However, some additional features are accessible only through the MDIO.

MDIO/MDC management interface (continued)

The MDIO management interface consists of a bidirectional data path (MDIO) and a clock reference (MDC). The timing required to read to the internal registers is shown in Figure 14. The timing required to write from the internal registers is shown in Figure 15. The TLK3104SCGNT reads in and latches out register bits on the rising edge of the MDC clock and it could run as fast as 10 MHz. The MDIO controller, on the other hand, drives and reads MDIO on falling edge of the MDC clock.

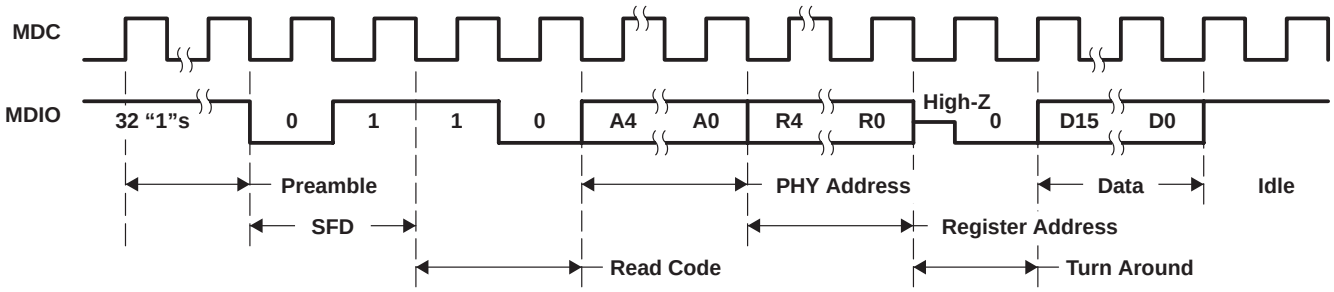


Figure 14. Management Interface Read Timing

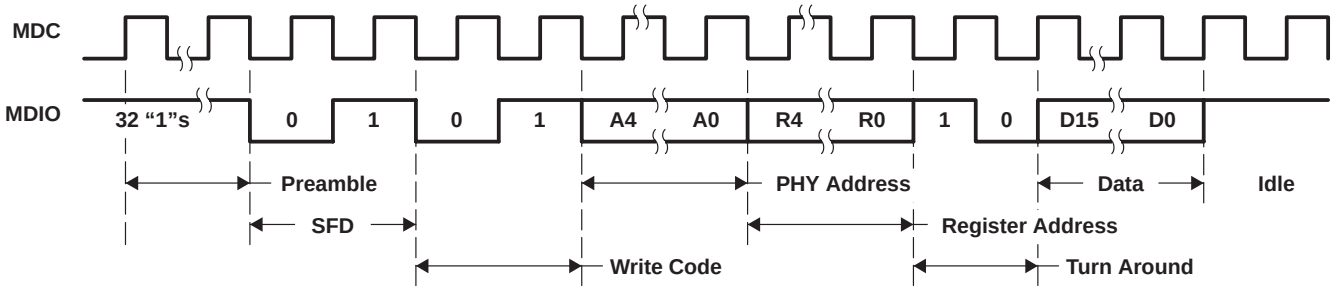


Figure 15. Management Interface Write Timing

The MDIO management interface allows up to 32 (16 bit) internal registers. Sixteen registers are defined by the IEEE 802.3 clause 22 specification. Additional registers are allowed for expanded functionality. The TLK3104SCGNT implements five IEEE defined registers. The TLK3104SCGNT also implements eight registers for expanded functionality. Both the IEEE defined registers and the expanded functionality registers are outlined in Table 6.

Table 6. MDIO Registers

REGISTER ADDRESS	REGISTER NAME	DEFINITION
0	Control	IEEE 802.3 defined. See Table 7
1	Status	IEEE 802.3 defined. See Table 8
2,3	PHY identifier	IEEE 802.3 defined. See Table 9
4−14	Not applicable	
15	Extended status	IEEE 802.3 defined. See Table 10
16	Global configuration	See Table 11
17:20	Channel A−D configuration	See Tables 12, 13, 14, and 15
21	Test register	For production test only.
22	Channel status	See Table 16
23	Parity error detection	See Table 17
24	Channel synchronization FIFO	See Table 18

detailed description (continued)

Table 7. Control Register Bit Definitions (Register 0)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
0.15	Reset	Logically OR'ed with the inverse of RSTN pin. 1 = Global resets including FIFO clear 0 = Normal operation	Read/write self clearing†
0.14	Loopback	1 = Enable loopback mode on all channels 0 = Disable loopback mode on all channels (default)	Read/write
0.13	Speed selection (LSB)	Not applicable. Read returns a 1.	Read only
0.12	Auto-negotiation enable	Not applicable. Read returns a 0.	Read only
0.11	Power down	Logically OR'ed with the inversion of the ENABLE pin. 1 = Power down mode is enabled 0 = Normal operation (default)	Read/write
0.10	Isolate	Not applicable. Read returns a 0.	Read only
0.9	Restart auto-negotiation	Not applicable. Read returns a 0.	Read only
0.8	Duplex mode	Only full duplex is supported. Write is ignored, read returns a 1.	Read only
0.7	Collision test	Not applicable. Read returns a 0.	Read only
0.6	Speed selection (MSB)	Not applicable. Read returns a 1.	Read only
0.5:0	Reserved	Write as 0. Ignore on read	

† After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 8. Status Register Bit Definitions (Register 1)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
1.15:9		Read returns a 0.	Read only
1.8	Extended status	Read returns a 1 indicating extended status information is held in register 15.	Read only
1.7	Reserved	Ignore when read.	Read only
1.6:3	Various configurations	Read returns a 0.	Read only
1.2	Link status	1 = Link is up 0 = Link is down	Read only
1.1	Jabber detect	Read returns a 0	Read only
1.0	Extended capability	Read returns a 1 indicating extended register capability	Read only

Table 9. PHY Identifier Bit Definitions (Register 2, 3)

Register 2 and 3 are read only registers and they are hard coded as the following:
Register 2(15:0): 0100,0000,0000,0000
Register 3(15:0): 0110,0000,0001,0000

Table 10. Extended Status Register Bit Definitions (Register 15)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
15.15:12	Various configurations	Read returns a 0.	Read only
15.11:0	Reserved	Ignore when read	Read only

detailed description (continued)

Table 11. Global Configuration Register Bit Definitions (Register 16)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
16.15:13	Reserved	Ignore when read	Read only
16.12	Serial port selection S1	In the SEL mode, this bit selects serial ports from channel C or channel D. 1 = Select serial port of channel C 0 = Select serial port of channel D (default)	Read/write
16.11	Serial port selection S0	In the SEL mode, this bit selects serial ports from channel A or channel B. 1 = Select serial port of channel B 0 = Select serial port of channel A (default)	Read/write
16.10	SEL (selection) mode enable	1 = Enable of the SEL mode 0 = SEL mode disabled (default)	Read/write
16.9	DIS (distribution) mode enable	1 = Enable of the DIS mode 0 = DIS mode disabled (default)	Read/write
16.8	LOS output enable	1 = Enable the reporting of LOS condition described in Table 3 for all channels. 1 is the default. 0 = Disable the above function	Read/write
16.7	Configuration: Config1	Configuration bits. See Table 1, default value = 0	Read/write
16.6	Configuration: Config0	Configuration bits. See Table 1, default value = 0	Read/write
16.5	Preemphasis: Pre2	Programmable preemphasis control (see the *electrical characteristics* section), default value = 0	Read/write
16.4	Preemphasis: Pre1	Programmable preemphasis control (see the *electrical characteristics* section), default value = 0	Read/write
16.3	Reserved	Ignore when read	Read only
16.2	PRBS enable	1 = Enable pseudo-random bit stream internal generation and verification on all channels 0 = Normal operation (default)	Read/write
16.1	Comma detect enable	1 = Enable comma detection and bit alignment on all channels (default) 0 = Disable comma detection on all channels	Read/write
16.0	Reserved	Ignore when read	Read only

Table 12. Channel A Configuration Registers Bit Definitions (Register 17)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
17.15:9	Reserved	Ignore when read	Read only
17.8	LOS output enable	1 = Enable the reporting of LOS condition described in Table 3 for channel A (default) 0 = Disable the above function.	Read/write
17.7	Configuration: Config1	Configuration bits (see Table 1), default value = 0	Read/write
17.6	Configuration: Config0	Configuration bits (see Table 1), default value = 0	Read/write
17.5	Preemphasis: Pre2	Programmable preemphasis control (see the *electrical characteristics* section), default value = 1	Read/write
17.4	Preemphasis: Pre1	Programmable preemphasis control (see the *electrical characteristics* section), default value = 1	Read/write
17.3	Loopback	1 = Enable loopback mode on channel A. 0 = Disable loopback mode on channel A (default). Logically OR'ed with register bit 0.14	Read/write
17.2	PRBS enable	1 = Enable pseudo-random bit stream internal generation and verification on channel A 0 = Normal operation (default). Logically OR'ed with register bit 16.2	Read/write
17.1	Comma detect enable	1 = Enable comma detection and bit alignment on channel A (default). 0 = Disable comma detection on channel A. Logically OR'ed with register bit 16.1	Read/write
17.0	Power down	1 = Power-down mode is enabled for channel A. 0 = Normal operation (default). Logically OR'ed with register bit 0.11	Read/write

detailed description (continued)

Table 13. Channel B Configuration Registers Bit Definitions (Register 18)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
18.15:9	Reserved	Ignore when read	Read only
18.8	LOS output enable	1 = Enable the reporting of LOS condition described in Table 3 for all channels (default) 0 = Disable the above function.	Read/write
18.7	Configuration: Config1	Configuration bits (see Table 1), default value = 0	Read/write
18.6	Configuration: Config0	Configuration bits (see Table 1), default value = 0	Read/write
18.5	Preemphasis: Pre2	Programmable preemphasis control (see the *electrical characteristics* section), default value = 0	Read/write
18.4	Preemphasis: Pre1	Programmable preemphasis control (see the *electrical characteristics* section), default value = 0	Read/write
18.3	Loopback	1 = Enable loopback mode on channel B. 0 = Disable loopback mode on channel B (default). Logically OR'ed with register bit 0.14	Read/write
18.2	PRBS enable	1 = Enable pseudo-random bit stream internal generation and verification on channel B 0 = Normal operation (default) Logically OR'ed with register bit 16.2	Read/write
18.1	Comma detect enable	1 = Enable comma detection and bit alignment on channel B (default). 0 = Disable comma detection on channel B. Logically OR'ed with register bit 16.1	Read/write
18.0	Power down	1 = Power-down mode is enabled for channel B. 0 = Normal operation (default). Logically OR'ed with register bit 0.11	Read/write

Table 14. Channel C Configuration Registers Bit Definitions (Register 19)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
19.15:7	Reserved	Ignore when read	Read only
19.8	LOS output enable	1 = Enable the reporting of LOS condition described in Table 3 for all channels (default) 0 = Disable the above function.	Read/write
19.7	Configuration: Config1	Configuration bits (see Table 1), default value = 0	Read/write
19.6	Configuration: Config0	Configuration bits (see Table 1), default value = 0	Read/write
19.5	Preemphasis: Pre2	Programmable preemphasis control (see the *electrical characteristics* section), default value = 0	Read/write
19.4	Preemphasis: Pre1	Programmable preemphasis control (see the *electrical characteristics* section), default value = 0	Read/write
19.3	Loopback	1 = Enable loopback mode on channel C. 0 = Disable loopback mode on channel C (default). Logically OR'ed with register bit 0.14	Read/write
19.2	PRBS enable	1 = Enable pseudo-random bit stream internal generation and verification on channel C 0 = Normal operation (default) Logically OR'ed with register bit 16.2	Read/write
19.1	Comma detect enable	1 = Enable comma detection and bit alignment on channel C (default). 0 = Disable comma detection on channel C. Logically OR'ed with register bit 16.1	Read/write
19.0	Power down	1 = Power-down mode is enabled for channel C. 0 = Normal operation (default). Logically OR'ed with register bit 0.11	Read/write

detailed description (continued)

Table 15. Channel D Configuration Registers Bit Definitions (Register 20)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
20.15:7	Reserved	Ignore when read	Read only
20.8	LOS output enable	1 = Enable the reporting of LOS condition described in Table 4 for channel D (default) 0 = Disable the above function.	Read/write
20.7	Configuration: Config1	Configuration bits (see Table 1), default value = 0	Read/write
20.6	Configuration: Config0	Configuration bits (see Table 1), default value = 0	Read/write
20.5	Preemphasis: Pre2	Programmable preemphasis control (see the *electrical characteristics* section), default value = 0	Read/write
20.4	Preemphasis: Pre1	Programmable preemphasis control (see the *electrical characteristics* section), default value = 0	Read/write
20.3	Loopback	1 = Enable loopback mode on channel D. 0 = Disable loopback mode on channel D (default). Logically OR'ed with register bit 0.14	Read/write
20.2	PRBS enable	1 = Enable pseudo-random bit stream internal generation and verification on channel D 0 = Normal operation (default) Logically OR'ed with register bit 16.2	Read/write
20.1	Comma detect enable	1 = Enable comma detection and bit alignment on channel D (default). 0 = Disable comma detection on channel D. Logically OR'ed with register bit 16.1	Read/write
20.0	Power down	1 = Power-down mode is enabled for channel D. 0 = Normal operation (default). Logically OR'ed with register bit 0.11	Read/write

detailed description (continued)

Table 16. Channel Status Register (Register 22)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
22.15	Channel D input FIFO collision error	1 = Collision error is detected to cause the FIFO self reset. 0 = No error After being read, this bit is reset to zero.	Read only
22.14	Channel C input FIFO collision error	1 = Collision error is detected to cause the FIFO self reset. 0 = No error After being read, this bit is reset to zero.	Read only
22.13	Channel B input FIFO collision error	1 = Collision error is detected to cause the FIFO self reset. 0 = No error After being read, this bit is reset to zero.	Read only
22.12	Channel A input FIFO collision error	1 = Collision error is detected to cause the FIFO self reset. 0 = No error After being read, this bit is reset to zero.	Read only
22.11	Channel D decode error	1 = Code word or running disparity error detected. 0 = No error After being read, this bit is reset to zero.	Read only
22.10	Channel C decode error	1 = Code word or running disparity error detected. 0 = No error After being read, this bit is reset to zero.	Read only
22.9	Channel B decode error	1 = Code word or running disparity error detected. 0 = No error After being read, this bit is reset to zero.	Read only
22.8	Channel A decode error	1 = Code word or running disparity error detected. 0 = No error After being read, this bit is reset to zero.	Read only
22.7	Channel D PRBS pass	1 =PRBS testing passes without error 0 = Error is detected during PRBS test After being read, this bit is reset to one.	Read only
22.6	Channel C PRBS pass	1 = PRBS testing passes without error 0 = Error is detected during PRBS test After being read, this bit is reset to one.	Read only
22.5	Channel B PRBS pass	1 = PRBS testing passes without error 0 = Error is detected during PRBS test After being read, this bit is reset to one.	Read only
22.4	Channel A PRBS pass	1 = PRBS testing passes without error 0 = Error is detected during PRBS test After being read, this bit is reset to one.	Read only
22.3	Channel D LOS output	1 = LOS condition is reported. 0 = No LOS After being read, this bit is reset to zero.	Read only
22.2	Channel C LOS output	1 = LOS condition is reported. 0 = No LOS After being read, this bit is reset to zero.	Read only
22.1	Channel B LOS output	1 = LOS condition is reported. 0 = No LOS After being read, this bit is reset to zero.	Read only
22.0	Channel A LOS output	1 = LOS condition is reported. 0 = No LOS After being read, this bit is reset to zero.	Read only

detailed description (continued)

Table 17. Parity Error Detection Register (Register 23)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
23.15	Channel D, bit 3	1 = Parity error detected on TDD3 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.14	Channel D, bit 2	1 = Parity error detected on TDD2 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.13	Channel D, bit 1	1 = Parity error detected on TDD1 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.12	Channel D, bit 0	1 = Parity error detected on TDD0 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.11	Channel C, bit 3	1 = Parity error detected on TDC3 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.10	Channel C, bit 2	1 = Parity error detected on TDC2 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.9	Channel C, bit 1	1 = Parity error detected on TDC1 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.8	Channel C, bit 0	1 = Parity error detected on TDC0 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.7	Channel B, bit 3	1 = Parity error detected on TDB3 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.6	Channel B, bit 2	1 = Parity error detected on TDB2 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.5	Channel B, bit 1	1 = Parity error detected on TDB1 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.4	Channel B, bit 0	1 = Parity error detected on TDB0 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.3	Channel A, bit 3	1 = Parity error detected on TDA3 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.2	Channel A, bit 2	1 = Parity error detected on TDA2 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.1	Channel A, bit 1	1 = Parity error detected on TDA1 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only
23.0	Channel A, bit 0	1 = Parity error detected on TDA0 differential lines 0 = No parity error detected. After being read, this bit is reset to zero.	Read only

Table 18. Channel Synchronization FIFO Register (Register 24)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
24.15:5	Reserved	Ignore when read	Read only
24.4	Channel resync	1 = Indicates the FIFO has been reset After being read, this bit is reset to zero	Read only
24.3	FIFO collision, channel D	1 = FIFO collision condition detected in channel D 0 = No collision detected After being read, this bit is reset to zero.	Read only
24.2	FIFO collision, channel C	1 = FIFO collision condition detected in channel C 0 = No collision detected After being read, this bit is reset to zero.	Read only
24.1	FIFO collision, channel B	1 = FIFO collision condition detected in channel B 0 = No collision detected After being read, this bit is reset to zero.	Read only
24.0	FIFO collision, channel A	1 = FIFO collision condition detected in channel A 0 = No collision detected After being read, this bit is reset to zero.	Read only

The control functions of the TLK3104SCGNT can be set through the MDIO interface and most of the functions could also be set through pins as well. Table 19 summarizes the control function configuration in TLK3104SCGNT.

Table 19. Control Function Setting

CONTROL FUNCTION	ACCESSIBILITY	DEFAULT	FINAL VALUE
CONFIG0	Pin D2	0	
	MDIO bit: 16.6 for global	0	
	17.6 for channel A	0	Channel A: OR function of pin D2, 16.6 and 17.6
	18.6 for channel B	0	Channel B: OR function of pin D2, 16.6 and 18.6
	19.6 for channel C	0	Channel C: OR function of pin D2, 16.6 and 19.6
	20.6 for channel D	0	Channel D: OR function of pin D2, 16.6 and 20.6
CONFIG1	Pin C2	0	
	MDIO bit: 16.7 for global	0	
	17.7 for channel A	0	Channel A: OR function of pin D2, 16.7 and 17.7
	18.7 for channel B	0	Channel B: OR function of pin D2, 16.7 and 18.7
	19.7 for channel C	0	Channel C: OR function of pin D2, 16.7 and 19.7
	20.7 for channel D	0	Channel D: OR function of pin D2, 16.7 and 20.7
Loopback	Pin C3 for channel A	0	
	D3 for channel B	0	
	P3 for channel C	0	Channel A: OR function of pin C3, 0.14 and 17.3
	R3 for channel D	0	Channel B: OR function of pin D3, 0.14 and 18.3
	MDIO bit: 0.14 for global	0	Channel C: OR function of pin P3, 0.14 and 19.3
	17.3 for channel A	0	Channel D: OR function of pin R3, 0.14 and 20.3
	18.3 for channel B	0	
	19.3 for channel C	0	
	20.3 for channel D	0	
PRBSEN	Pin P1	0	
	MDIO bit: 16.2 for global	0	
	17.2 for channel A	0	Channel A: OR function of pin P1, 16.2 and 17.2
	18.2 for channel B	0	Channel B: OR function of pin P1, 16.2 and 18.2
	19.2 for channel C	0	Channel C: OR function of pin P1, 16.2 and 19.2
	20.2 for channel D	0	Channel D: OR function of pin P1, 16.2 and 20.2
Comma detect enable/ Syncen	Pin D1	1	
	MDIO bit: 16.1 for global	1	
	17.1 for channel A	1	Channel A: AND function of pin D1, 16.1 and 17.1
	18.1 for channel B	1	Channel B: AND function of pin D1, 16.1 and 18.1
	19.1 for channel C	1	Channel C: AND function of pin D1, 16.1 and 19.1
	20.1 for channel D	1	Channel D: AND function of pin D1, 16.1 and 20.1

Table 19. Control Function Setting (Continued)

CONTROL FUNCTION	ACCESSIBILITY	DEFAULT	FINAL VALUE
Power down	Pin U1 (enable pin)	1	
	MDIO bit: 0.11 for global	0	
	17.0 for channel A	0	Channel A: OR function of the inversion of pin U1, 0.11 and 17.0
	18.0 for channel B	0	Channel B: OR function of the inversion of pin U1, 0.11 and 18.0
	19.0 for channel C	0	Channel C: OR function of the inversion of pin U1, 0.11 and 19.0
	20.0 for channel D	0	Channel D: OR function of the inversion of pin U1, 0.11 and 20.0
TESTEN	Pin P2	0	Set by pin P2
Pre1	MDIO bit: 16.4 for global	0	
	17.4 for channel A	0	Channel A: OR function 16.4 and 17.4
	18.4 for channel B	0	Channel B: OR function 16.4 and 18.4
	19.4 for channel C	0	Channel C: OR function 16.4 and 19.4
	20.4 for channel D	0	Channel D: OR function 16.4 and 20.4
Pre2	MDIO bit: 16.5 for global	0	
	17.5 for channel A	0	Channel A: OR function 16.5 and 17.5
	18.5 for channel B	0	Channel B: OR function 16.5 and 18.5
	19.5 for channel C	0	Channel C: OR function 16.5 and 19.5
	20.5 for channel D	0	Channel D: OR function 16.5 and 20.5
LOS output enable	MDIO bit: 16.8 for global	1	
	17.8 for channel A	1	Channel A: AND function of 16.8 and 17.8
	18.8 for channel B	1	Channel B: AND function of 16.8 and 18.8
	19.8 for channel C	1	Channel C: AND function of 16.8 and 19.8
	20.8 for channel D	1	Channel D: AND function of 16.8 and 20.8
PSYNC	Pin C1	0	Set by Pin C1
RSTN/reset	Pin B1	1	OR function of the inverse of pin B1 and 0.15.
	MDIO bit: 0.15	0	
CODE	Pin J1	1	Set by pin J1

8-b/10-b bypass

For bench and production testing, the on chip 8-b/10-b encoder/decoder could be bypassed through the CODE pin. The TDKx and RDKx are the fifth data bit for the transmit and receive interface respectively, and the TLK3104SCGNT works as a 5-bit serdes under this mode. If used under normal data transmission, 8-b/10-b or an equivalent coding scheme is needed to encode the random data before it enters the TLK3104SCGNT. Figure 16 shows the transmit data mapping under the 8-b/10-b bypass mode.

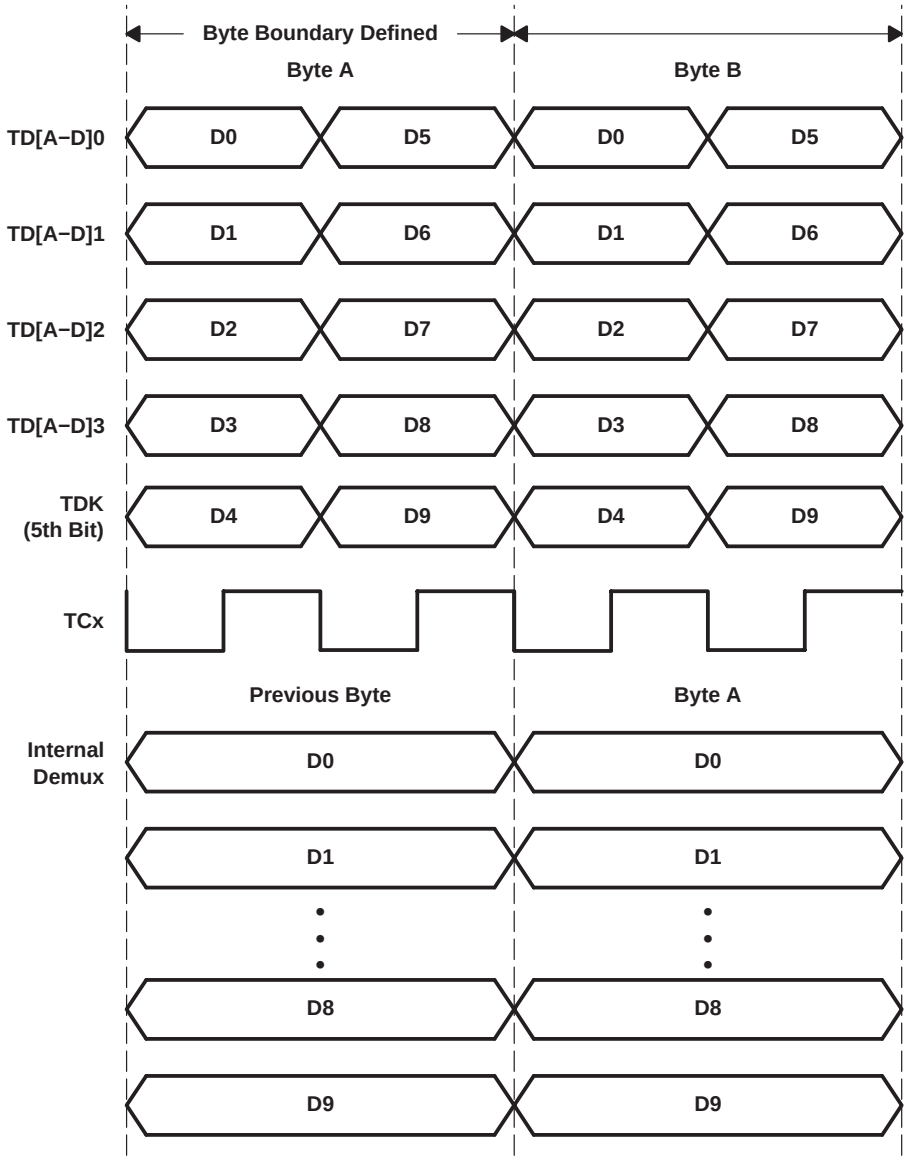


Figure 16. Transmit Data Mapping Under 8-b/10-b Bypass

chip reset

The TLK3104SCGNT has a RSTN pin to reset all the logic states. Users can pulse the pin low for eight reference clock cycles and release it to reset all the states to their default values. There is also an equivalent function in MDIO register bit 0.15. The reset function of the whole chip is set by logically OR'ed the inverse of RSTN and the bit 0.15.

operating frequency range

The TLK3104SCGNT is optimized for operation at a serial data rate of 3.125 Gbit/s. The TLK3104SCGNT can operate at a serial data rate between 3 Gbps to 3.125 Gbps. External clocks must be within ±100 PPM of the desired parallel data rate clock.

IDDEN function

When held low, the ENABLE pin disables all quiescent power in both the analog and digital circuitry. This allows for I_{DDQ} testing on all power supplies and can also be used to conserve power when the link is inactive.

loopback testing

The TLK3104SCGNT can provide a self-test function by enabling the internal loop-back path with the assertion of LPENx for each channel. Enabling this pin causes the serial transmitted data to be routed internally to the receiver for that channel. The parallel data output can be compared to the parallel input data for that channel to provide functional verification. The external serial output is held in a high-impedance state during the loop-back testing.

JTAG

The TLK3104SCGNT has a JTAG test control interface to allow for boundary scan. However, due to the sensitivity of the high-speed serial pins, TXxP/N and RXxP/N are not scanned under JTAG.

power-on reset

Upon application of minimum valid power, the TLK3104SCGNT generates a power-on reset. During the power-on reset the receive data pins RDx[0..3] are 3-state and the recovered receive clock pins RCx are held low. The length of the power-on reset cycle is dependent upon the reference clock (RFCP/RFCN) frequency, but is less than 1 ms in duration.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD}, V_{DDQ}, V_{DDA} (see Note 1) . . . . . −0.3 V to 3 V
Input voltage, V_I, (TTL) . . . . . −0.3 V to 4 V
Voltage range at any terminal . . . . . −0.3 V to V_{DD} + 0.3 V
Storage temperature, T_{stg} . . . . . −65°C to 150°C
Electrostatic discharge . . . . . Class 3, A:2 kV
Ambient temperature range, T_A, (see Note 2) . . . . . −40°C to 75°C
Junction temperature, T_J . . . . . 125°C Max

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. PCB conditions is defined in JEDEC JESD51-7.

DISSIPATION RATING TABLE‡

AIR FLOW	0 m/s	1 m/s	2 m/s
θ JA(C/W)	21.6	17.8	16.7
Psi jt(C/W)	9.84		

‡ PCB conditions are defined in JEDEC JESD51-7

recommended operating conditions

power supply and power consumption

			MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}, V_{DDA}, V_{DDIO}			2.3	2.5	2.7	V
Power dissipation, P_D	Transceiver mode	3.125 Gbps, PRBS pattern		2.7	3.2	W
	Transmit only mode			2.1	2.6	
	Receive only mode			2.2	2.6	
	Repeater mode			1.9	2.3	
Shutdown current, I_{DA}, V_{DDA}		Enable = 0, V_{DDA} pins, V_{DDA} = max		165		µA
Shutdown current I_{DD}, V_{DD}		Enable = 0, V_{DD} pins, V_{DD} = max		9		mA

reference clock timing requirements over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	NOM	MAX	UNIT
Frequency, R_ω		620	622.08	625	MHz
Accuracy		−100		100	ppm
Duty cycle		40%	50%	60%	
Jitter	Random			40	ps

NOTE 3: This clock should be crystal referenced to meet the requirements of the above table.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

reference clock input signals: RFCP/N

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage		825		1675	mV
$V_{(idth)}$	Input differential threshold voltage	See Figure 18	100			mV
C_i	Input capacitance				3	pF
R_{IN}	Input differential impedance		80	100	120	Ω

LVDS input signals: TD[0:3]x, TDKx, TCx

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage		825		1675	mV
$V_{(idth)}$	Input differential threshold voltage	See Figure 18	100			mV
r_i	Differential input impedance		80	100	120	Ω
C_i	Input capacitance				3	pF
t_{su}	Input setup time requirement	Reference to raising edge of the clock, see Figure 2	800			ps
t_h	Input hold time requirement		0			ps
$t_{(duty)}$	Input clock duty cycle	Nominal: 622.08 MHz	40%		60%	

TTL input signals

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2		3.6	V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input current	V_{DD} = MAX, V_{IN} = 2 V			40	µA
I_{IL}	Low-level input current	V_{DD} = MAX, V_{IN} = 0.4 V			−600	µA
C_i	Input capacitance				4	pF

LVDS output signals: RD[0:3]x, RDKx, RCx

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OD}	Output differential voltage	R_L = 100 ±1%, see Figure 17	300		600	mV
V_{OC}	Output common mode output voltage	R_L = 100 ±1%, see Figure 17	1125		1375	mV
ΔV_{OD}	Change in V_{OD} between 1 and 0	R_L = 100 ±1%			25	mV
ΔV_{OC}	Change in V_{OC} between 1 and 0	R_L = 100 ±1%			25	mV
	Output short circuit current	Outputs shorted to ground or shorted together			12	mA
I_O	Power off current	V_{DD} = 0 V			10	µA
t_d	Output delay time	Reference to rising edge of RCx, see Figure 7	130		320	ps
t_r, t_f	Output transition time	20%−80%, see Figure 17	100		300	ps
	Skew				50	ps
	Output clock duty cycle	622.08 MHz	40%		60%	
	Output clock period variations	622.08 MHz	−100		100	ps

TTL input signals

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 µA, V_{DD} = MIN	2	2.3		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, V_{DD} = MIN	0	0.25	0.6	V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

serial transmitter/receiver characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(p)}$ = |TXP − TXN|, transmit differential output voltage under preemphasis		PRE1 = 1, PRE2 = 1, R_t = 50 Ω, see Figure 19	730	870	1020	mV
		PRE1 = 0, PRE2 = 1	770	910	1060	
		PRE1 =0, PRE2 = 0	790	940	1100	
		PRE1 = 1, PRE2 = 0	850	1020	1200	
$V_{OD(d)}$ = |TXP − TXN|, transmit differential output voltage under preemphasis		PRE1 = 1, PRE2 = 1	550	650	820	mV
		PRE1 = 0, PRE2 = 1	590	690	920	
		PRE1 = 0, PRE2 = 0	620	730	980	
		PRE1 = 1, PRE2 = 0	700	820	1060	
$V_{(cmt)}$	Transmit common mode voltage range	R_t = 50 Ω	1000	1250	1400	mV
	Receive input differential voltage requirement, V_{ID} = |RXP − RXN|		150		1600	mV
$V_{(cmr)}$	Receiver common mode voltage range		1050	1500	2150	mV
I_{lkg}	Receiver input leakage		−550		550	µA
R_N	Receiver differential impedance		80	100	120	Ω
C_i	Receiver input capacitance				1	pF

serial differential switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_t	Differential signal transition time (20% to 80%)	R_L = 50 Ω, C_L = 5 pF		120		ps
	Serial data output total jitter (p−p)	Differential output jitter, PRBS at 3.125 Gbps		77		ps
	Serial data output jitter (RMS)	Differential output jitter, 101010... at 3.125 Gbps		4.77		ps

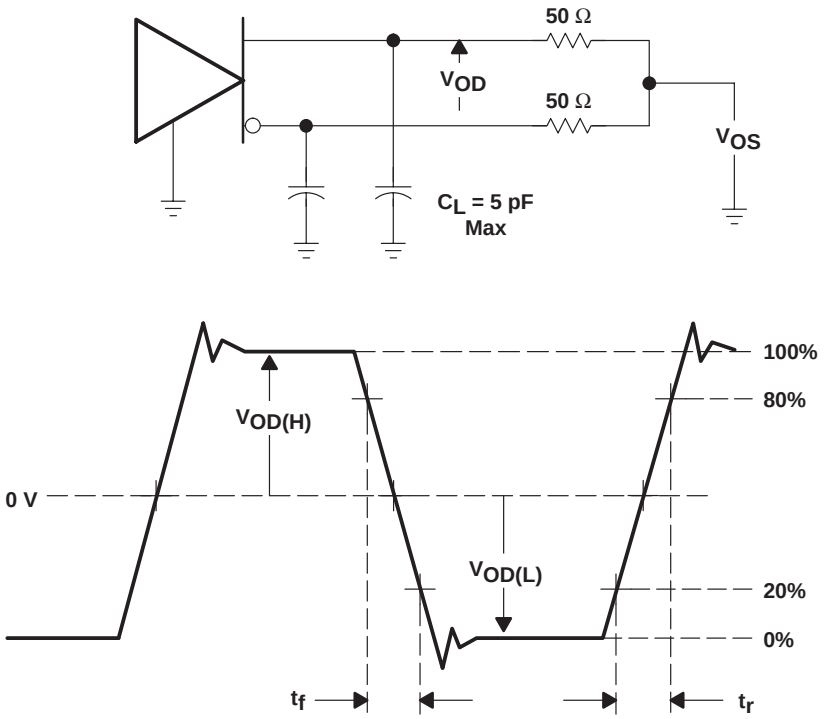


Figure 17. Test Load and Voltage Definitions for LVDS Outputs

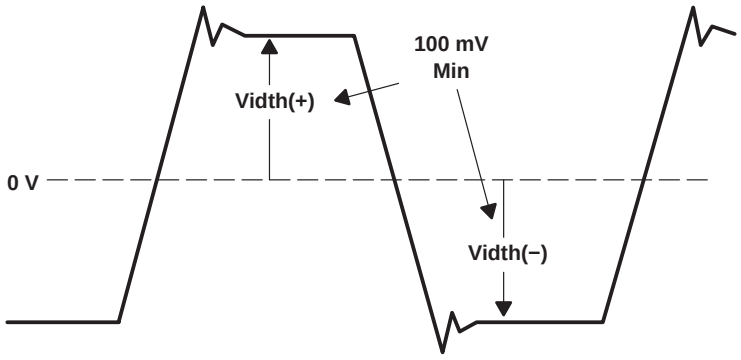


Figure 18. LVDS Input and Reference Clock Input (RFCP/N) Threshold Voltage Definition

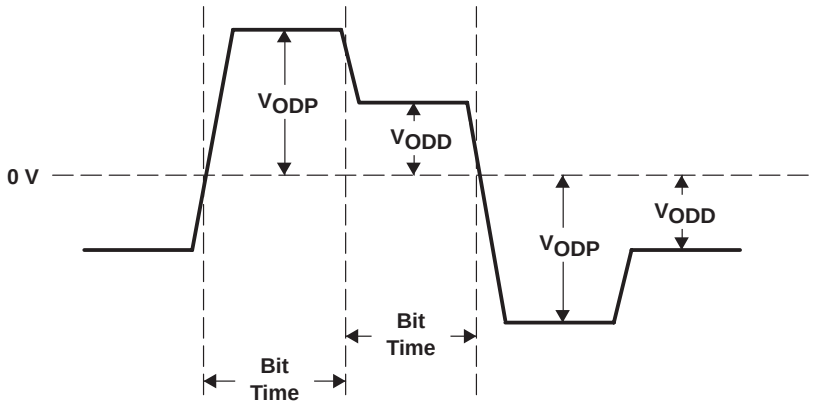


Figure 19. Output Differential Voltage Under Preemphasis

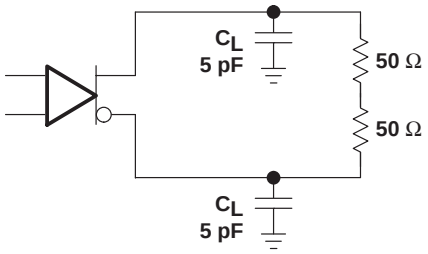


Figure 20. Transmitter Test Setup

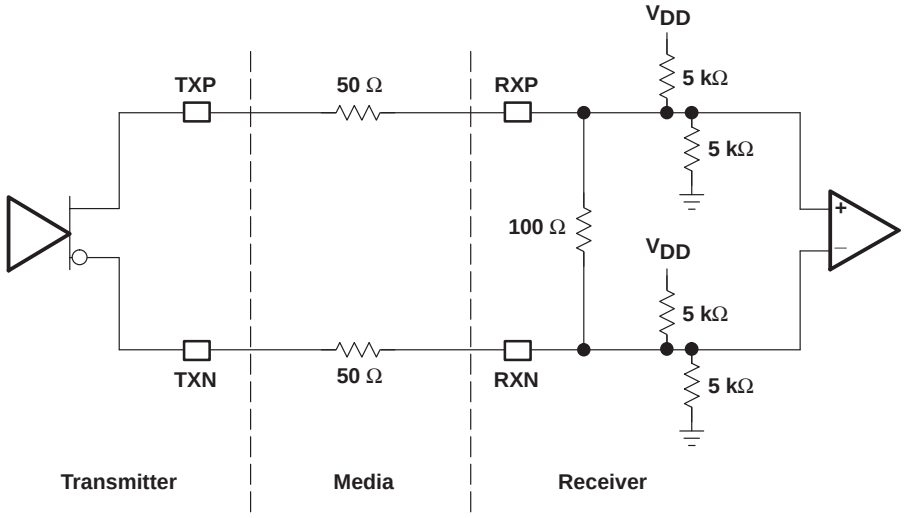


Figure 21. High-Speed I/O Directly Coupled Mode

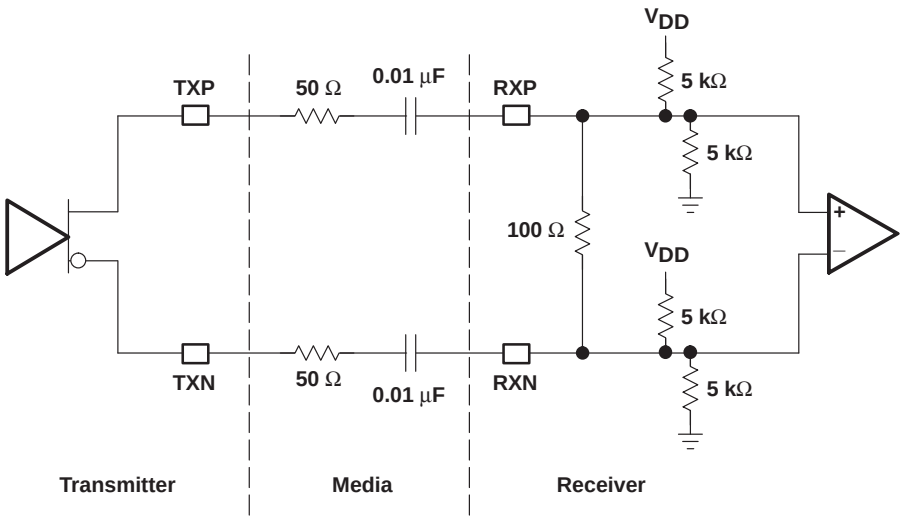


Figure 22. High-Speed I/O AC-Coupled Mode

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