

MC33102

Sleep-Mode™ Two-State, Micropower Operational Amplifier

The MC33102 dual operational amplifier is an innovative design concept employing Sleep-Mode technology. Sleep-Mode amplifiers have two separate states, a sleepmode and an awakemode. In sleepmode, the amplifier is active and waiting for an input signal. When a signal is applied causing the amplifier to source or sink 160 μ A (typically) to the load, it will automatically switch to the awakemode which offers higher slew rate, gain bandwidth, and drive capability.

- Two States: “Sleepmode” (Micropower) and “Awakemode” (High Performance)
- Switches from Sleepmode to Awakemode in 4.0 μ s when Output Current Exceeds the Threshold Current ($R_L = 600 \Omega$)
- Independent Sleepmode Function for Each Op Amp
- Standard Pinouts – No Additional Pins or Components Required
- Sleepmode State – Can Be Used in the Low Current Idle State as a Fully Functional Micropower Amplifier
- Automatic Return to Sleepmode when Output Current Drops Below Threshold
- No Deadband/Crossover Distortion; as Low as 1.0 Hz in the Awakemode
- Drop-in Replacement for Many Other Dual Op Amps
- ESD Clamps on Inputs Increase Reliability without Affecting Device Operation

TYPICAL SLEEPMODE/AWAKEMODE PERFORMANCE

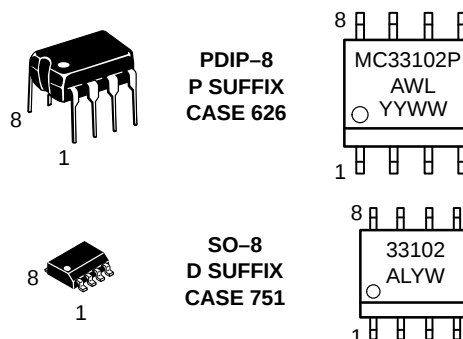
Characteristic	Sleepmode (Typical)	Awakemode (Typical)	Unit
Low Current Drain	45	750	μ A
Low Input Offset Voltage	0.15	0.15	mV
High Output Current Capability	0.15	50	mA
Low T.C. of Input Offset Voltage	1.0	1.0	μ V/ $^{\circ}$ C
High Gain Bandwidth (@ 20 kHz)	0.33	4.6	MHz
High Slew Rate	0.16	1.7	V/ μ s
Low Noise (@ 1.0 kHz)	28	9.0	nV/ $\sqrt{\text{Hz}}$



ON Semiconductor

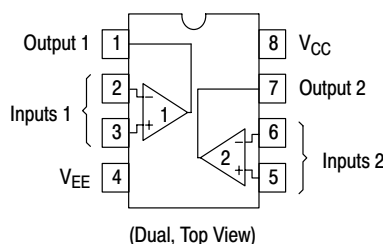
<http://onsemi.com>

MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS

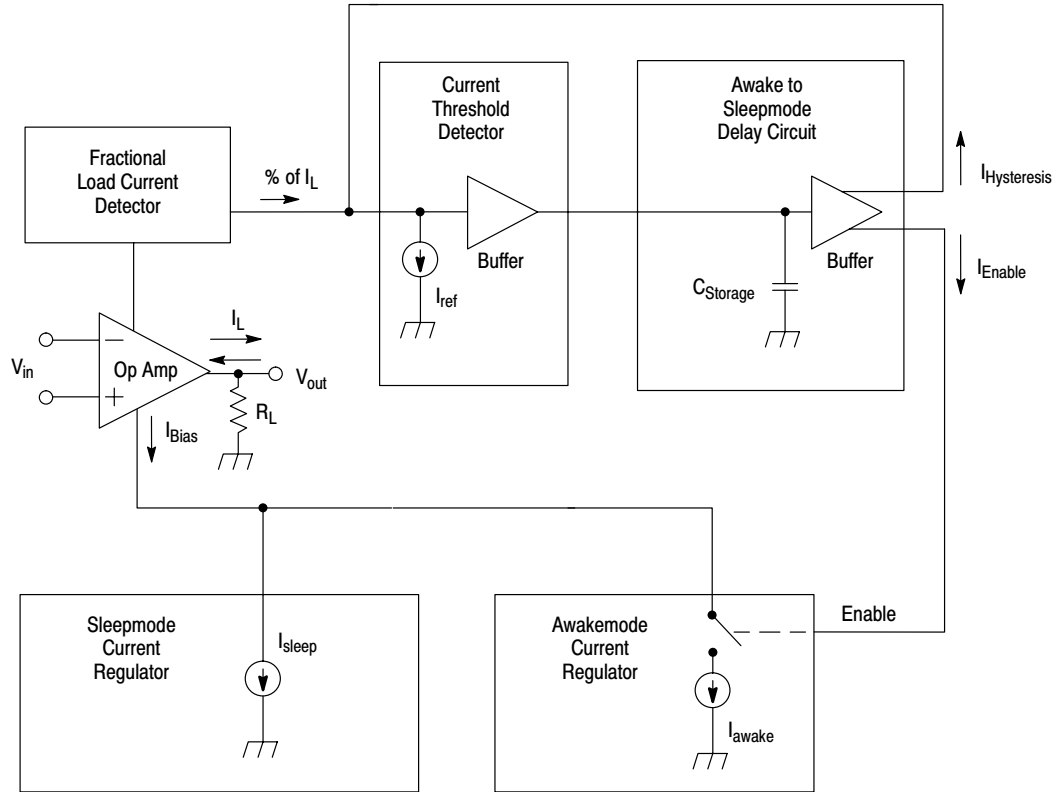


ORDERING INFORMATION

Device	Package	Shipping
MC33102D	SO-8	98 Units/Rail
MC33102DR2	SO-8	2500 Tape & Reel
MC33102P	PDIP-8	50 Units/Rail

MC33102

Simplified Block Diagram



MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range Input Voltage Range	V_{IDR} V_{IR}	Note 1.	V
Output Short Circuit Duration (Note 2.)	t_{SC}	Note 2.	sec
Maximum Junction Temperature Storage Temperature	T_J T_{stg}	+150 -65 to +150	°C
Maximum Power Dissipation	P_D	Note 2.	mW

1. Either or both input voltages should not exceed V_{CC} or V_{EE} .
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (refer to Figure 1).

MC33102

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 50\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) Sleepmode $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$ Awakemode $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$	2	$ V_{IO} $	– –	0.15 –	2.0 3.0	mV
Input Offset Voltage Temperature Coefficient ($R_S = 50\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = -40^\circ\text{ to }+85^\circ\text{C}$ (Sleepmode and Awakemode)	3	$\Delta V_{IO}/\Delta T$	–	1.0	–	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) Sleepmode $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$ Awakemode $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$	4, 6	I_{IB}	– –	8.0 –	50 60	nA
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) Sleepmode $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$ Awakemode $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$	–	$ I_{IO} $	– –	0.5 –	5.0 6.0	nA
Common Mode Input Voltage Range ($\Delta V_{IO} = 5.0\text{ mV}$, $V_O = 0\text{ V}$) Sleepmode and Awakemode	5	V_{ICR}	–13 –	–14.8 +14.2	– +13	V
Large Signal Voltage Gain Sleepmode ($R_L = 1.0\text{ M}\Omega$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$ Awakemode ($V_O = \pm 10\text{ V}$, $R_L = 600\ \Omega$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$	7	A_{VOL}	25 15 50 25	200 – 700 –	– – – –	kV/V
Output Voltage Swing ($V_{ID} = \pm 1.0\text{ V}$) Sleepmode ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$) $R_L = 1.0\text{ M}\Omega$ $R_L = 1.0\text{ M}\Omega$ Awakemode ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$) $R_L = 600\ \Omega$ $R_L = 600\ \Omega$ $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$ Awakemode ($V_{CC} = +2.5\text{ V}$, $V_{EE} = -2.5\text{ V}$) $R_L = 600\ \Omega$ $R_L = 600\ \Omega$	8, 9, 10	V_{O+} V_{O-} V_{O+} V_{O-} V_{O+} V_{O-} V_{O+} V_{O-}	+13.5 – +12.5 – +13.3 – +1.1 –	+14.2 –14.2 +13.6 –13.6 +14 –14 +1.6 –1.6	– –13.5 – –12.5 – –13.3 – –1.1	V V
Common Mode Rejection ($V_{CM} = \pm 13\text{ V}$) Sleepmode and Awakemode	11	CMR	80	90	–	dB
Power Supply Rejection ($V_{CC}/V_{EE} = +15\text{ V}/-15\text{ V}$, $5.0\text{ V}/-15\text{ V}$, $+15\text{ V}/-5.0\text{ V}$) Sleepmode and Awakemode	12	PSR	80	100	–	dB

MC33102

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Output Transition Current Sleepmode to Awakemode (Source/Sink) ($V_S = \pm 15\text{ V}$) ($V_S = \pm 2.5\text{ V}$) Awakemode to Sleepmode (Source/Sink) ($V_S = \pm 15\text{ V}$) ($V_S = \pm 2.5\text{ V}$)	13, 14	$ I_{TH1} $ $ I_{TH2} $	200 250 – –	160 200 142 180	– – 90 140	μA
Output Short Circuit Current (Awakemode) ($V_{ID} = \pm 1.0\text{ V}$, Output to Ground) Source Sink	15, 16	$ I_{SC} $	50 50	110 110	– –	mA
Power Supply Current (per Amplifier) ($A_{CL} = 1$, $V_O = 0\text{V}$) Sleepmode ($V_S = \pm 15\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$ Sleepmode ($V_S = \pm 2.5\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$ Awakemode ($V_S = \pm 15\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	17	I_D	– – – – – –	45 48 38 42 750 800	65 70 65 – 800 900	μA

MC33102

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V _{in} = -5.0 V to +5.0 V, C _L = 50 pF, A _V = 1.0) Sleepmode (R _L = 1.0 MΩ) Awakemode (R _L = 600 Ω)	18	SR	0.10 1.0	0.16 1.7	— —	V/μs
Gain Bandwidth Product Sleepmode (f = 10 kHz) Awakemode (f = 20 kHz)	19	GBW	0.25 3.5	0.33 4.6	— —	MHz
Sleepmode to Awakemode Transition Time (A _{CL} = 0.1, V _{in} = 0 V to +5.0 V) R _L = 600 Ω R _L = 10 kΩ	20, 21	t _{tr1}	— —	4.0 15	— —	μs
Awakemode to Sleepmode Transition Time	22	t _{tr2}	—	1.5	—	sec
Unity Gain Frequency (Open Loop) Sleepmode (R _L = 100 kΩ, C _L = 0 pF) Awakemode (R _L = 600 Ω, C _L = 0 pF)		f _U	— —	200 2500	— —	kHz
Gain Margin Sleepmode (R _L = 100 kΩ, C _L = 0 pF) Awakemode (R _L = 600 Ω, C _L = 0 pF)	23, 25	A _M	— —	13 12	— —	dB
Phase Margin Sleepmode (R _L = 100 kΩ, C _L = 0 pF) Awakemode (R _L = 600 Ω, C _L = 0 pF)	24, 26	∅ _M	— —	60 60	— —	Degree s
Channel Separation (f = 100 Hz to 20 kHz) Sleepmode and Awakemode	29	CS	—	120	—	dB
Power Bandwidth (Awakemode) (V _O = 10 V _{pp} , R _L = 100 kΩ, THD ≤ 1%)		BW _P	—	20	—	kHz
Total Harmonic Distortion (V _O = 2.0 V _{pp} , A _V = 1.0) Awakemode (R _L = 600 Ω) f = 1.0 kHz f = 10 kHz f = 20 kHz	30	THD	— — —	0.005 0.016 0.031	— — —	%
DC Output Impedance (V _O = 0 V, A _V = 10, I _Q = 10 μA) Sleepmode Awakemode	31	R _O	— —	1.0 k 96	— —	Ω
Differential Input Resistance (V _{CM} = 0 V) Sleepmode Awakemode		R _{in}	— —	1.3 0.17	— —	MΩ
Differential Input Capacitance (V _{CM} = 0 V) Sleepmode Awakemode		C _{in}	— —	0.4 4.0	— —	pF
Equivalent Input Noise Voltage (f = 1.0 kHz, R _S = 100 Ω) Sleepmode Awakemode	32	e _n	— —	28 9.0	— —	nV/√Hz
Equivalent Input Noise Current (f = 1.0 kHz) Sleepmode Awakemode	33	i _n	— —	0.01 0.05	— —	pA/√Hz

MC33102

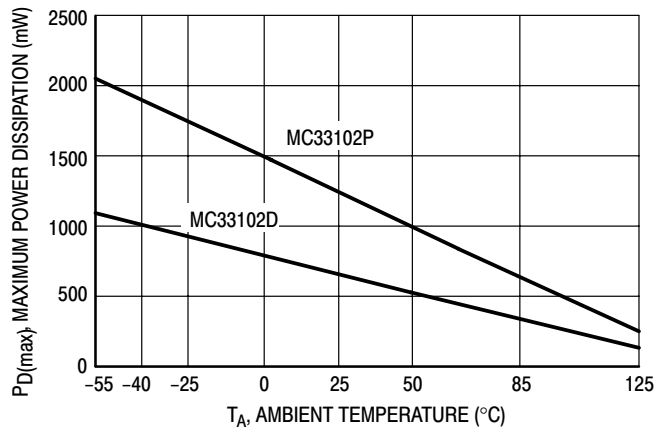


Figure 1. Maximum Power Dissipation versus Temperature

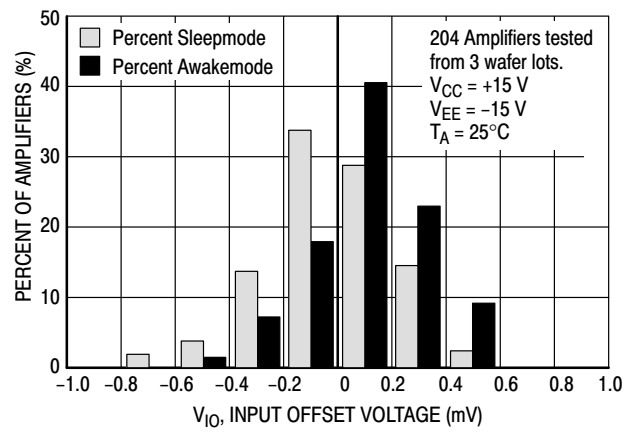


Figure 2. Distribution of Input Offset Voltage (MC33102D Package)

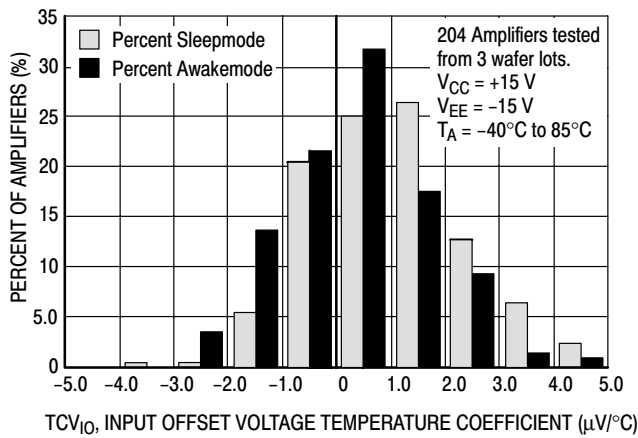


Figure 3. Input Offset Voltage Temperature Coefficient Distribution (MC33102D Package)

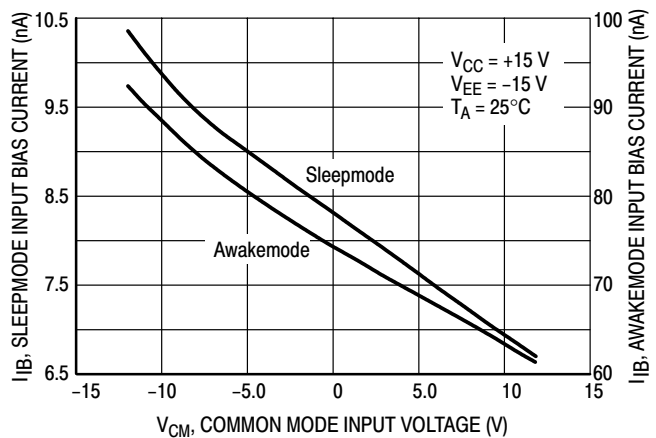


Figure 4. Input Bias Current versus Common Mode Input Voltage

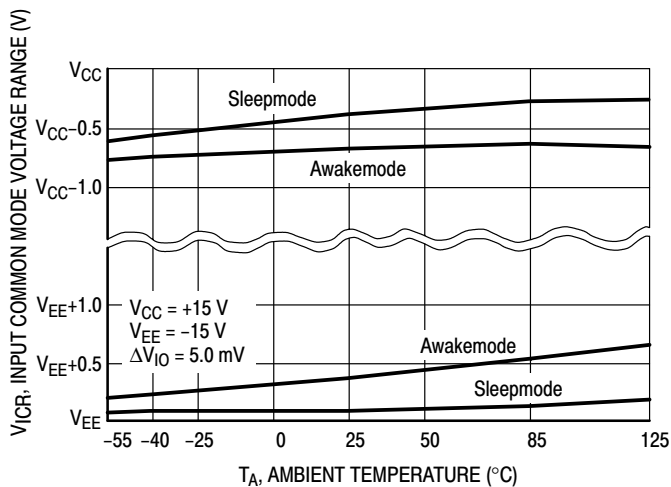


Figure 5. Input Common Mode Voltage Range versus Temperature

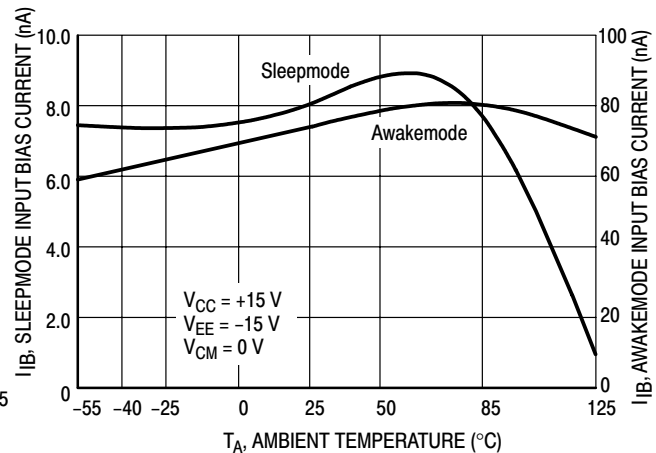


Figure 6. Input Bias Current versus Temperature

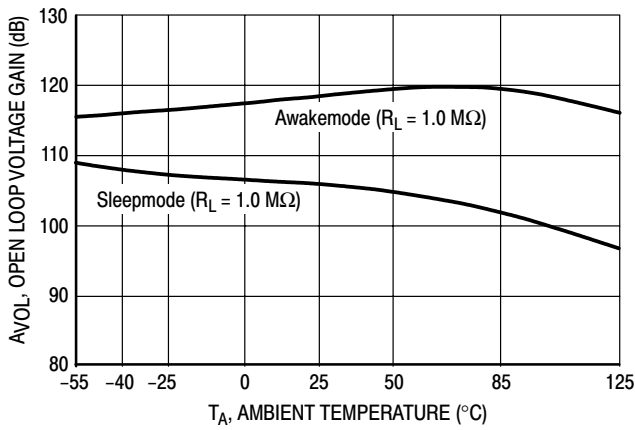


Figure 7. Open Loop Voltage Gain versus Temperature

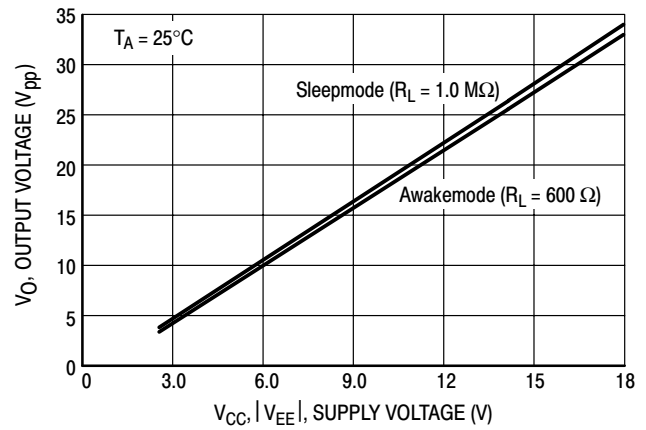


Figure 8. Output Voltage Swing versus Supply Voltage

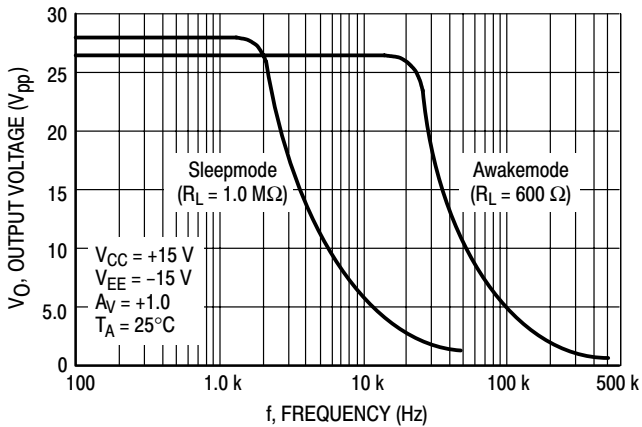


Figure 9. Output Voltage versus Frequency

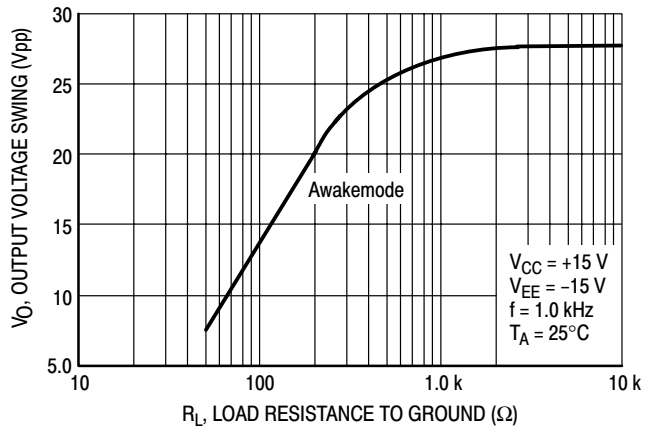


Figure 10. Maximum Peak-to-Peak Output Voltage Swing versus Load Resistance

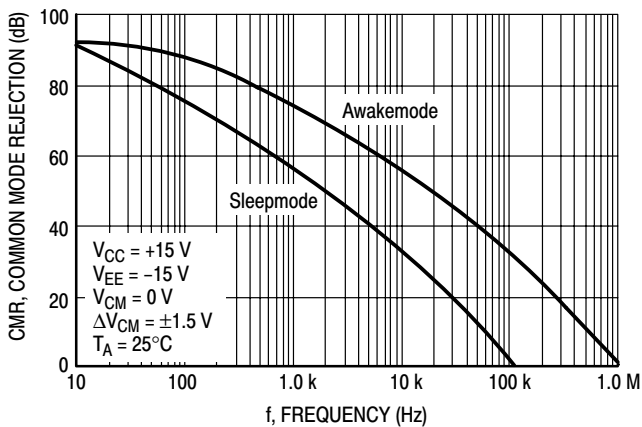


Figure 11. Common Mode Rejection versus Frequency

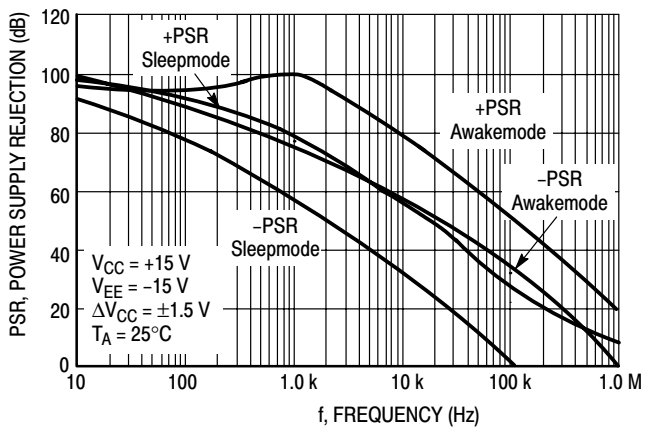


Figure 12. Power Supply Rejection versus Frequency

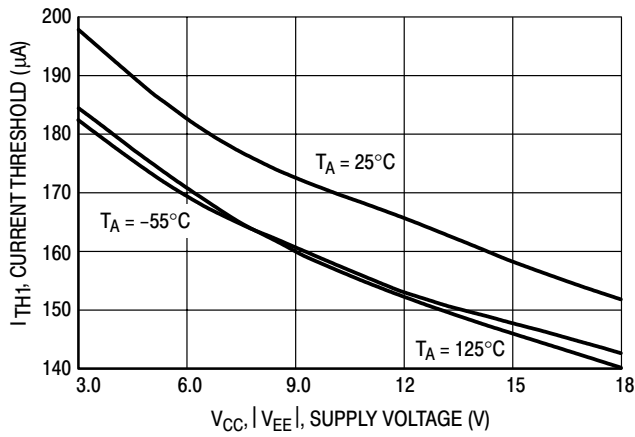


Figure 13. Sleepmode to Awakemode Current Threshold versus Supply Voltage

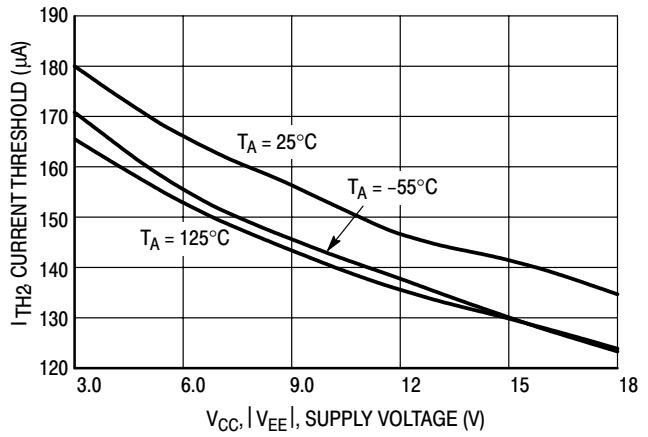


Figure 14. Awakemode to Sleepmode Current Threshold versus Supply Voltage

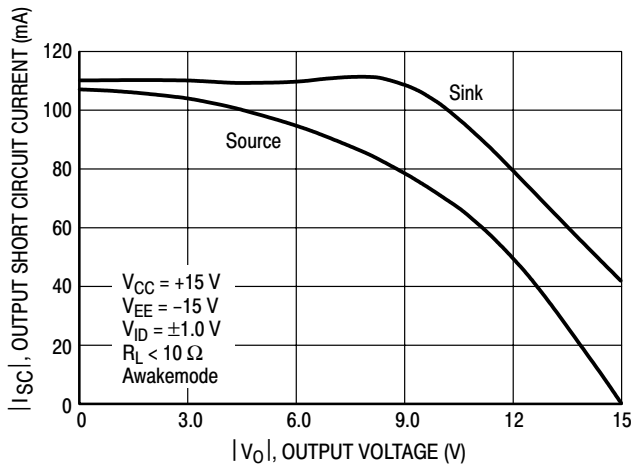


Figure 15. Output Short Circuit Current versus Output Voltage

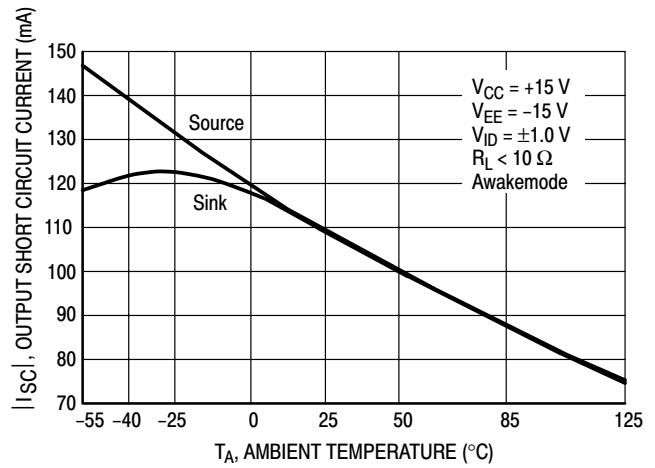


Figure 16. Output Short Circuit Current versus Temperature

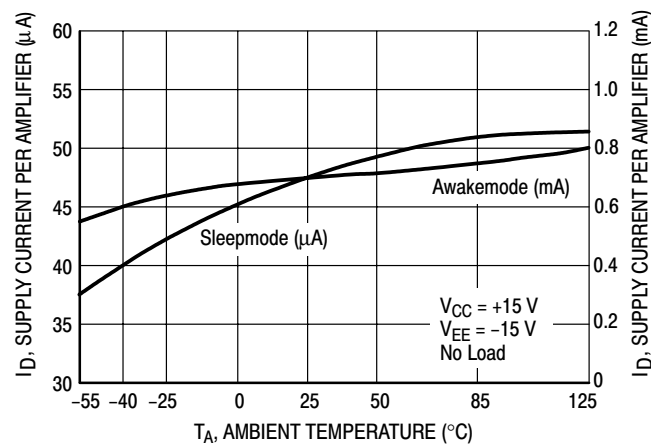


Figure 17. Power Supply Current Per Amplifier versus Temperature

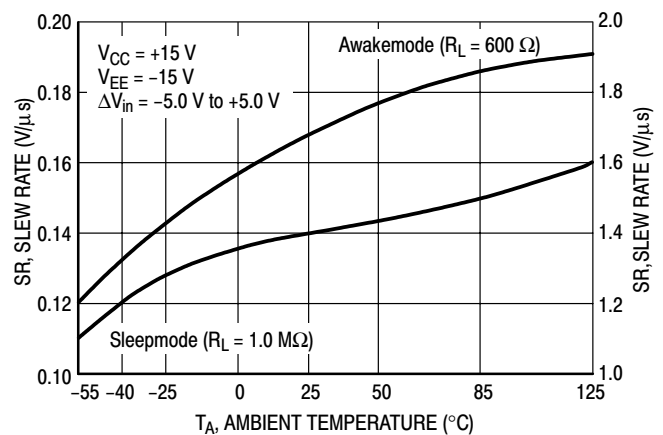


Figure 18. Slew Rate versus Temperature

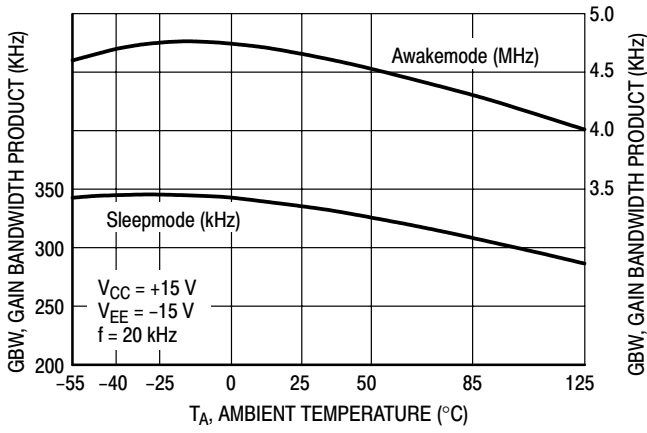


Figure 19. Gain Bandwidth Product versus Temperature

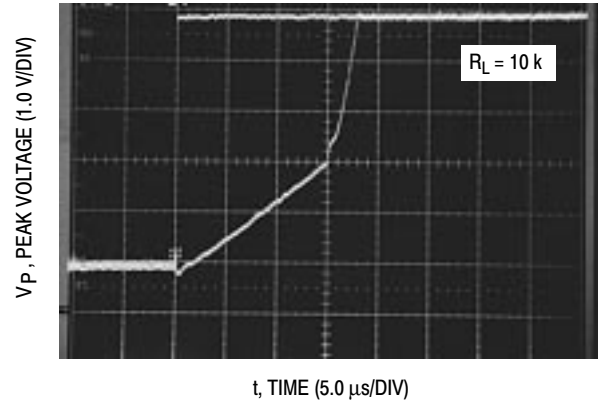


Figure 20. Sleepmode to Awakemode Transition Time

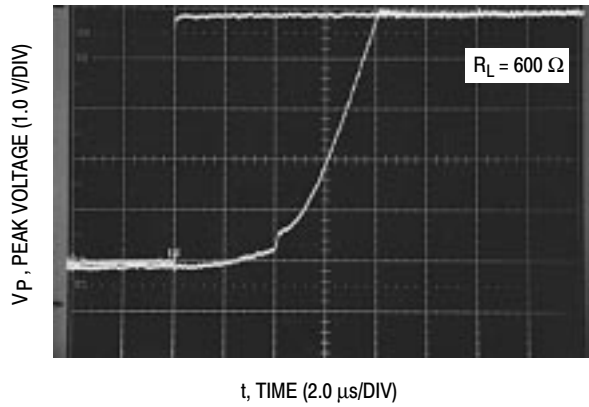


Figure 21. Sleepmode to Awakemode Transition Time

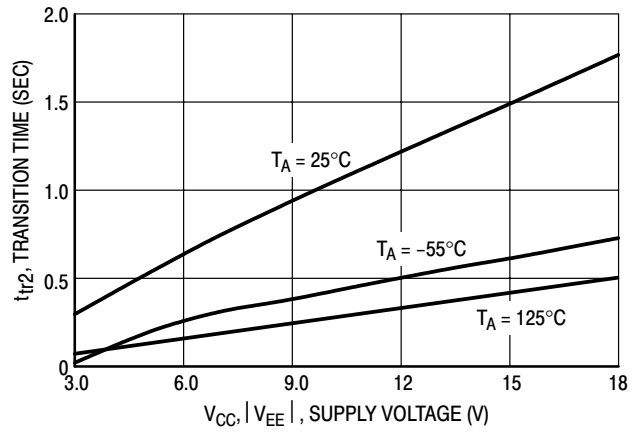


Figure 22. Awakemode to Sleepmode Transition Time versus Supply Voltage

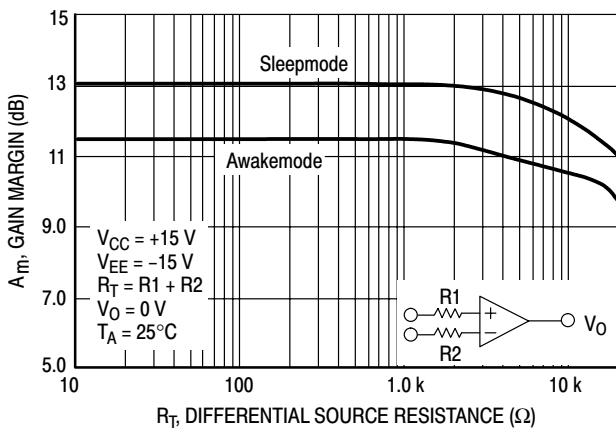


Figure 23. Gain Margin versus Differential Source Resistance

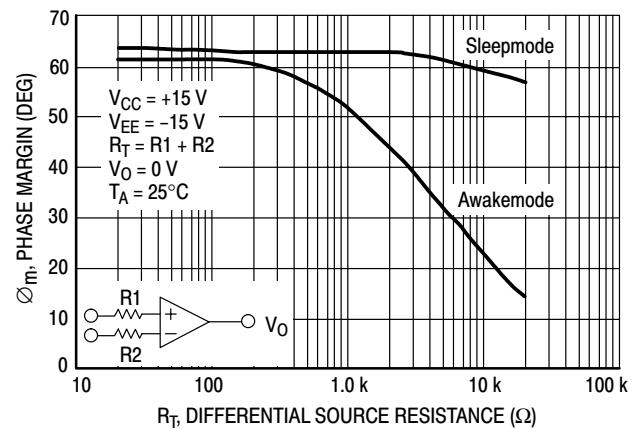


Figure 24. Phase Margin versus Differential Source Resistance

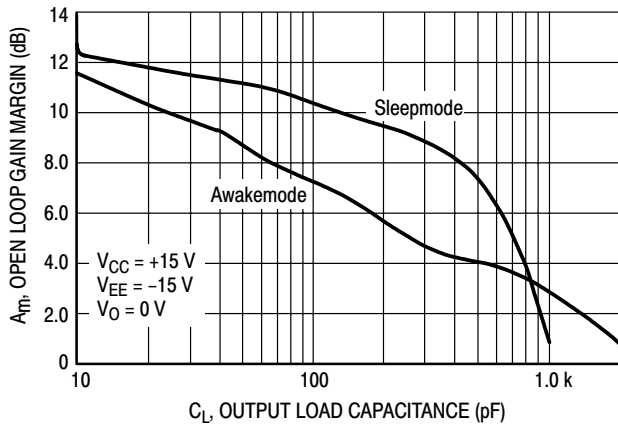


Figure 25. Open Loop Gain Margin versus Output Load Capacitance

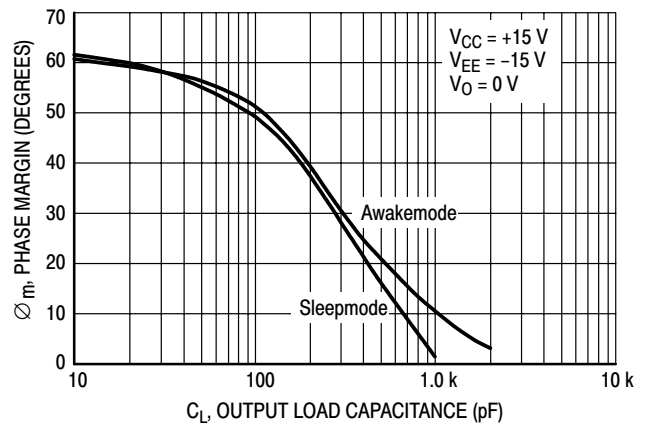


Figure 26. Phase Margin versus Output Load Capacitance

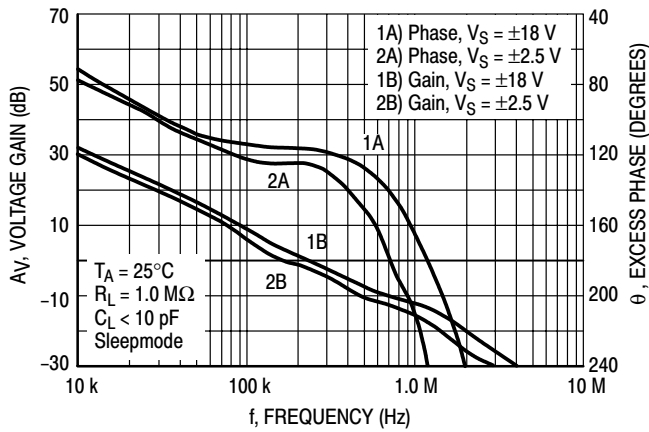


Figure 27. Sleepmode Voltage Gain and Phase versus Frequency

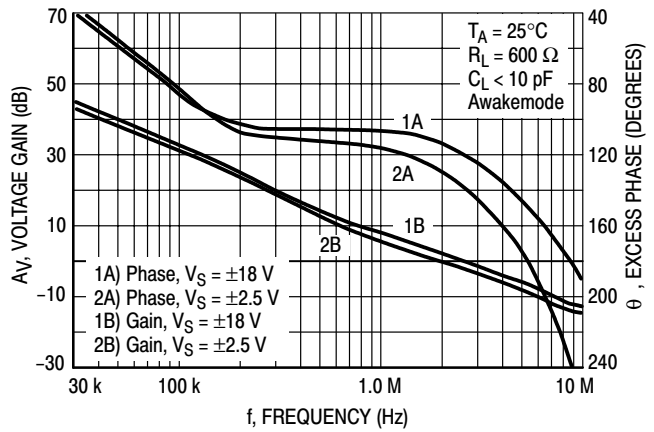


Figure 28. Awakemode Voltage Gain and Phase versus Frequency

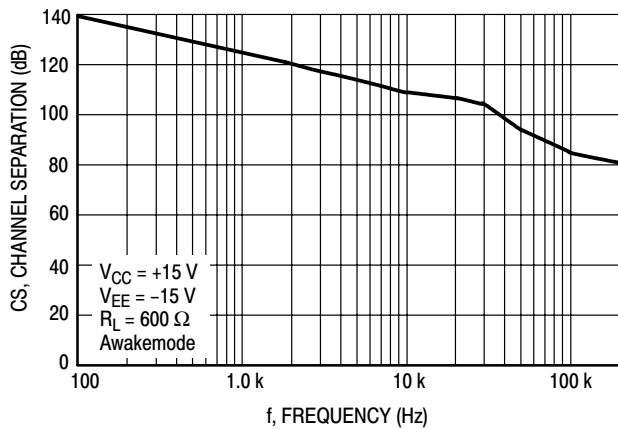


Figure 29. Channel Separation versus Frequency

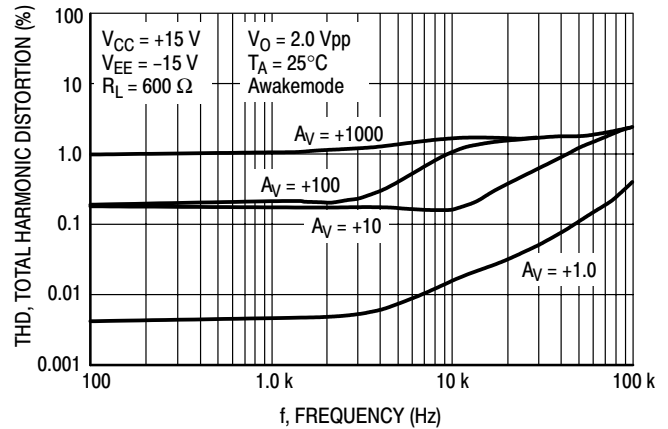


Figure 30. Total Harmonic Distortion versus Frequency

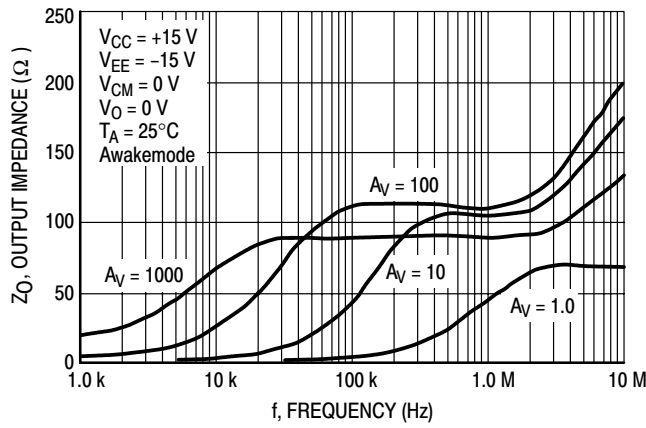


Figure 31. Awakemode Output Impedance versus Frequency

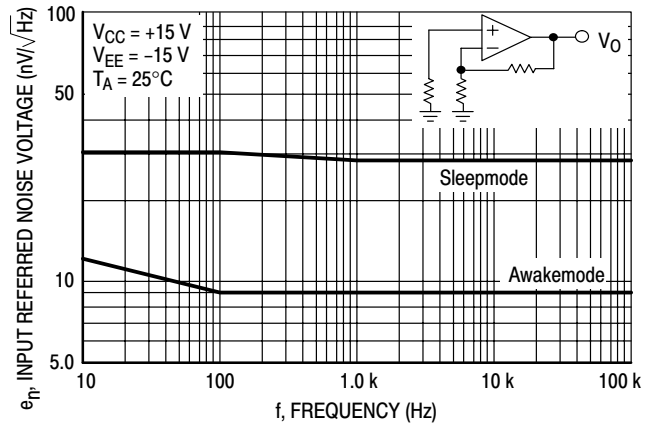


Figure 32. Input Referred Noise Voltage versus Frequency

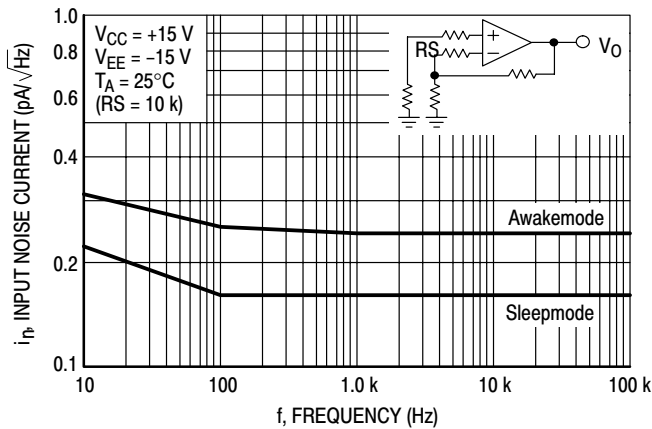


Figure 33. Current Noise versus Frequency

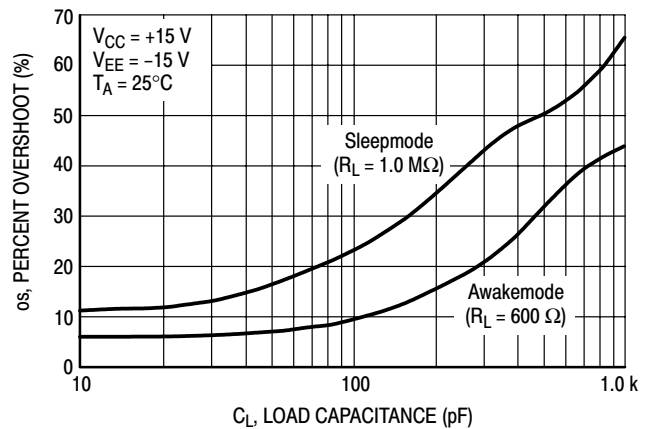


Figure 34. Percent Overshoot versus Load Capacitance

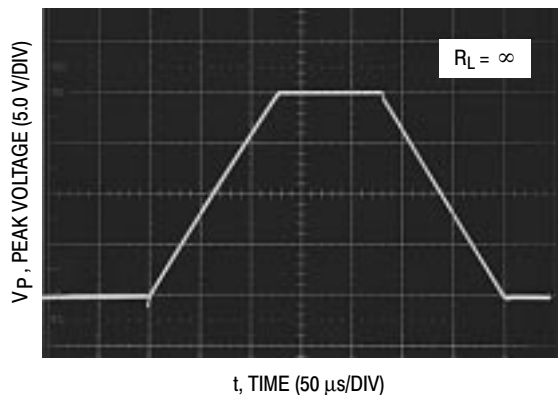


Figure 35. Sleepmode Large Signal Transient Response

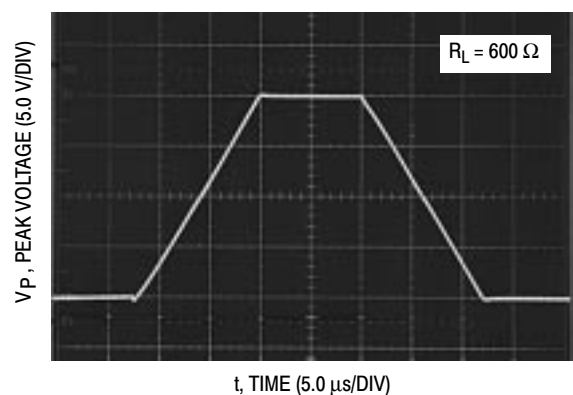


Figure 36. Awakemode Large Signal Transient Response

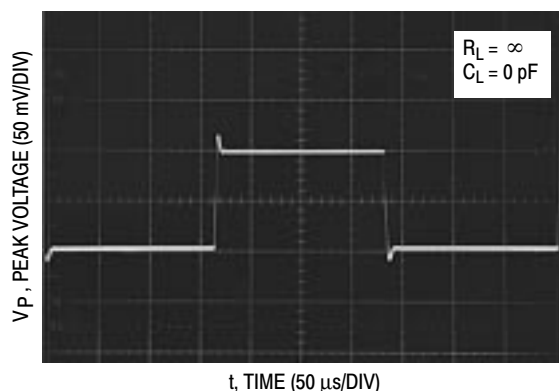


Figure 37. Sleepmode Small Signal Transient Response

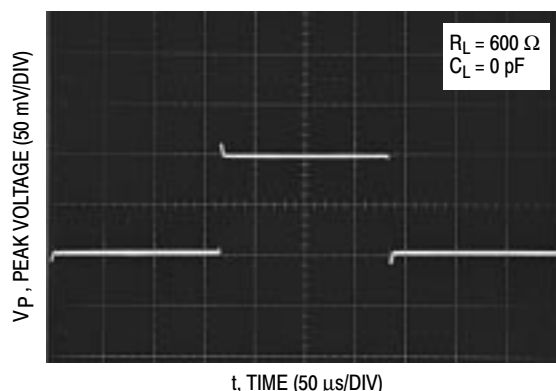


Figure 38. Awakemode Small Signal Transient Response

CIRCUIT INFORMATION

The MC33102 was designed primarily for applications where high performance (which requires higher current drain) is required only part of the time. The two-state feature of this op amp enables it to conserve power during idle times, yet be powered up and ready for an input signal. Possible applications include laptop computers, automotive, cordless phones, baby monitors, and battery operated test equipment. Although most applications will require low power consumption, this device can be used in any application where better efficiency and higher performance is needed.

The Sleep-Mode™ amplifier has two states; a sleepmode and an awakemode. In the sleepmode state, the amplifier is active and functions as a typical micropower op amp. When a signal is applied to the amplifier causing it to source or sink sufficient current (see Figure 13), the amplifier will automatically switch to the awakemode. See Figures 20 and 21 for transition times with 600 Ω and 10 kΩ loads.

The awakemode uses higher drain current to provide a high slew rate, gain bandwidth, and output current capability. In the awakemode, this amplifier can drive 27 Vpp into a 600 Ω load with $V_S = \pm 15$ V.

An internal delay circuit is used to prevent the amplifier from returning to the sleepmode at every zero crossing. This delay circuit also eliminates the crossover distortion commonly found in micropower amplifiers. This amplifier can process frequencies as low as 1.0 Hz without the amplifier returning to sleepmode, depending on the load.

The first stage PNP differential amplifier provides low noise performance in both the sleep and awake modes, and an all NPN output stage provides symmetrical source and sink AC frequency response.

APPLICATIONS INFORMATION

The MC33102 will begin to function at power supply voltages as low as $V_S = \pm 1.0$ V at room temperature. (At this voltage, the output voltage swing will be limited to a few hundred millivolts.) The input voltages must range between V_{CC} and V_{EE} supply voltages as shown in the maximum rating table. Specifically, **allowing the input to go more negative than 0.3 V below V_{EE} may cause product damage.** Also, exceeding the input common mode voltage range on either input may cause phase reversal, even if the inputs are between V_{CC} and V_{EE} .

When power is initially applied, the part may start to operate in the awakemode. This is because of the currents generated due to charging of internal capacitors. When this occurs and the sleepmode state is desired, the user will have to wait approximately 1.5 seconds before the device will switch back to the sleepmode. To prevent this from occurring, ramp the power supplies from 1.0 V to full supply. Notice that the device is more prone to switch into the awakemode when V_{EE} is adjusted than with a similar change in V_{CC} .

The amplifier is designed to switch from sleepmode to awakemode whenever the output current exceeds a preset current threshold (I_{TH}) of approximately 160 μA. As a result, the output switching threshold voltage (V_{ST}) is controlled by the output loading resistance (R_L). This loading can be a load resistor, feedback resistors, or both. Then:

$$V_{ST} = (160 \mu A) \times R_L$$

Large valued load resistors require a large output voltage to switch, but reduce unwanted transitions to the awakemode. For instance, in cases where the amplifier is connected with a large closed loop gain (A_{CL}), the input offset voltage (V_{IO}) is multiplied by the gain at the output and could produce an output voltage exceeding V_{ST} with no input signal applied.

Small values of R_L allow rapid transition to the awakemode because most of the transition time is consumed slewing in the sleepmode until V_{ST} is reached (see Figures 20, 21). The output switching threshold voltage V_{ST} is higher for larger values of R_L , requiring the amplifier to slew longer in the slower sleepmode state before switching to the awakemode.

The transition time (t_{tr1}) required to switch from sleep to awake mode is:

$$t_{tr1} = t_D = I_{TH}(R_L/SR_{sleepmode})$$

Where:

t_D = Amplifier delay ($< 1.0 \mu s$)

I_{TH} = Output threshold current for more transition
($160 \mu A$)

R_L = Load resistance

$SR_{sleepmode}$ = Sleepmode slew rate ($0.16 V/\mu s$)

Although typically $160 \mu A$, I_{TH} varies with supply voltage and temperature. In general, any current loading on the output which causes a current greater than I_{TH} to flow will switch the amplifier into the awakemode. This includes transition currents such as those generated by charging load capacitances. In fact, the maximum capacitance that can be driven while attempting to remain in the sleepmode is approximately $1000 pF$.

$$\begin{aligned} C_{L(max)} &= I_{TH}/SR_{sleepmode} \\ &= 160 \mu A / (0.16 V/\mu s) \\ &= 1000 pF \end{aligned}$$

Any electrical noise seen at the output of the MC33102 may also cause the device to transition to the awakemode. To

minimize this problem, a resistor may be added in series with the output of the device (inserted as close to the device as possible) to isolate the op amp from both parasitic and load capacitance.

The awakemode to sleepmode transition time is controlled by an internal delay circuit, which is necessary to prevent the amplifier from going to sleep during every zero crossing. This time is a function of supply voltage and temperature as shown in Figure 22.

Gain bandwidth product (GBW) in both modes is an important system design consideration when using a sleepmode amplifier. The amplifier has been designed to obtain the maximum GBW in both modes. "Smooth" AC transitions between modes with no noticeable change in the amplitude of the output voltage waveform will occur as long as the closed loop gains (A_{CL}) in both modes are substantially equal to the frequency of operation. For smooth AC transitions:

$$(A_{CLsleepmode})(BW) < GBW_{sleepmode}$$

Where:

$A_{CLsleepmode}$ = Closed loop gain in the sleepmode

BW = The required system bandwidth or operating frequency

TESTING INFORMATION

To determine if the MC33102 is in the awakemode or the sleepmode, the power supply currents (I_{D+} and I_{D-}) must be measured. When the magnitude of **either** power supply current exceeds $400 \mu A$, the device is in the awakemode. When the magnitudes of both supply currents are less than $400 \mu A$, the device is in the sleepmode. Since the total supply current is typically ten times higher in the awakemode than the sleepmode, the two states are easily distinguishable.

The measured value of I_{D+} equals the I_D of both devices (for a dual op amp) plus the output source current of device A and the output source current of device B. Similarly, the measured value of I_{D-} is equal to the I_{D-} of both devices plus

the output sink current of each device. I_{out} is the sum of the currents caused by both the feedback loop and load resistance. The total I_{out} needs to be subtracted from the measured I_D to obtain the correct I_D of the dual op amp.

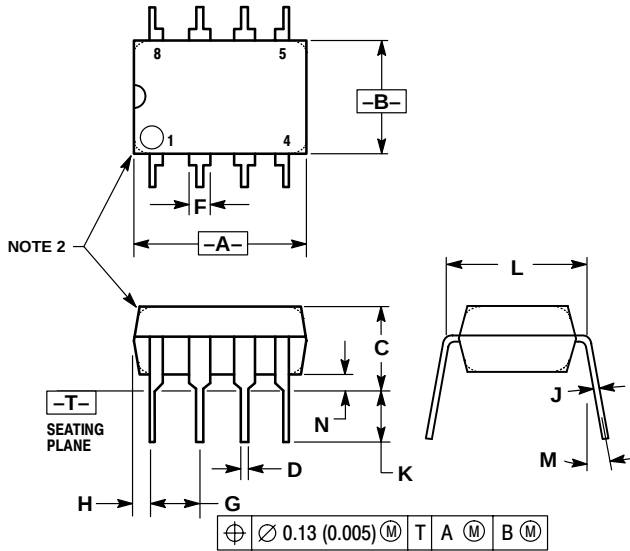
An accurate way to measure the awakemode I_{out} current on automatic test equipment is to remove the I_{out} current on both Channel A and B. Then measure the I_D values before the device goes back to the sleepmode state. The transition will take typically 1.5 seconds with $\pm 15 V$ power supplies.

The large signal sleepmode testing in the characterization was accomplished with a $1.0 M\Omega$ load resistor which ensured the device would remain in sleepmode despite large voltage swings.

MC33102

PACKAGE DIMENSIONS

PDIP-8
P SUFFIX
CASE 626-05
ISSUE K

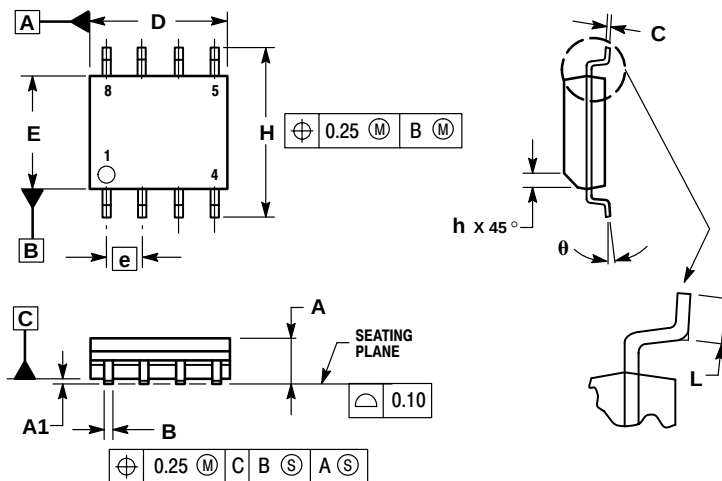


NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

SO-8
D SUFFIX
CASE 751-06
ISSUE T



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

Notes

SLEEPMODE is a trademark of Semiconductor Components Industries, LLC.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)
Email: ONlit-german@hibbertco.com

French Phone: (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)
Email: ONlit-french@hibbertco.com

English Phone: (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, England, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)
Email: ONlit-spanish@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2745

Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.