

# DATA SHEET

## **74LVC1G79**

Single D-type flip-flop;  
positive-edge trigger

Product specification  
Supersedes data of 2003 Jan 30

2003 May 16

## Single D-type flip-flop; positive-edge trigger

## 74LVC1G79

## FEATURES

- Wide supply voltage range from 1.65 to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 to 1.95 V)
  - JESD8-5 (2.3 to 2.7 V)
  - JESD8B/JESD36 (2.7 to 3.6 V).
- $\pm 24$  mA output drive ( $V_{CC} = 3.0$  V)
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from  $-40$  to  $+85$  °C and  $-40$  to  $+125$  °C.

## DESCRIPTION

The 74LVC1G79 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. This feature allows the use of this device in a mixed 3.3 and 5 V environment.

This device is fully specified for partial Power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC1G79 provides a single positive-edge triggered D-type flip-flop.

Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D input must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

| SYMBOL            | PARAMETER                                | CONDITIONS  | TYPICAL | UNIT |
|-------------------|--|---|---------|------|
| $t_{PHL}/t_{PLH}$ | propagation delay CP to Q                | $V_{CC} = 1.8$ V; $C_L = 30$ pF; $R_L = 1$ k $\Omega$ | 3.6     | ns   |
|                   |  | $V_{CC} = 2.5$ V; $C_L = 30$ pF; $R_L = 500$ $\Omega$ | 2.3     | ns   |
|                   |  | $V_{CC} = 2.7$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$ | 2.6     | ns   |
|                   |  | $V_{CC} = 3.3$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$ | 2.2     | ns   |
|                   |  | $V_{CC} = 5.0$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$ | 1.7     | ns   |
| $C_I$             | input capacitance                        |   | 5       | pF   |
| $C_{PD}$          | power dissipation capacitance per buffer | $V_{CC} = 3.3$ V; notes 1 and 2                       | 17      | pF   |

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in volts;

$N$  = total switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND to } V_{CC}$ .

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## FUNCTION TABLE

See note 1.

| INPUT |   | OUTPUT |
|-------|---|--------|
| CP    | D | Q      |
| ↑     | L | L      |
| ↑     | H | H      |
| L     | X | q      |

## Note

1. H = HIGH voltage level;

L = LOW voltage level;

↑ = LOW-to-HIGH CP transition;

X = don't care;

q = lower case letter indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CP transition.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE           |      |         |          |        |         |
|-------------|-------------------|------|---------|----------|--------|---------|
|             | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE   | MARKING |
| 74LVC1G79GW | −40 to +125 °C    | 5    | SC-88A  | plastic  | SOT353 | VP      |
| 74LVC1G79GV | −40 to +125 °C    | 5    | SC-74A  | plastic  | SOT753 | V79     |

## PINNING

| PIN | SYMBOL          | DESCRIPTION          |
|-----|-----------------|----------------------|
| 1   | D               | data input D         |
| 2   | CP              | clock pulse input CP |
| 3   | GND             | ground (0 V)         |
| 4   | Q               | data output Q        |
| 5   | V <sub>CC</sub> | supply voltage       |

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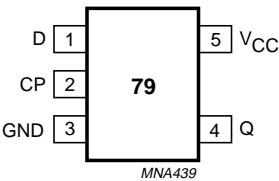


Fig.1 Pin configuration.

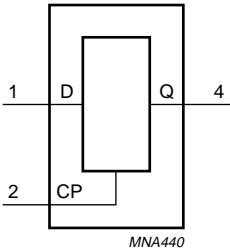


Fig.2 Logic symbol.

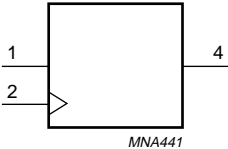


Fig.3 IEE/IEC logic symbol.

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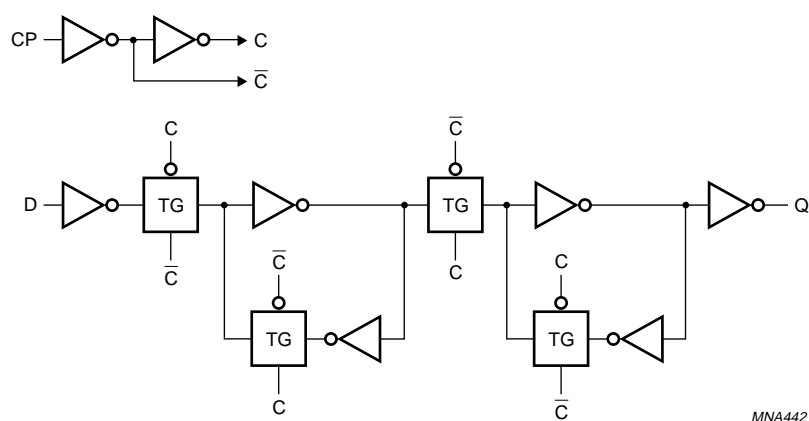


Fig.4 Logic diagram.

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## RECOMMENDED OPERATING CONDITIONS

| SYMBOL     | PARAMETER                     | CONDITIONS                      | MIN. | MAX.     | UNIT |
|------------|-------------------------------|---------------------------------|------|----------|------|
| $V_{CC}$   | supply voltage                |                                 | 1.65 | 5.5      | V    |
| $V_I$      | input voltage                 |                                 | 0    | 5.5      | V    |
| $V_O$      | output voltage                | active mode                     | 0    | $V_{CC}$ | V    |
|            |                               | $V_{CC} = 0$ V; Power-down mode | 0    | 5.5      | V    |
| $T_{amb}$  | operating ambient temperature |                                 | -40  | +125     | °C   |
| $t_r, t_f$ | input rise and fall times     | $V_{CC} = 1.65$ to $2.7$ V      | 0    | 20       | ns/V |
|            |                               | $V_{CC} = 2.7$ to $5.5$ V       | 0    | 10       | ns/V |

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

| SYMBOL            | PARAMETER                     | CONDITIONS                   | MIN. | MAX. | UNIT |
|-------------------|-------------------------------|------------------------------|------|------|------|
| $V_{CC}$          | supply voltage                |                              | -0.5 | +6.5 | V    |
| $I_{IK}$          | input diode current           | $V_I < 0$                    | -    | -50  | mA   |
| $V_I$             | input voltage                 | note 1                       | -0.5 | +6.5 | V    |
| $I_{OK}$          | output diode current          | $V_O > V_{CC}$ or $V_O < 0$  | -    | ±50  | mA   |
| $V_O$             | output voltage                | active mode; note 1          | -0.5 | +6.5 | V    |
|                   |                               | Power-down mode; note 1      | -0.5 | +6.5 | V    |
| $I_O$             | output source or sink current | $V_O = 0$ to $V_{CC}$        | -    | ±50  | mA   |
| $I_{CC}, I_{GND}$ | $V_{CC}$ or GND current       |                              | -    | ±100 | mA   |
| $T_{stg}$         | storage temperature           |                              | -65  | +150 | °C   |
| $P_D$             | power dissipation             | $T_{amb} = -40$ to $+125$ °C | -    | 250  | mW   |

## Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL                           | PARAMETER   | TEST CONDITIONS   |                     | MIN.                   | TYP. <sup>(1)</sup> | MAX.                   | UNIT |
|----------------------------------|---|---|---------------------|------------------------|---------------------|------------------------|------|
|                                  |   | OTHER   | V <sub>CC</sub> (V) |                        |                     |                        |      |
| T <sub>amb</sub> = −40 to +85 °C |   |   |                     |                        |                     |                        |      |
| V <sub>IH</sub>                  | HIGH-level input voltage                          |   | 1.65 to 1.95        | 0.65 × V <sub>CC</sub> | –                   | –                      | V    |
|                                  |   |   | 2.3 to 2.7          | 1.7                    | –                   | –                      | V    |
|                                  |   |   | 2.7 to 3.6          | 2.0                    | –                   | –                      | V    |
|                                  |   |   | 4.5 to 5.5          | 0.7 × V <sub>CC</sub>  | –                   | –                      | V    |
| V <sub>IL</sub>                  | LOW-level input voltage                           |   | 1.65 to 1.95        | –                      | –                   | 0.35 × V <sub>CC</sub> | V    |
|                                  |   |   | 2.3 to 2.7          | –                      | –                   | 0.7                    | V    |
|                                  |   |   | 2.7 to 3.6          | –                      | –                   | 0.8                    | V    |
|                                  |   |   | 4.5 to 5.5          | –                      | –                   | 0.3 × V <sub>CC</sub>  | V    |
| V <sub>OL</sub>                  | LOW-level output voltage                          | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>             |                     |                        |                     |                        |      |
|                                  |   | I <sub>O</sub> = 100 μA   | 1.65 to 5.5         | –                      | –                   | 0.1                    | V    |
|                                  |   | I <sub>O</sub> = 4 mA   | 1.65                | –                      | –                   | 0.45                   | V    |
|                                  |   | I <sub>O</sub> = 8 mA   | 2.3                 | –                      | –                   | 0.3                    | V    |
|                                  |   | I <sub>O</sub> = 12 mA  | 2.7                 | –                      | –                   | 0.4                    | V    |
|                                  |   | I <sub>O</sub> = 24 mA  | 3.0                 | –                      | –                   | 0.55                   | V    |
| V <sub>OH</sub>                  | HIGH-level output voltage                         | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>             |                     |                        |                     |                        |      |
|                                  |   | I <sub>O</sub> = −100 μA  | 1.65 to 5.5         | V <sub>CC</sub> − 0.1  | –                   | –                      | V    |
|                                  |   | I <sub>O</sub> = −4 mA  | 1.65                | 1.2                    | –                   | –                      | V    |
|                                  |   | I <sub>O</sub> = −8 mA  | 2.3                 | 1.9                    | –                   | –                      | V    |
|                                  |   | I <sub>O</sub> = −12 mA   | 2.7                 | 2.2                    | –                   | –                      | V    |
|                                  |   | I <sub>O</sub> = −24 mA   | 3.0                 | 2.3                    | –                   | –                      | V    |
| I <sub>LI</sub>                  | input leakage current                             | V <sub>I</sub> = 5.5 V or GND                                   | 5.5                 | –                      | ±0.1                | ±5                     | μA   |
|                                  |   |   |                     |                        |                     |                        |      |
| I <sub>off</sub>                 | power OFF leakage current                         | V <sub>I</sub> or V <sub>O</sub> = 5.5 V                        | 0                   | –                      | ±0.1                | ±10                    | μA   |
| I <sub>CC</sub>                  | quiescent supply current                          | V <sub>I</sub> = V <sub>CC</sub> or GND;<br>I <sub>O</sub> = 0  | 5.5                 | –                      | 0.1                 | 10                     | μA   |
| ΔI <sub>CC</sub>                 | additional quiescent supply current per input pin | V <sub>I</sub> = V <sub>CC</sub> − 0.6 V;<br>I <sub>O</sub> = 0 | 2.3 to 5.5          | –                      | 5                   | 500                    | μA   |

## Single D-type flip-flop; positive-edge trigger

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| SYMBOL                            | PARAMETER   | TEST CONDITIONS  |                     | MIN.                      | TYP. <sup>(1)</sup>  | MAX.                   | UNIT                  |
|-----------------------------------|---|--|---------------------|---------------------------|--|------------------------|-----------------------|
|                                   |   | OTHER  | V <sub>CC</sub> (V) |                           |  |                        |                       |
| T <sub>amb</sub> = −40 to +125 °C |   |  |                     |                           |  |                        |                       |
| V <sub>IH</sub>                   | HIGH-level input voltage                          |  | 1.65 to 1.95        | 0.65 × V <sub>CC</sub>    | —  | —                      | V                     |
|                                   |   |  | 2.3 to 2.7          | 1.7                       | —  | —                      | V                     |
|                                   |   |  | 2.7 to 3.6          | 2.0                       | —  | —                      | V                     |
|                                   |   |  | 4.5 to 5.5          | 0.7 × V <sub>CC</sub>     | —  | —                      | V                     |
| V <sub>IL</sub>                   | LOW-level input voltage                           |  | 1.65 to 1.95        | —                         | —  | 0.35 × V <sub>CC</sub> | V                     |
|                                   |   |  | 2.3 to 2.7          | —                         | —  | 0.7                    | V                     |
|                                   |   |  | 2.7 to 3.6          | —                         | —  | 0.8                    | V                     |
|                                   |   |  | 4.5 to 5.5          | —                         | —  | 0.3 × V <sub>CC</sub>  | V                     |
| V <sub>OL</sub>                   | LOW-level output voltage                          | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>O</sub> = 100 μA<br>I <sub>O</sub> = 4 mA<br>I <sub>O</sub> = 8 mA<br>I <sub>O</sub> = 12 mA<br>I <sub>O</sub> = 24 mA<br>I <sub>O</sub> = 32 mA | 1.65 to 5.5         | —                         | —  | 0.1                    | V                     |
|                                   |   |  | 1.65                | —                         | —  | 0.70                   | V                     |
|                                   |   |  | 2.3                 | —                         | —  | 0.45                   | V                     |
|                                   |   |  | 2.7                 | —                         | —  | 0.60                   | V                     |
|                                   |   |  | 3.0                 | —                         | —  | 0.80                   | V                     |
|                                   |   |  | 4.5                 | —                         | —  | 0.80                   | V                     |
|                                   |   |  | V <sub>OH</sub>     | HIGH-level output voltage | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>O</sub> = −100 μA<br>I <sub>O</sub> = −4 mA<br>I <sub>O</sub> = −8 mA<br>I <sub>O</sub> = −12 mA<br>I <sub>O</sub> = −24 mA<br>I <sub>O</sub> = −32 mA | 1.65 to 5.5            | V <sub>CC</sub> − 0.1 |
| 1.65                              | 0.95  | —  |                     |                           |  | —                      | V                     |
| 2.3                               | 1.7   | —  |                     |                           |  | —                      | V                     |
| 2.7                               | 1.9   | —  |                     |                           |  | —                      | V                     |
| 3.0                               | 2.0   | —  |                     |                           |  | —                      | V                     |
| 4.5                               | 3.4   | —  |                     |                           |  | —                      | V                     |
| I <sub>LI</sub>                   | input leakage current                             | V <sub>I</sub> = 5.5 V or GND  |                     |                           |  | 5.5                    | —                     |
| I <sub>off</sub>                  | power OFF leakage current                         | V <sub>I</sub> or V <sub>O</sub> = 5.5 V   | 0                   | —                         | —  | ±200                   | μA                    |
| I <sub>CC</sub>                   | quiescent supply current                          | V <sub>I</sub> = V <sub>CC</sub> or GND;<br>I <sub>O</sub> = 0   | 5.5                 | —                         | —  | 200                    | μA                    |
| ΔI <sub>CC</sub>                  | additional quiescent supply current per input pin | V <sub>I</sub> = V <sub>CC</sub> − 0.6 V;<br>I <sub>O</sub> = 0  | 2.3 to 5.5          | —                         | —  | 5000                   | μA                    |

**Note**

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.



## Single D-type flip-flop; positive-edge trigger

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## AC CHARACTERISTICS

GND = 0 V.

| SYMBOL                                   | PARAMETER                        | TEST CONDITIONS  |                     | MIN. | TYP. | MAX. | UNIT |
|--|----------------------------------|------------------|---------------------|------|------|------|------|
|  |                                  | WAVEFORMS        | V <sub>CC</sub> (V) |      |      |      |      |
| T <sub>amb</sub> = −40 to +85 °C; note 1 |                                  |                  |                     |      |      |      |      |
| t <sub>PHL</sub> /t <sub>PLH</sub>       | propagation delay<br>CP to Q     | see Figs 5 and 7 | 1.65 to 1.95        | 1.0  | 3.6  | 9.9  | ns   |
|  |                                  |                  | 2.3 to 2.7          | 1.5  | 2.3  | 7.0  | ns   |
|  |                                  |                  | 2.7                 | 1.5  | 2.6  | 6.0  | ns   |
|  |                                  |                  | 3.0 to 3.6          | 0.5  | 2.2  | 5.0  | ns   |
|  |                                  |                  | 4.5 to 5.5          | 0.5  | 1.7  | 3.8  | ns   |
| t <sub>su</sub>                          | set-up time D to CP              | see Figs 6 and 7 | 1.65 to 1.95        | 2.5  | 1.4  | –    | ns   |
|  |                                  |                  | 2.3 to 2.7          | 1.7  | 0.9  | –    | ns   |
|  |                                  |                  | 2.7                 | 1.7  | 0.9  | –    | ns   |
|  |                                  |                  | 3.0 to 3.6          | 1.3  | 0.6  | –    | ns   |
|  |                                  |                  | 4.5 to 5.5          | 1.2  | 0.6  | –    | ns   |
| t <sub>h</sub>                           | hold time D to CP                | see Figs 6 and 7 | 1.65 to 1.95        | 0    | −0.7 | –    | ns   |
|  |                                  |                  | 2.3 to 2.7          | 0    | −0.4 | –    | ns   |
|  |                                  |                  | 2.7                 | +0.5 | −0.3 | –    | ns   |
|  |                                  |                  | 3.0 to 3.6          | +0.5 | −0.3 | –    | ns   |
|  |                                  |                  | 4.5 to 5.5          | +0.5 | −0.2 | –    | ns   |
| t <sub>w</sub>                           | clock pulse width HIGH<br>or LOW | see Figs 6 and 7 | 1.65 to 1.95        | 3.0  | 1.1  | –    | ns   |
|  |                                  |                  | 2.3 to 2.7          | 2.5  | 0.7  | –    | ns   |
|  |                                  |                  | 2.7                 | 2.5  | 0.6  | –    | ns   |
|  |                                  |                  | 3.0 to 3.6          | 2.5  | 0.6  | –    | ns   |
|  |                                  |                  | 4.5 to 5.5          | 2.0  | 0.5  | –    | ns   |
| f <sub>max</sub>                         | maximum clock pulse<br>frequency | see Figs 6 and 7 | 1.65 to 1.95        | 160  | 250  | –    | MHz  |
|  |                                  |                  | 2.3 to 2.7          | 160  | 300  | –    | MHz  |
|  |                                  |                  | 2.7                 | 160  | 350  | –    | MHz  |
|  |                                  |                  | 3.0 to 3.6          | 160  | 450  | –    | MHz  |
|  |                                  |                  | 4.5 to 5.5          | 200  | 500  | –    | MHz  |

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| SYMBOL                             | PARAMETER                        | TEST CONDITIONS  |                     | MIN. | TYP. | MAX. | UNIT |
|------------------------------------|----------------------------------|------------------|---------------------|------|------|------|------|
|                                    |                                  | WAVEFORMS        | V <sub>CC</sub> (V) |      |      |      |      |
| T <sub>amb</sub> = −40 to +125 °C  |                                  |                  |                     |      |      |      |      |
| t <sub>PHL</sub> /t <sub>PLH</sub> | propagation delay<br>CP to Q     | see Figs 5 and 7 | 1.65 to 1.95        | 1.0  | –    | 12.5 | ns   |
|                                    |                                  |                  | 2.3 to 2.7          | 0.5  | –    | 9.0  | ns   |
|                                    |                                  |                  | 2.7                 | 0.5  | –    | 8.0  | ns   |
|                                    |                                  |                  | 3.0 to 3.6          | 0.5  | –    | 6.5  | ns   |
|                                    |                                  |                  | 4.5 to 5.5          | 0.5  | –    | 5.0  | ns   |
| t <sub>su</sub>                    | set-up time D to CP              | see Figs 6 and 7 | 1.65 to 1.95        | 2.5  | –    | –    | ns   |
|                                    |                                  |                  | 2.3 to 2.7          | 1.7  | –    | –    | ns   |
|                                    |                                  |                  | 2.7                 | 1.7  | –    | –    | ns   |
|                                    |                                  |                  | 3.0 to 3.6          | 1.2  | –    | –    | ns   |
|                                    |                                  |                  | 4.5 to 5.5          | 1.2  | –    | –    | ns   |
| t <sub>h</sub>                     | hold time D to CP                | see Figs 6 and 7 | 1.65 to 1.95        | 0    | –    | –    | ns   |
|                                    |                                  |                  | 2.3 to 2.7          | 0    | –    | –    | ns   |
|                                    |                                  |                  | 2.7                 | 0.5  | –    | –    | ns   |
|                                    |                                  |                  | 3.0 to 3.6          | 0.5  | –    | –    | ns   |
|                                    |                                  |                  | 4.5 to 5.5          | 0.5  | –    | –    | ns   |
| t <sub>w</sub>                     | clock pulse width<br>HIGH or LOW | see Figs 6 and 7 | 1.65 to 1.95        | 3.0  | –    | –    | ns   |
|                                    |                                  |                  | 2.3 to 2.7          | 2.5  | –    | –    | ns   |
|                                    |                                  |                  | 2.7                 | 2.5  | –    | –    | ns   |
|                                    |                                  |                  | 3.0 to 3.6          | 2.5  | –    | –    | ns   |
|                                    |                                  |                  | 4.5 to 5.5          | 2.0  | –    | –    | ns   |
| f <sub>max</sub>                   | maximum clock pulse<br>frequency | see Figs 6 and 7 | 1.65 to 1.95        | 160  | –    | –    | MHz  |
|                                    |                                  |                  | 2.3 to 2.7          | 160  | –    | –    | MHz  |
|                                    |                                  |                  | 2.7                 | 160  | –    | –    | MHz  |
|                                    |                                  |                  | 3.0 to 3.6          | 160  | –    | –    | MHz  |
|                                    |                                  |                  | 4.5 to 5.5          | 200  | –    | –    | MHz  |

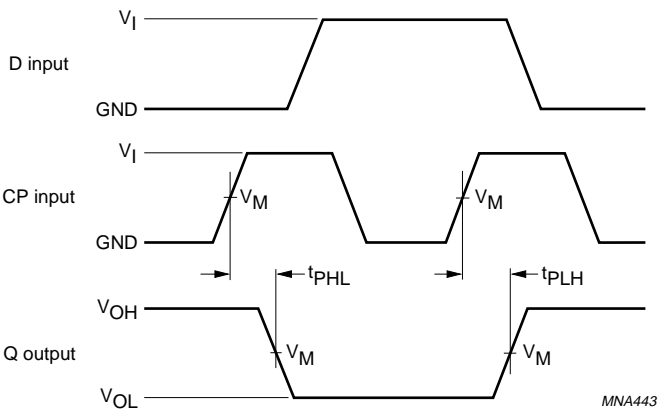
**Note**

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

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AC WAVEFORMS



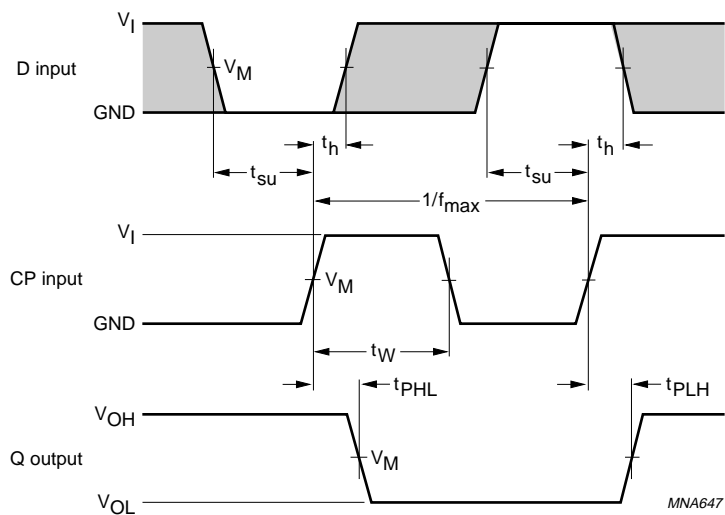
| $V_{CC}$       | $V_M$               | INPUT    |                       |
|----------------|---------------------|----------|-----------------------|
|                |                     | $V_I$    | $t_r = t_f$           |
| 1.65 to 1.95 V | $0.5 \times V_{CC}$ | $V_{CC}$ | $\leq 2.0 \text{ ns}$ |
| 2.3 to 2.7 V   | $0.5 \times V_{CC}$ | $V_{CC}$ | $\leq 2.0 \text{ ns}$ |
| 2.7 V          | 1.5 V               | 2.7 V    | $\leq 2.5 \text{ ns}$ |
| 3.0 to 3.6 V   | 1.5 V               | 2.7 V    | $\leq 2.5 \text{ ns}$ |
| 4.5 to 5.5 V   | $0.5 \times V_{CC}$ | $V_{CC}$ | $\leq 2.5 \text{ ns}$ |

$V_{OL}$  and  $V_{OH}$  are typical output voltage drop that occur with the output load.

Fig.5 Clock (CP) to output (Q) propagation delay times.

Single D-type flip-flop; positive-edge trigger

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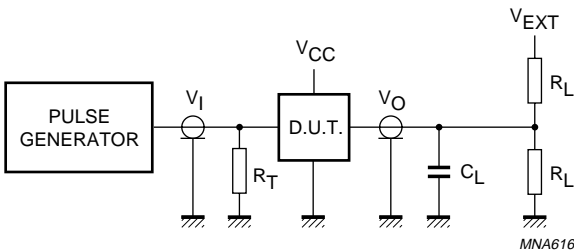
| $V_{CC}$       | $V_M$               | INPUT    |               |
|----------------|---------------------|----------|---------------|
|                |                     | $V_I$    | $t_r = t_f$   |
| 1.65 to 1.95 V | $0.5 \times V_{CC}$ | $V_{CC}$ | $\leq 2.0$ ns |
| 2.3 to 2.7 V   | $0.5 \times V_{CC}$ | $V_{CC}$ | $\leq 2.0$ ns |
| 2.7 V          | 1.5 V               | 2.7 V    | $\leq 2.5$ ns |
| 3.0 to 3.6 V   | 1.5 V               | 2.7 V    | $\leq 2.5$ ns |
| 4.5 to 5.5 V   | $0.5 \times V_{CC}$ | $V_{CC}$ | $\leq 2.5$ ns |

The shaded areas indicate when the input is permitted to change for predictable output performance.  $V_{OL}$  and  $V_{OH}$  are typical output voltage drop that occur with the output load.

Fig.6 Clock (CP) to output (Q) propagation delays, clock pulse width, D to CP set-up times, the CP to D hold times and maximum clock pulse frequency.

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| V <sub>CC</sub> | V <sub>I</sub>  | C <sub>L</sub> | R <sub>L</sub> | V <sub>EXT</sub>                   |                                    |                                    |
|-----------------|-----------------|----------------|----------------|------------------------------------|------------------------------------|------------------------------------|
|                 |                 |                |                | t <sub>PLH</sub> /t <sub>PHL</sub> | t <sub>PZH</sub> /t <sub>PHZ</sub> | t <sub>PZL</sub> /t <sub>PLZ</sub> |
| 1.65 to 1.95 V  | V <sub>CC</sub> | 30 pF          | 1 kΩ           | open                               | GND                                | 2 × V <sub>CC</sub>                |
| 2.3 to 2.7 V    | V <sub>CC</sub> | 30 pF          | 500 Ω          | open                               | GND                                | 2 × V <sub>CC</sub>                |
| 2.7 V           | 2.7 V           | 50 pF          | 500 Ω          | open                               | GND                                | 6 V                                |
| 3.0 to 3.6 V    | 2.7 V           | 50 pF          | 500 Ω          | open                               | GND                                | 6 V                                |
| 4.5 to 5.5 V    | V <sub>CC</sub> | 50 pF          | 500 Ω          | open                               | GND                                | 2 × V <sub>CC</sub>                |

Definitions for test circuit:  
R<sub>L</sub> = Load resistor.  
C<sub>L</sub> = Load capacitance including jig and probe capacitance.  
R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.7 Load circuitry for switching times.

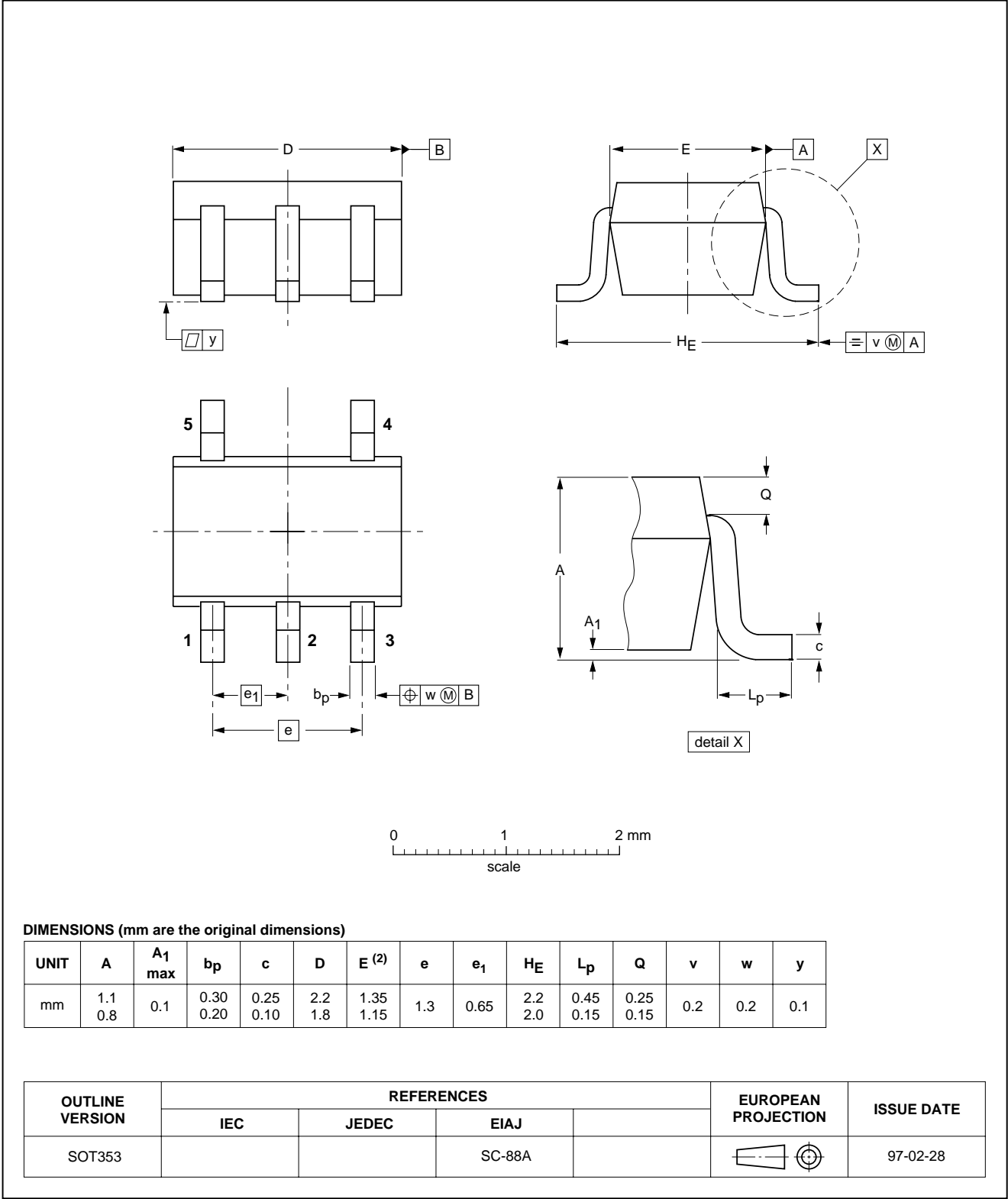
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PACKAGE OUTLINES

Plastic surface mounted package; 5 leads

SOT353

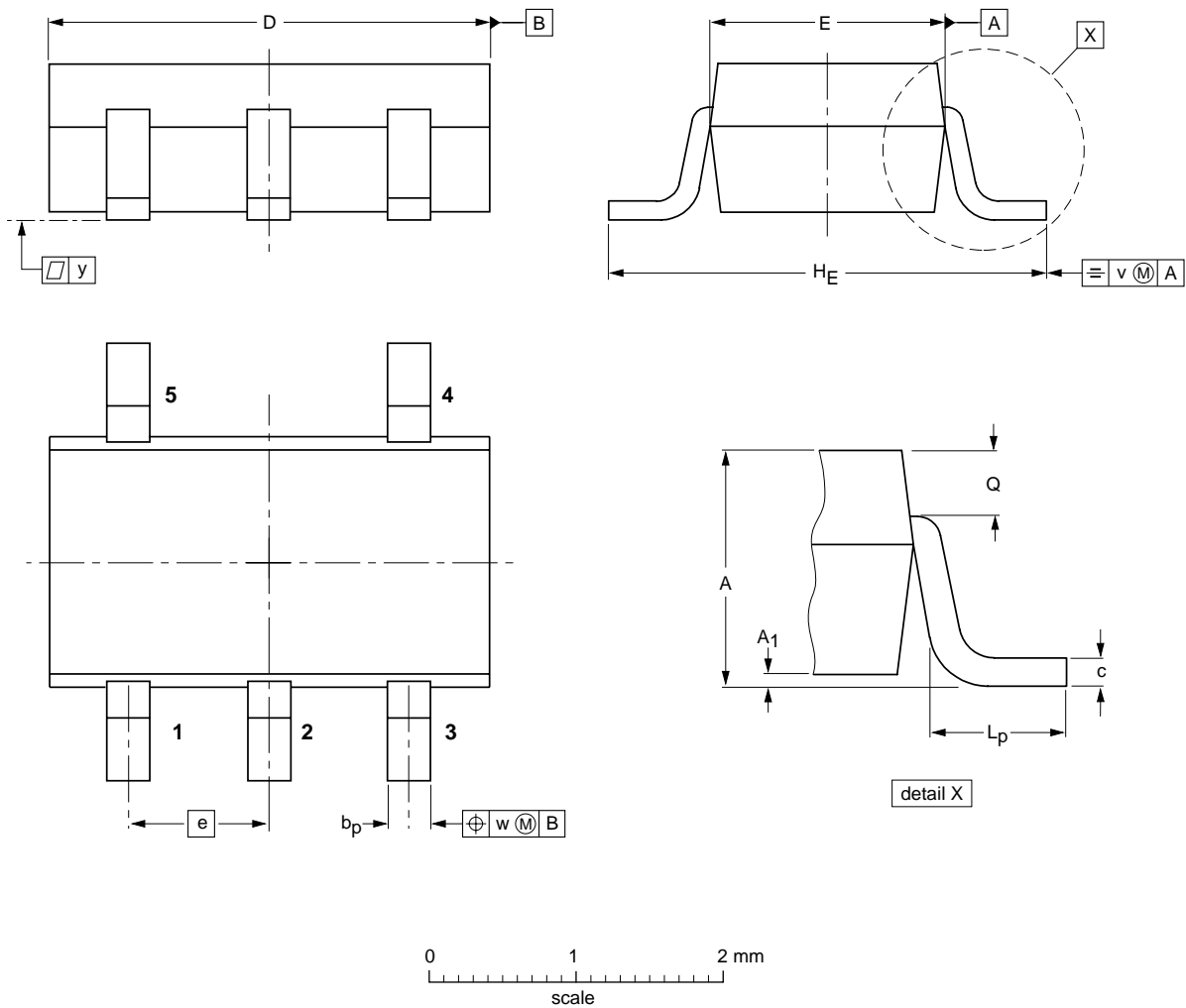


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Plastic surface mounted package; 5 leads

SOT753



DIMENSIONS (mm are the original dimensions)

| UNIT | A          | A <sub>1</sub> | b <sub>p</sub> | c            | D          | E          | e    | H <sub>E</sub> | L <sub>p</sub> | Q            | v   | w   | y   |
|------|------------|----------------|----------------|--------------|------------|------------|------|----------------|----------------|--------------|-----|-----|-----|
| mm   | 1.1<br>0.9 | 0.100<br>0.013 | 0.40<br>0.25   | 0.26<br>0.10 | 3.1<br>2.7 | 1.7<br>1.3 | 0.95 | 3.0<br>2.5     | 0.6<br>0.2     | 0.33<br>0.23 | 0.2 | 0.2 | 0.1 |

| OUTLINE<br>VERSION | REFERENCES |       |        |  | EUROPEAN<br>PROJECTION  | ISSUE DATE |
|--------------------|------------|-------|--------|--|---|------------|
|                    | IEC        | JEDEC | JEITA  |  |   |            |
| SOT753             |            |       | SC-74A |  |  | 02-04-16   |

## Single D-type flip-flop; positive-edge trigger

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### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA packages
  - for packages with a thickness  $\geq 2.5$  mm
  - for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.



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## Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE <sup>(1)</sup>   | SOLDERING METHOD                  |                       |
|--|-----------------------------------|-----------------------|
|  | WAVE                              | REFLOW <sup>(2)</sup> |
| BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA                                     | not suitable                      | suitable              |
| DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable <sup>(3)</sup>       | suitable              |
| PLCC <sup>(4)</sup> , SO, SOJ  | suitable                          | suitable              |
| LQFP, QFP, TQFP  | not recommended <sup>(4)(5)</sup> | suitable              |
| SSOP, TSSOP, VSO, VSSOP  | not recommended <sup>(6)</sup>    | suitable              |

## Notes

1. For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## ADDITIONAL SOLDERING INFORMATION

The SOT353 and SOT753 packages are suitable for both wave and reflow soldering methods. For more detailed information on these soldering methods refer to “Data Handbook SC18 - Discrete Semiconductor Packages” which can be found on URL <http://www.semiconductors.philips.com/package>.

## Single D-type flip-flop; positive-edge trigger

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## DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS <sup>(1)</sup> | PRODUCT STATUS <sup>(2)(3)</sup> | DEFINITION   |
|-------|----------------------------------|----------------------------------|--|
| I     | Objective data                   | Development                      | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.  |
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**NOTES**

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## **Contact information**

For additional information please visit **<http://www.semiconductors.philips.com>**. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to: **[sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com)**.

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