Features

- **Wide voltage range: 2.7V–3.6V**
- **Ultra-low active, standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Package available in a standard 44-pin TSOP Type II (forward pinout) package**
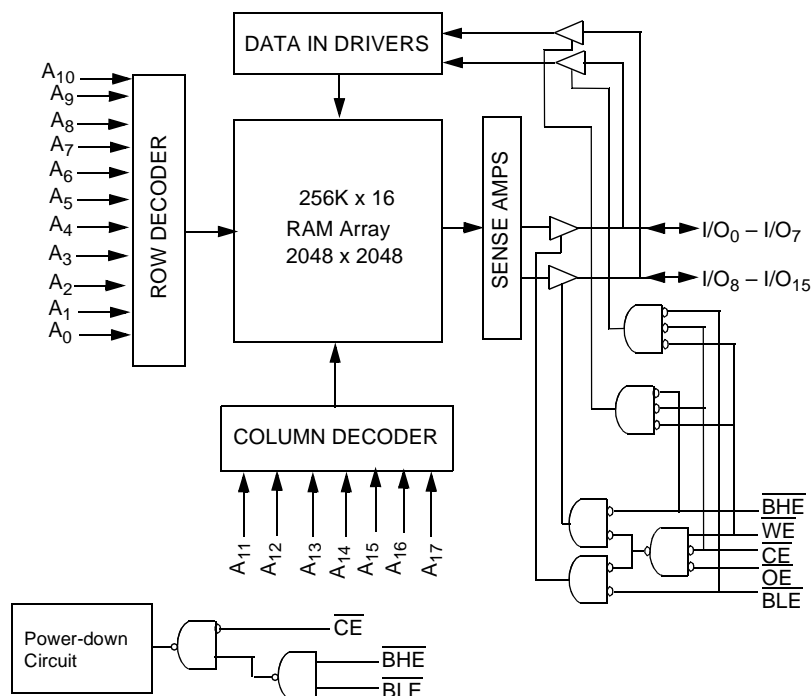
Functional Description[1]

The CY62147V is a high-performance CMOS static RAM organized as 256K words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The devices also have an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}$ HIGH) or when $\overline{CE}$ is LOW and both $\overline{BLE}$ and $\overline{BHE}$ are HIGH. The input/output pins (I/O$_0$ through I/O$_{15}$) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O$_0$ through I/O$_7$), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O$_8$ through I/O$_{15}$) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O$_0$ to I/O$_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O$_8$ to I/O$_{15}$. See the truth table at the back of this data sheet for a complete description of read and write modes.
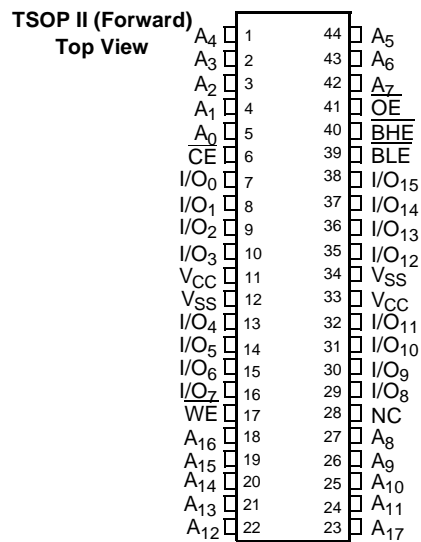
Logic Block Diagram

Note:
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

Pin Configurations

TSOP II (Forward)
Top View

A_4	1	44	A_5
A_3	2	43	A_6
A_2	3	42	A_7
A_1	4	41	$\overline{OE}$
A_0	5	40	$\overline{BHE}$
$\overline{CE}$	6	39	$\overline{BLE}$
I/O_0	7	38	I/O_{15}
I/O_1	8	37	I/O_{14}
I/O_2	9	36	I/O_{13}
I/O_3	10	35	I/O_{12}
V_{CC}	11	34	V_{SS}
V_{SS}	12	33	V_{CC}
I/O_4	13	32	I/O_{11}
I/O_5	14	31	I/O_{10}
I/O_6	15	30	I/O_9
I/O_7	16	29	I/O_8
$\overline{WE}$	17	28	NC
A_{16}	18	27	A_8
A_{15}	19	26	A_9
A_{14}	20	25	A_{10}
A_{13}	21	24	A_{11}
A_{12}	22	23	A_{17}

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State[2] ....−0.5V to V_{CC} + 0.5V

DC Input Voltage[2] .... −0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)............................. 20 mA

Static Discharge Voltage.. > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current.. > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	−40°C to +85°C	2.7V to 3.6V

Product Portfolio

	V_{CC} Range (V)			Speed (ns)	Power Dissipation			
					Operating I_{CC}, (mA)		Standby I_{SB2}, (µA)	
Product	$V_{CC(min.)}$	$V_{CC(typ.)}$[3]	$V_{CC(max.)}$		Typ.[3]	Maximum	Typ.[3]	Maximum
CY62147VLL	2.7	3.0	3.6	70	7	15	2	20

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62147V-70			Unit
				Min.	Typ.[3]	Max.	
V_{OH}	Output HIGH Voltage	$I_{OH} = −1.0$ mA	$V_{CC} = 2.7V$	2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA	$V_{CC} = 2.7V$			0.4	V
V_{IH}	Input HIGH Voltage		$V_{CC} = 3.6V$	2.2		V_{CC} + 0.5V	V
V_{IL}	Input LOW Voltage		$V_{CC} = 2.7V$	−0.5		0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$		−1	±1	+1	µA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled		−1	+1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	$I_{OUT} = 0$ mA, $f = f_{MAX} = 1/t_{RC}$, CMOS Levels	$V_{CC} = 3.6V$		7	15	mA
		$I_{OUT} = 0$ mA, $f = 1$ MHz, CMOS Levels			1	2	mA

Notes:
2. $V_{IL(min.)} = −2.0V$ for pulse durations less than 20 ns.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

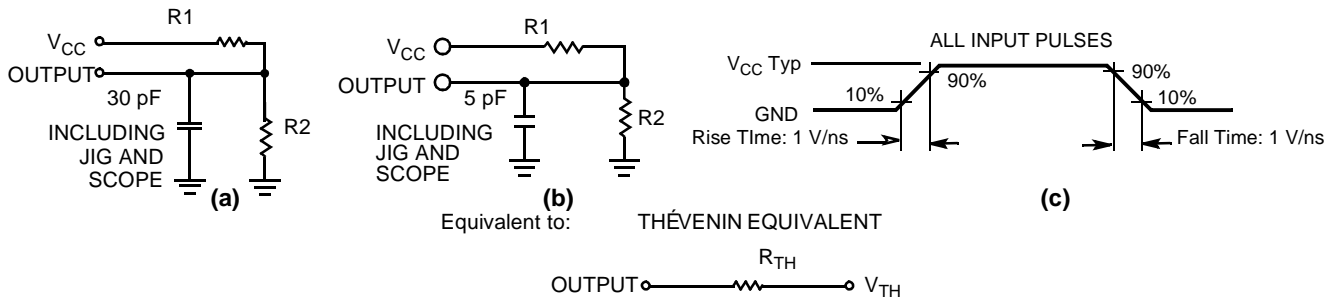**Electrical Characteristics** Over the Operating Range (continued)

Parameter	Description	Test Conditions		CY62147V-70 Min.	CY62147V-70 Typ.[3]	CY62147V-70 Max.	Unit
I_{SB1}	Automatic CE Power-down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, f = f$_{MAX}$			2	20	µA
I_{SB2}	Automatic CE Power-down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, f = 0	$V_{CC} = 3.6V$				

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = V_{CC(typ.)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance

Parameter	Description	Test Conditions	BGA	TSOPII	Units
Θ_{JA}	Thermal Resistance (Junction to Ambient)[4]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	55	60	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[4]		16	22	°C/W

AC Test Loads and Waveforms

Parameter	3.0V	Unit
R1	1105	Ω
R2	1550	Ω
R_{TH}	645	Ω
V_{TH}	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ.[3]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0		3.6	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$; No input may exceed $V_{CC} + 0.3V$		1	10	µA
t_{CDR}[4]	Chip Deselect to Data Retention Time		0			ns
t_R[5]	Operation Recovery Time		70			ns

Note:
4. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Waveform

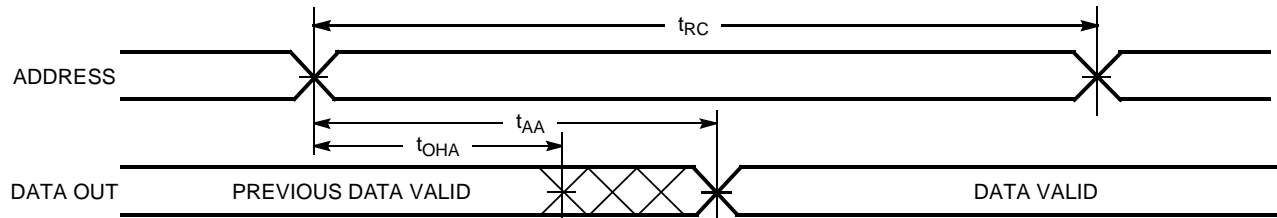## Switching Characteristics Over the Operating Range[6]

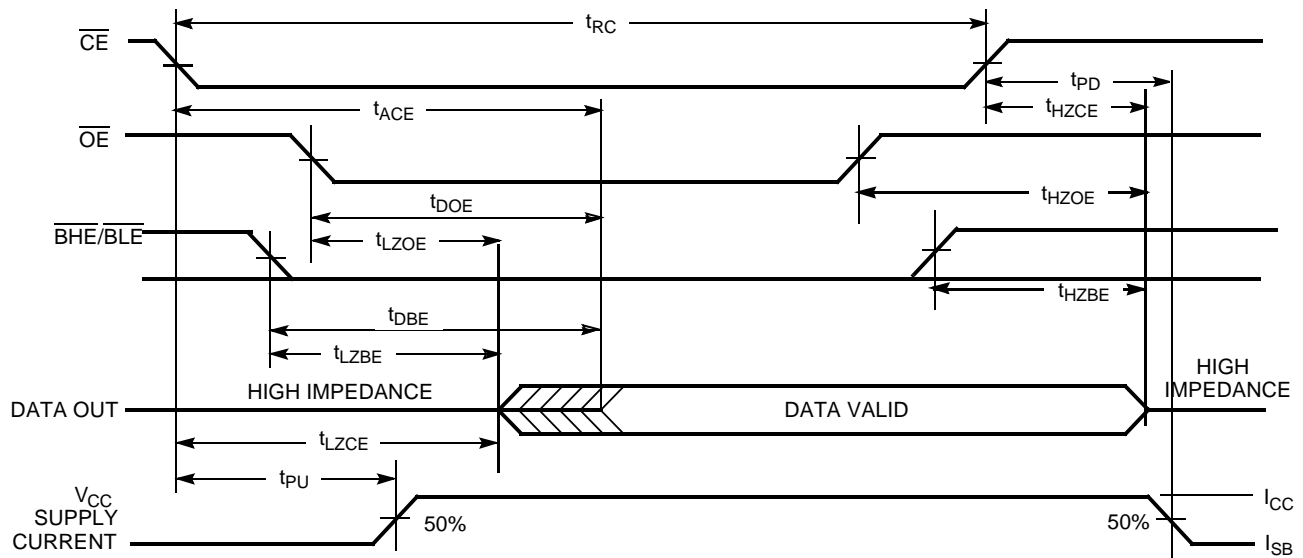| Parameter	Description	70 ns Min.	70 ns Max.	Unit
Read Cycle				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	CE LOW to Data Valid		70	ns
t_{DOE}	OE LOW to Data Valid		25	ns
t_{LZOE}	OE LOW to Low-Z[7, 9]	5		ns
t_{HZOE}	OE HIGH to High-Z[9]		20	ns
t_{LZCE}	CE LOW to Low-Z[7]	10		ns
t_{HZCE}	CE HIGH to High-Z[7, 9]		20	ns
t_{PU}	CE LOW to Power-up	0		ns
t_{PD}	CE HIGH to Power-down		70	ns
t_{DBE}	BHE / BLE LOW to Data Valid		70	ns
t_{LZBE}[8]	BHE / BLE LOW to Low-Z	5		ns
t_{HZBE}	BHE / BLE HIGH to High-Z		20	ns
Write Cycle[10, 11]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	CE LOW to Write End	60		ns
t_{AW}	Address Set-up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	WE Pulse Width	40		ns
t_{BW}	BHE / BLE Pulse Width	60		ns
t_{SD}	Data Set-up to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	WE LOW to High-Z[7, 9]		25	ns
t_{LZWE}	WE HIGH to Low-Z[7]	10		ns

Notes:
5. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)}$ > 10 µs or stable at $V_{CC(min.)}$ >10 µs.
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. If both byte enables are toggled together this value is 10ns
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle #3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.
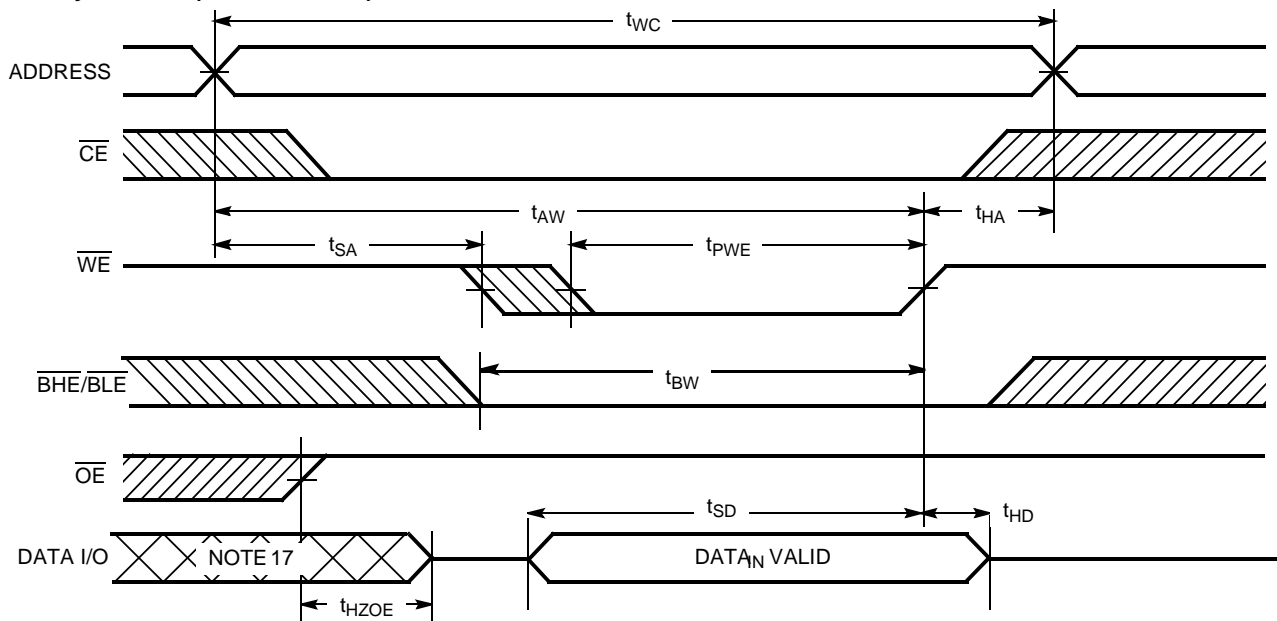
Switching Waveforms
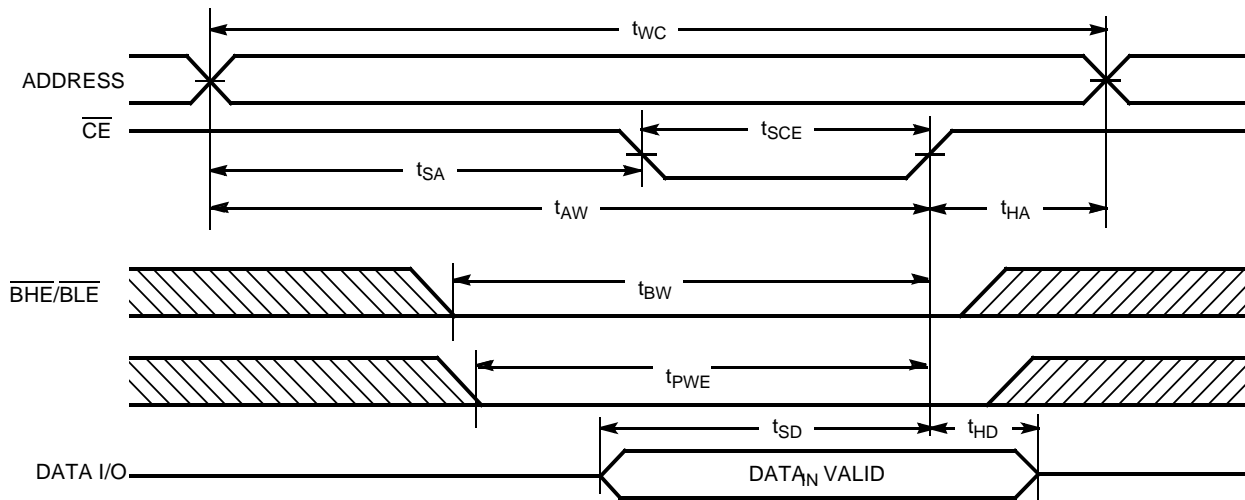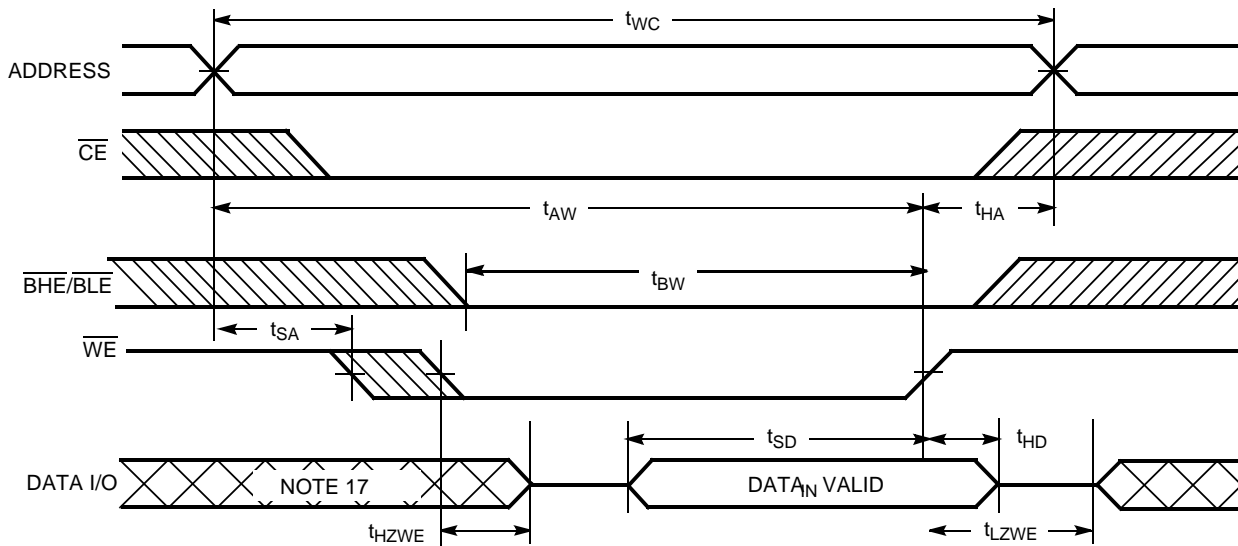
Read Cycle No. 1 [12, 13]

Read Cycle No. 2 [13, 14]

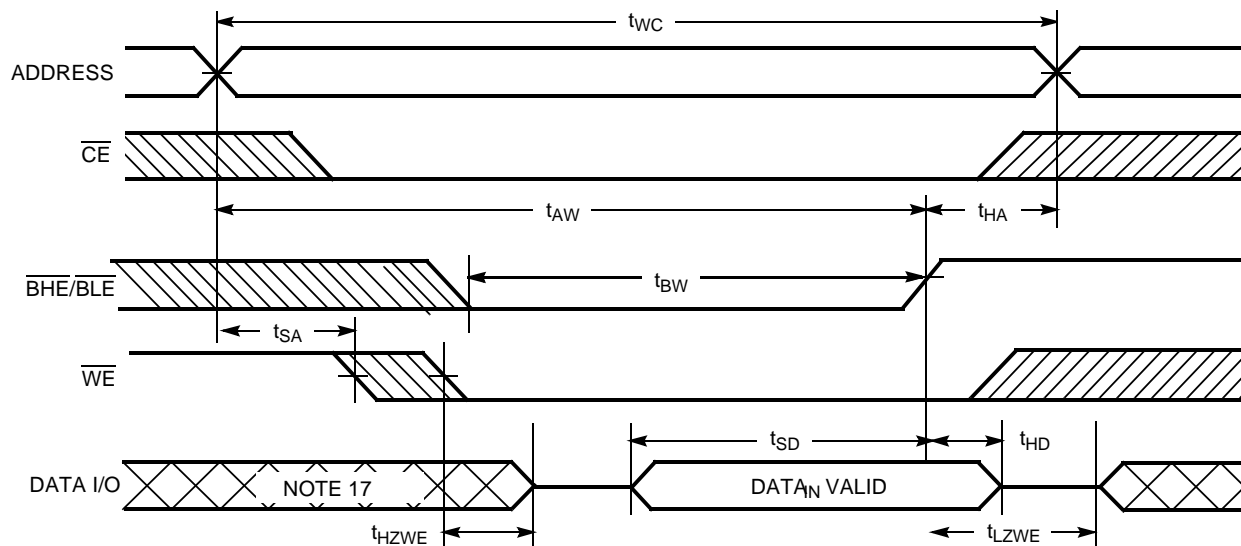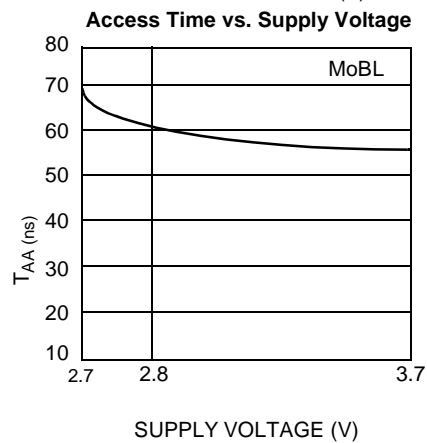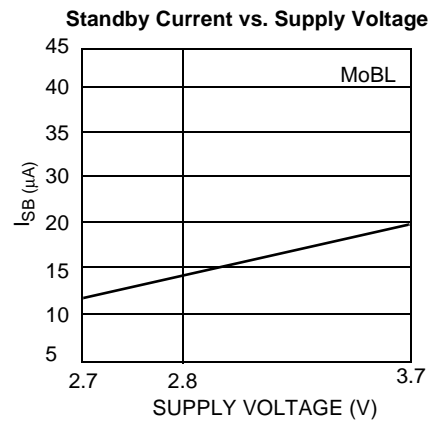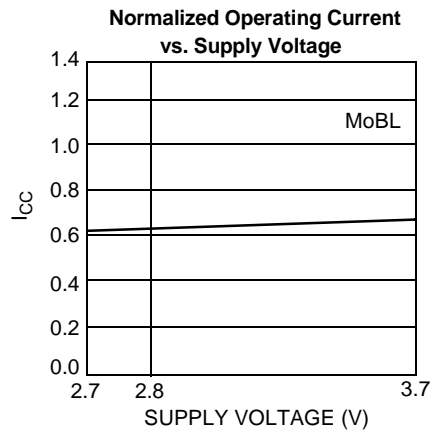### Write Cycle No. 1 ($\overline{WE}$ Controlled) [10, 15, 16]

Notes:
12. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 15, 16]

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[11, 16]

Notes:
15. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[17]
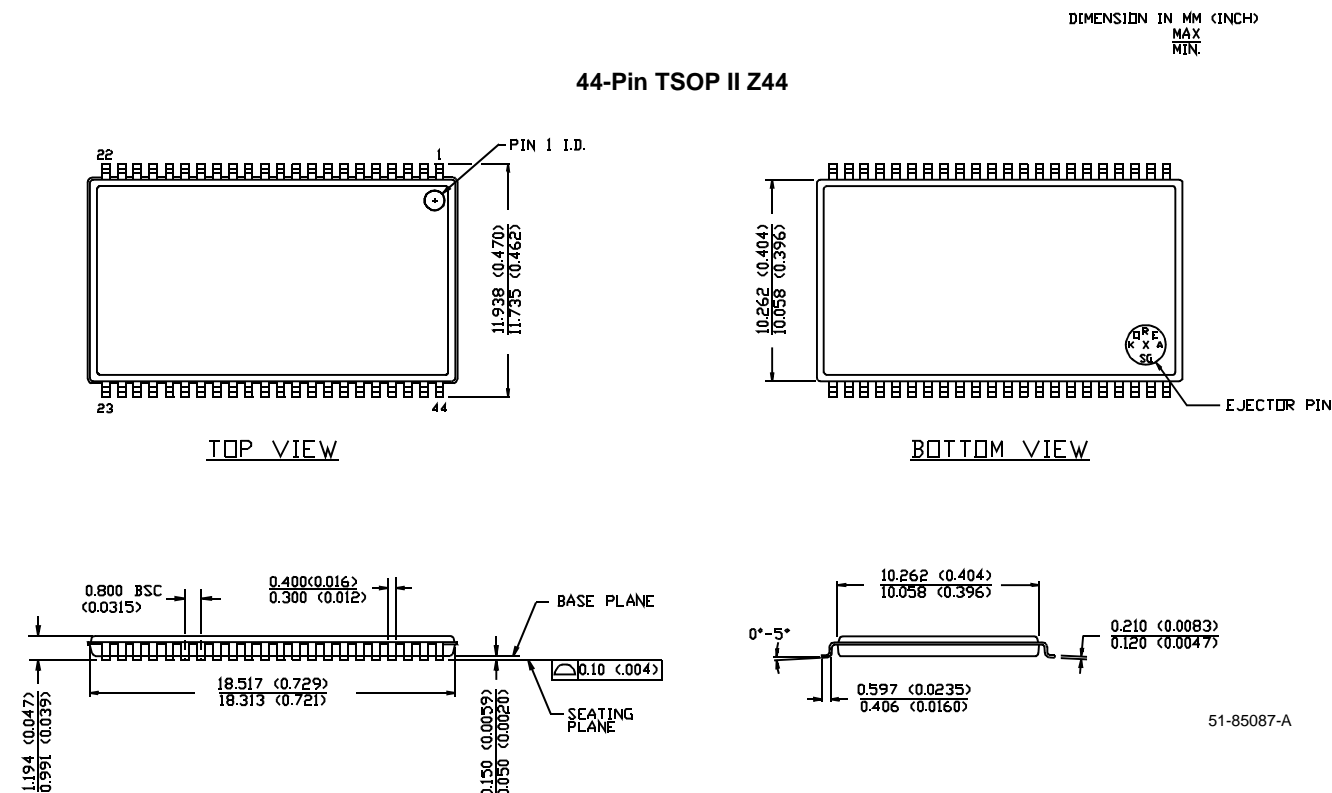

Typical DC and AC Characteristics

Normalized Operating Current vs. Supply Voltage

Standby Current vs. Supply Voltage

Access Time vs. Supply Voltage

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	X	X	H	H	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O$_O$–I/O$_{15}$)	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O$_O$–I/O$_7$); I/O$_8$–I/O$_{15}$ in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O$_8$–I/O$_{15}$); I/O$_0$–I/O$_7$ in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O$_O$–I/O$_{15}$)	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O$_O$–I/O$_7$); I/O$_8$–I/O$_{15}$ in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O$_8$–I/O$_{15}$); I/O$_0$–I/O$_7$ in High-Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62147VLL-70ZI	Z44	44-pin TSOP II	Industrial

Package Diagram

44-Pin TSOP II Z44

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Document Title: CY62147V MoBL® 4M (256K x 16) Static RAM
Document Number: 38-05050

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109958	12/16/01	SZV	Changed from Spec number: 38-00757 to 38-05050
A	116514	09/04/02	GBI	Added footnote 1. Deleted fBGA package (replacement fBGA package is available in CY62147CV30).