

TUSB6015 USB 2.0 High Speed Peripheral Controller Data Sheet

FEATURES

- USB 2.0 High-Speed (HS) Compliant Peripheral Controller Core
 - USB-IF TID # 40630005
- Integrated USB 2.0 PHY
- NOR FLASH - Like External Host Interface
- DP/DM lines are high impedance when the device is not powered
- Six physical endpoints
 - Each endpoint is configurable as IN or OUT with dedicated 1K buffer
- NOR Flash Interface Access modes:
 - Asynchronous 16-bit single access
 - Asynchronous 32-bit single access
 - Asynchronous 16x16 burst access w/ DMA
 - Synchronous 16x16 burst access with DMA (Max GPMC clock is 65 MHz)
- Interrupt on DP/DM line state change for CEA-936-A detect
- VBUS MAX Voltage rating will be 6V for USB Charging
- RoHS Complaint 80 Terminal BGA MICROSTAR JUNIOR Package

DESCRIPTION

The TUSB6015 is a USB 2.0 HS Peripheral Controller designed for seamless interface to an external Host processor through the NOR FLASH-like interface.

The NOR FLASH-like interface is a 16-bit, multiplexed address/data, interface with support for synchronous burst and single asynchronous read/write access. Configuration registers are accessible via the asynchronous chip select only; the End Point FIFO's are accessible via both the synchronous and asynchronous chip selects.

The device also has eight user configurable general purpose I/O interface pins. The GPIO can be configured as an interrupt or wakeup source. Some GPIO have secondary NOR-flash DMA Request functionality.

The device is fully compliant with the Universal Serial Bus Specification Rev. 2.0.

The ESD protection level is 2KV HBM (JESD22-A114D), 500V CDM (JESD22-C101C).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appear at the end of this data sheet.

TUSB6015ZQE

SLLS937
REVISION 1.4 SEPTEMBER 12, 2008

Ordering Information¹

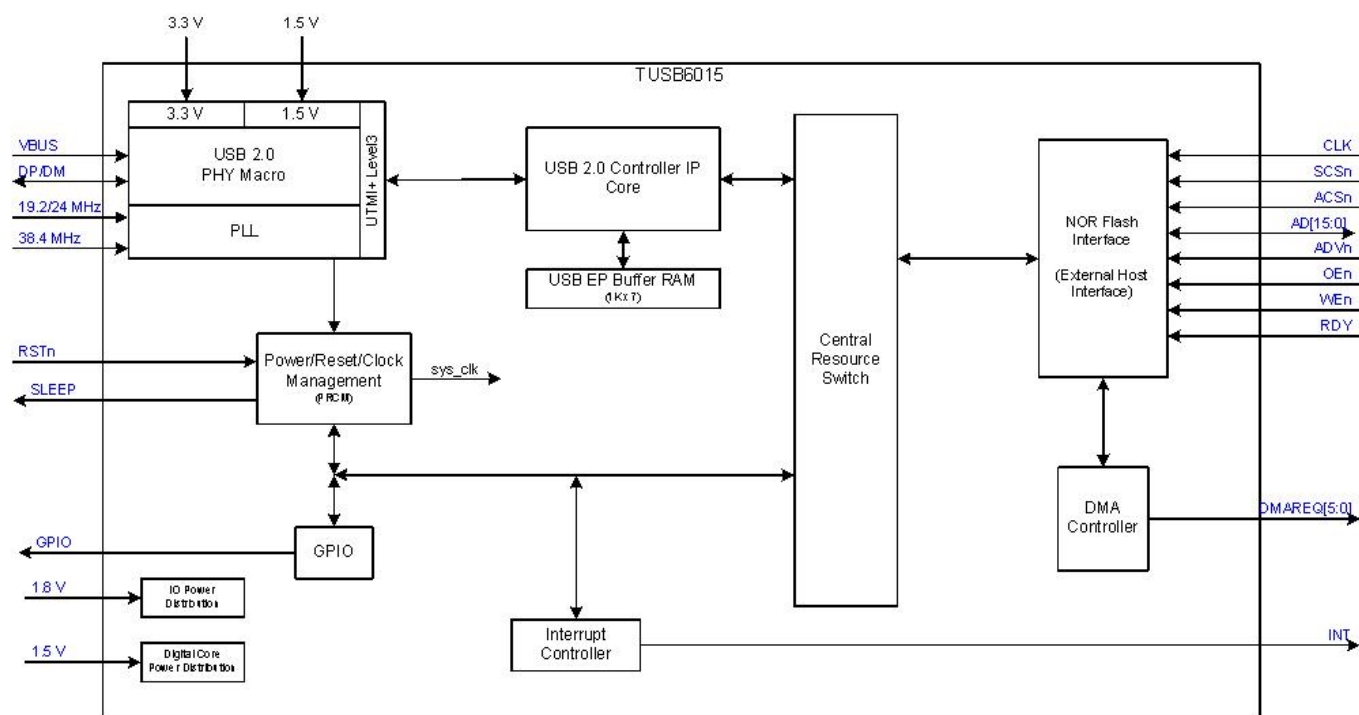
PACKAGED DEVICES	PACKAGE ²	MARKING
TUSB6015IZQE	ZQE	TUSB6015I
TUSB6015IZQER• ³	ZQE	TUSB6015I

¹ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

² Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

³The tape and reel option is available for TUSB6015IZQE by adding an R suffix.

Device Block Diagram



Electrical Characteristics

Absolute Maximum Ratings¹

3.3V Supply Voltage, VDDA3P3.....	-0.5 V to 4.2 V
1.8V Supply Voltage VDD18.....	-0.5 V to 2.1 V
1.5V Supply Voltage, VDD15, VDDD1P5, VDDCM1P5, VDDA1P5.....	-0.5 V to 2.1 V
USB VBUS Supply Voltage ²	0 V to 6.0 V
Input voltage, V_I , 3.3V USB ³	-0.5 V to VDDA3P3 + 0.5 V
Output voltage, V_O , 3.3V USB.....	-0.5 V to VDDA3P3 + 0.5 V
Input clamp current, I_{IK}	±20 mA
Output clamp current, I_{OK}	±20 mA
Storage temperature range, Tstg	-65°C to 150°C

Recommended Operating Conditions

PARAMETER			MIN	TYP	MAX	UNIT
VDDA3P3	Supply voltage for PHY Analog		3	3.3	3.6	V
VDD18	Supply voltage for Digital I/O		1.62	1.8	1.98	V
VDD15	Supply voltage for Digital Core	TUSB6015I (Industrial grade)	1.35	1.5	1.65	V
VDDD1P5	Supply voltage for PHY Digital					
VDDCM1P5	Supply voltage for PHY Common Module					
VDDA1P5	Supply voltage for PHY Analog					
T _A	Operating Temperature		-40		85	°C

¹Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

²VBUS can tolerate 6V for the lifetime of the device. It can handle 6.5V for 36 hours.

³TUSB6015 complies with short circuit withstand and AC stress conditions as described in Chapter 7.1.1 of the USB 2.0 specification.

Electrical Characteristics for the Digital I/O **$T_A = -30^{\circ}\text{C} - 85^{\circ}\text{C}$, $V_{DD18} = 1.8\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$ (Unless otherwise noted)**

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage	LVC MOS		0		V_{DD18}	V
V_O	Output voltage	LVC MOS		0		V_{DD18}	V
V_{IH}	High-level input voltage	LVC MOS		$0.7 \times V_{DD18}$		V_{DD18}	V
V_{IL}	Low-level input voltage	LVC MOS		0		$0.3 \times V_{DD18}$	V
V_{OH}	High-level output voltage	LVC MOS	$I_{OH} = 8\text{mA}$	$0.8 \times V_{DD18}$			V
V_{OL}	Low-level output voltage	LVC MOS open-drain	$I_{OL} = 4\text{mA}$			$0.22 \times V_{DD18}$	V
		LVC MOS	$I_{OL} = 8\text{mA}$			$0.22 \times V_{DD18}$	
		LVC MOS (1.5V_SWEN, 3.3V_SWEN only)	$I_{OL} = 100\mu\text{A}$		10		mV
I_{IH}	High-level input current	LVC MOS	$V_I = V_I \text{ max}$			± 1	μA
I_{IL}	Low-level input current	LVC MOS	$V_I = V_I \text{ min}$			± 1	μA
I_{OZ}	Output leakage current (high-Z)		$V_I = V_I \text{ max or } V_{SS}$			± 20	μA
C_i	Input Capacitance (1.8V NOR Interface)					2.43	pF
t_r, t_f	Input rise/fall time			0		25	ns

Vbus - Electrical Characteristics for the Integrated USB 2.0 Transceiver, **$T_A = -30^{\circ}\text{C} - 85^{\circ}\text{C}$, $V_{DD15} = 1.5\text{V} \pm 10\%$, $V_{DD18} = 1.8\text{V} \pm 10\%$, $V_{DDA1P5} = 1.5\text{V} \pm 10\%$,** **$V_{DDA3P3} = 3.3 \pm 10\%$, $V_{DDD1P5} = 1.5\text{V} \pm 10\%$, $V_{DDCM1P5} = 1.5 \pm 10\%$, $V_{SS} = 0\text{V}$ (unless****otherwise noted)[†]**

PARAMETER	MIN	TYP	MAX	UNIT
Input Levels				
Vbus Input Impedance	360		690	k Ω
Vbus Valid Comparator	4.4		4.75	V
Vbus leakage current (when device is powered off)			11	μA

[†]Characterization only. Limits approved by design.

DP and DM - Electrical Characteristics for the Integrated USB 2.0 Transceiver

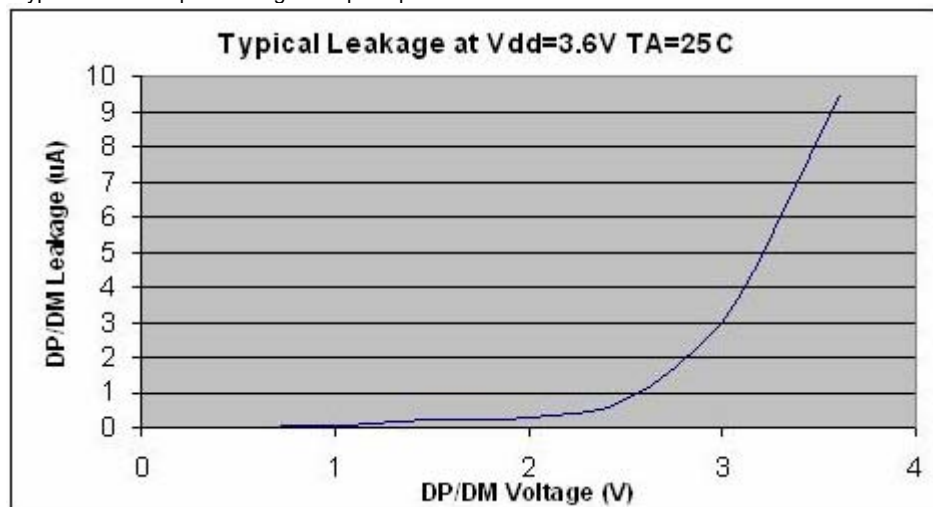
$T_A = -30^{\circ}\text{C} - 85^{\circ}\text{C}$, $V_{DD15} = 1.5\text{V} \pm 10\%$, $V_{DD18} = 1.8\text{V} \pm 10\%$, $V_{DDA1P5} = 1.5\text{V} \pm 10\%$, $V_{DDA3P3} = 3.3 \pm 10\%$, $V_{DDD1P5} = 1.5\text{V} \pm 10\%$, $V_{DDCM1P5} = 1.5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$ (unless otherwise noted)[†]

PARAMETER		MIN	TYP	MAX	UNIT
Input Levels for Full Speed					
V_{DI}	Full-speed differential input threshold	0.2			V
V_{CM}	Input (was differential) common mode range	0.8		2.5	V
Input Levels for High Speed					
$V(HSSQ)$	High-speed squelch detection threshold (differential signal amplitude)	100		150	mV
V_{DI}	High-speed differential input threshold voltage	100			mV
$CHSLOAD$	Capacitance to ground on each line			5.5	pF
Output Levels for Full Speed					
V_{OL}	Low-level output voltage	0		0.3	V
V_{OH}	High-level output voltage (driven)	2.8		3.6	V
$V_{O(SE1)}$	Output voltage on SE1	0.8			V
$V_{O(CRS)}$	Output signal crossover voltage	1.3		2	V
Output Levels for High Speed					
$V(HSOI)$	High-speed idle level	-10		10	mV
$V(HSOH)$	High-speed data signaling high	360		440	mV
$V(HSOL)$	High-speed data signaling low	-10		10	mV
$V_{ID(CHIRPJ)}$	Chirp J level (differential voltage)	700		1100	mV
$V_{ID(CHIRPK)}$	Chirp K level (differential voltage)	-900		-500	mV
Driver Characteristics (Full Speed)					
t_r	Full-speed rise time	4		20	ns
t_f	Full-speed fall time	4		20	ns
$t(RFM)$	Full-speed rise/fall time matching	90%		110%	
Driver Characteristics (High Speed)					
t_r	Rise time (10%-90%)	500			ps
t_f	Fall time (10%-90%)	500			ps
$r_{O(HSDRV)}$	Driver output resistance (serves as a high-speed termination)	40.5		49.5	Ω
$t(FRFM)$	Differential rise and fall time matching	90%		111.11%	
Clock Timings					
$t(HSDRAT)$	High-speed data rate	479.76		480.24	Mb/s
Single-Ended Receiver					
V_{IT+}	Positive-going input threshold voltage			2.0	V
V_{IT-}	Negative-going input threshold voltage	0.8			V
V_{hys}	Hysteresis voltage	200		500	mV

DP and DM - Electrical Characteristics for the Integrated USB 2.0 Transceiver (CONT'D)

INPUT LEAKAGE		TEST CONDITION	MIN	TYP	MAX	UNIT
DP/DM	Measurement taken with pull-up/dn disabled and device in idle mode	DP/DM Voltage = 0 – VDDA3.3	-1.3		1.3	uA
DP/DM	Measurement taken with pull-up/dn disabled and device in active mode	DP/DM Voltage = 2V		See Chart ¹	1.3	uA

†Characterization only. Limits approved by design.

¹Typical DP/DM Input Leakage with pull-up/dn disabled and device in active mode

Power Sequencing Guidelines

Power-On Reset

The system reset function ensures an orderly start-up sequence for the TUSB6015. There is a one active low external system reset input (RSTn). The reset initializes the Power/Reset/Clock Manager (PRCM) module, which in turn generates all the internal resets to initialize USB 2.0 PHY Macro and synchronous logic in the core. While reset is asserted (active low), the dual functional pin is sampled to determine device configuration after reset.

Since TUSB6015 relies on a dual function pin to configure the device during reset, the reset must be sufficiently long for (external) marginal pull-up/pull-down to achieve the intended levels. Reset pulse duration should be at least three times actual RC constant time (with typical 22 kOhm marginal pull-up resistor with 50 pF load, reset pulse should be at least 3.3 μ s).

All functional pins remain in same state even after RSTn is de-asserted and stay in that state until internal core reset is cleared. The internal core reset is held for 16 system clock cycles following low-to-high RSTn transition.

Upon power-on reset, the following must be determined for proper device initialization:

- System reference clock source

Device uses dual-mode pin to determine initial clock input setup. Dual function pin is latched during the reset. After the reset this terminal assumes the normal functionality.

External Pin	Function	Description
GPIO6	Reference Clock Frequency Select	Determines the reference clock pin 0 – 38.4 MHz (CLKIN_38_4 pin is used) 1 – 19.2 MHz (CLKIN_19_2_24 pin is used)
CLK_24_SEL	CLKIN_19_2_24 Frequency Select	Determines the reference frequency of the CLKIN_19_2_24 pin 0 – RSVD 1 – 19.2 MHz If GPIO6 is low at reset, this pin will have no effect on clock selection.

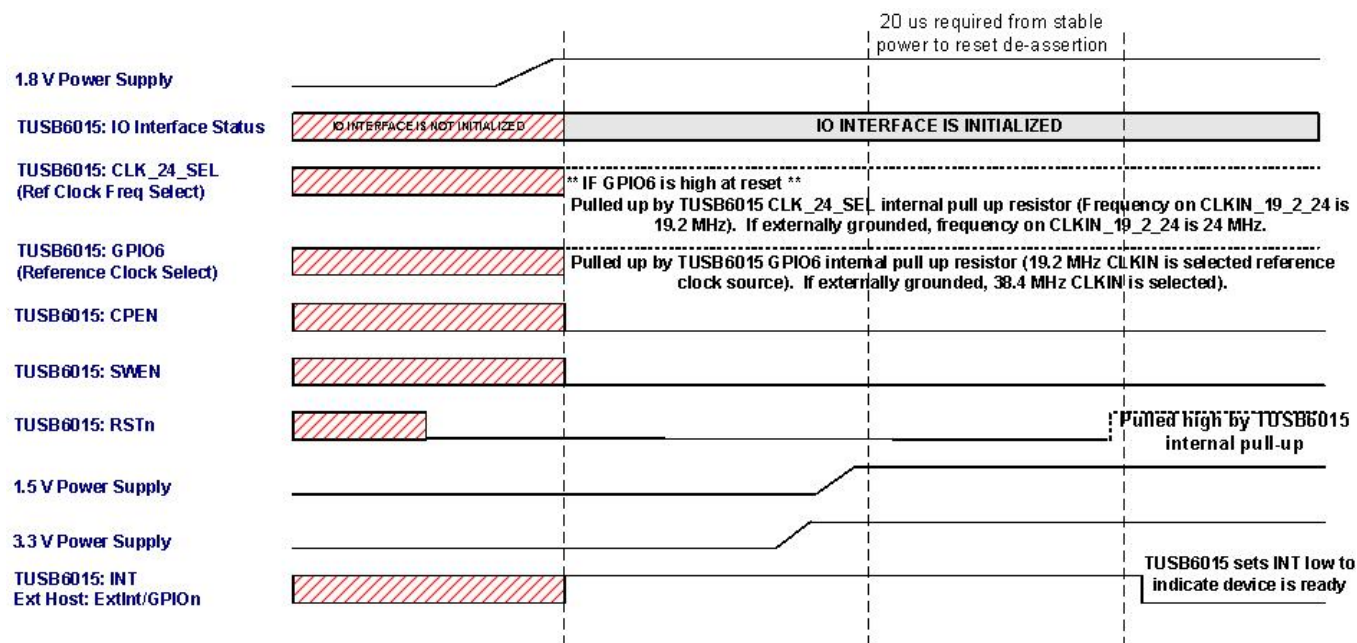
Upon exiting reset, the USB 2.0 PHY is not in the suspend state and the system clock (60 MHz) is enabled and free running. The USB 2.0 HS Peripheral Controller Core powers up and a session is not enabled. With session not enabled, all the USB 2.0 HS Peripheral Controller Core State Machine's are in the idle state.

After reset is de-asserted, the device asserts the DevReady interrupt to the External Host to indicate that it is ready to be programmed. The host reads the NOR Flash Interrupt Source register and decides how to proceed based on the device's current status.


TUSB6015ZQE

SLLS937
REVISION 1.4 SEPTEMBER 12, 2008

System Power-Up Sequence



NOTE: Reference Clock Source selection is latched on RSTn rising edge.
No external components are required to select 19.2 MHz CLKIN as a reference clock source.

 Signal state cannot be guaranteed

 Signal state is stable and valid

Input Supply Current

$$T_A = 25^{\circ}\text{C}$$

VDDA3.3 = 3.3V +/- 10%, VSS = 0V

PARAMETER		TEST CONDITIONS	TYP	UNIT
IDD	Input supply current	Idle ¹	16.5	uA
		No Bus Activity ²	3.7	mA
		Active (Transmit / Receive) ³	3.6	mA
		Reset ⁴	2.7	mA

VDD1.8⁷ = 1.8V +/- 10%, VSS = 0V

PARAMETER		TEST CONDITIONS	TYP	UNIT
IDD	Input supply current	Idle ¹	0.26	uA
		No Bus Activity ²	157.0	uA
		Active (Transmit / Receive) ³	350.0	uA
		Reset ⁴	1.8	mA

Cumulative VDD1.5 = 1.5V +/- 10%, VSS = 0V

(VDD1.5, VDDD1.5, VDDCM1.5, VDDA1.5)

PARAMETER		TEST CONDITIONS	TYP	UNIT
IDD	Input supply current	Idle ¹	2.0	uA
		No Bus Activity ²	56.5	mA
		Active (Transmit / Receive) ³	58.0	mA
		Reset ⁴	29.2	mA

¹ DevIdle bit set in Device PRCM Management Register, USB cable unplugged.

² Normal operation with no packets being transferred on the USB, except SOF every 125 μ s.

³ Bulk IN and OUT on one End Point. Packet size is 512 bytes.

⁴ TUSB6015 RSTn asserted.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appear at the end of this data sheet.

Input Clock Requirements

CLKIN 19.2 MHz Recommended Operating Conditions

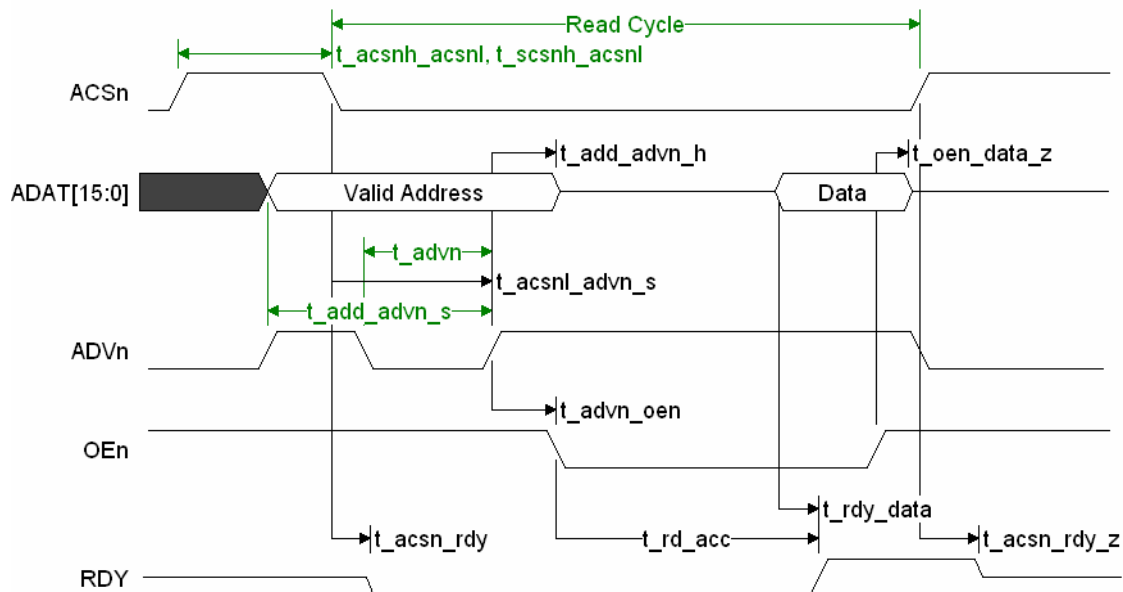
PARAMETER	VALUE
Nominal Clock Frequency (GPIO6 = high @ reset) (CLK_24_SEL = high @ reset)	19.20 MHz
Frequency Accuracy	+/- 100 ppm
Maximum Rise/Fall Time	5ns (10% to 90%)
Input Clock Type	Square Wave
Duty Cycle	45% - 55%
Input Capacitance Loading	4pF
Jitter	118 ps

CLKIN 38.4 MHz Recommended Operating Conditions

PARAMETER	VALUE
Nominal Clock Frequency (GPIO6 = low @ reset)	38.40 MHz
Frequency Accuracy	+/- 100 ppm
Input Clock Type	Sinusoid
Duty Cycle	45% - 55%
Input Common Mode Voltage VCM (V_{CM})	1 V +/- 100 mV
Vp-p	200 mV – 800 mV
Input Capacitance Loading	5 pF
Rin	180 kOhms
Jitter	100 ps (peak-to-peak)

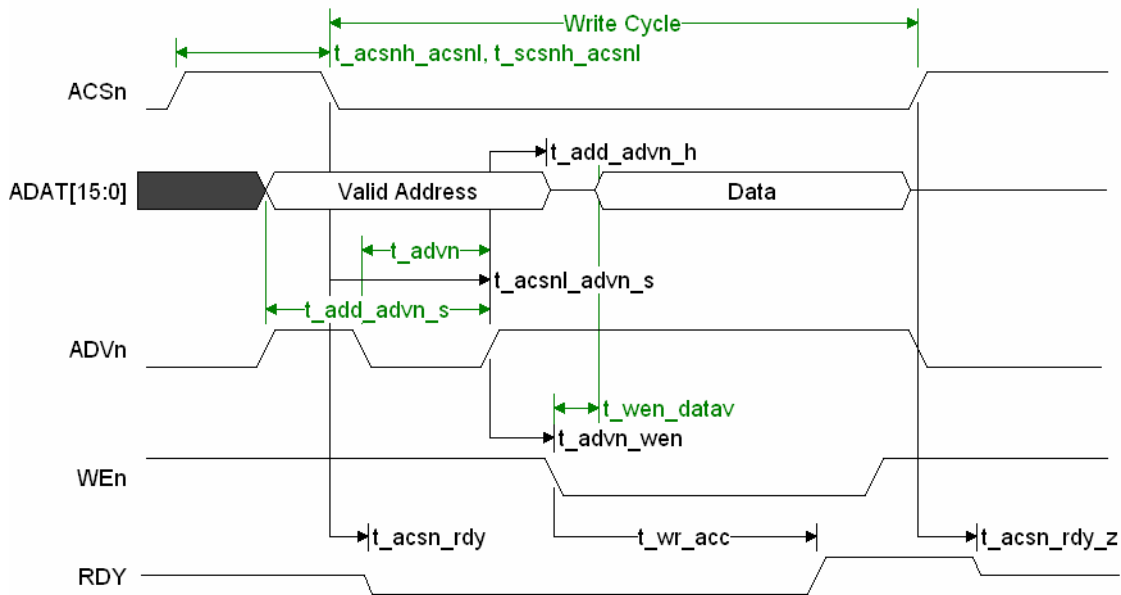
Timing Diagrams

Asynchronous Read Access



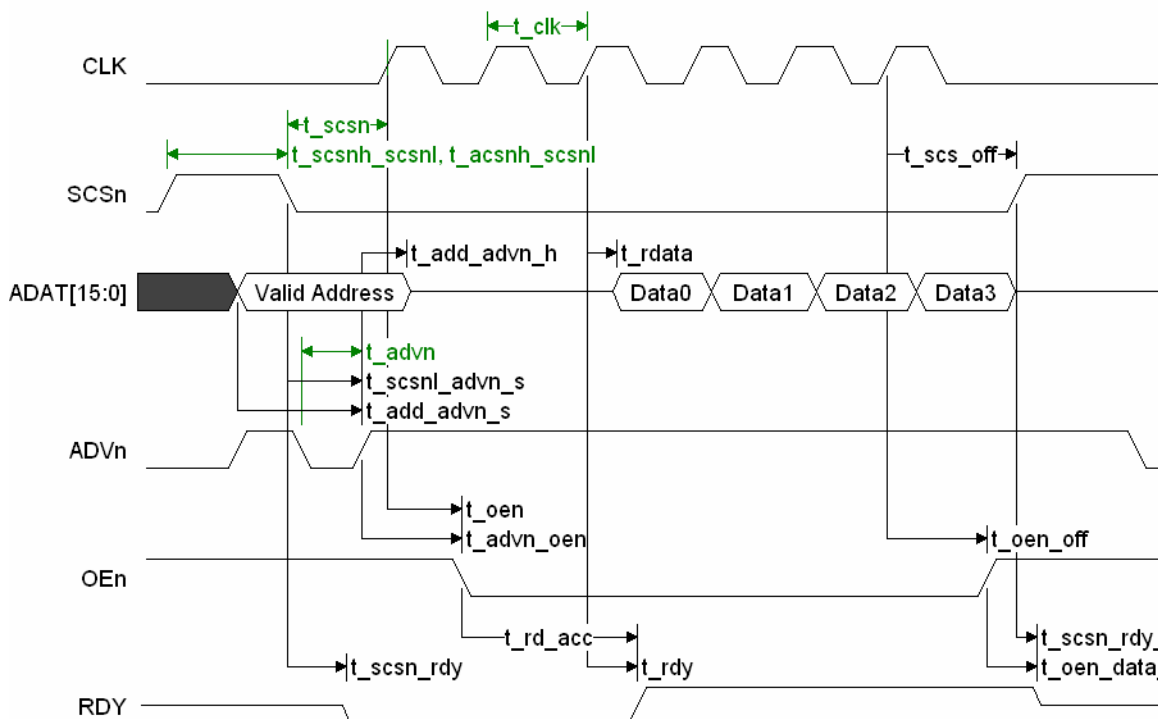
PARAMETER		MIN	MAX	UNIT
t_{acsnh_acsnl}	Delay time, ACSn high to ACSn low	8		ns
t_{scsnh_acsnl}	Delay time, SCSn high to ACSn low	8		ns
$t_{add_advn_h}$	Address Hold to ADVn high	0.8		ns
$t_{acsnl_advn_s}$	ACSn low Setup to ADVn high	18		ns
$t_{add_advn_s}$	Address Setup to ADVn high	18		ns
t_{advn_oen}	Sampled Address to OEn low	1		ns
t_{advn}	ADVn low pulse	7		ns
t_{rd_acc}	OEn low to RDY high (16-bit Register Access)	6	8	Sys Clk
	OEn low to RDY high (32-bit Register Access) 1 st 16-bit	5	7	Sys Clk
	OEn low to RDY high (32-bit Register Access) 2 nd 16-bit	2	4	Sys Clk
	OEn low to RDY high (FIFO Access, with DMAREQ) 1 st 16-bit	3	4	Sys Clk
	OEn low to RDY high (FIFO Access, with DMAREQ) 2 nd 16-bit	3	4	Sys Clk
t_{acsn_rdy}	ACSn low to RDY low		7	ns
$t_{acsn_rdy_z}$	ACSn high to RDY high-Z		7	ns
$t_{oen_data_z}$	OEn high to Data high-Z		8	ns
t_{rdy_data}	Delay time, RDY high to data valid	-1	6	ns

Asynchronous Write Access



PARAMETER		MIN	MAX	UNIT
t_acsnh_acsnl	Delay time, ACSn high to ACSn low	8		ns
t_scsnh_acsnl	Delay time, SCSn high to ACSn low	8		ns
t_add_advsn_h	Address Hold to ADVn high	0.8		ns
t_acsnl_advsn_s	ACSn low Setup to ADVn high	18		ns
t_add_advsn_s	Address Setup to ADVn high	18		ns
t_advsn	ADVn low pulse	7		ns
t_advsn_wen	ADVn to WEn low	1		ns
t_wr_acc	WEn low to RDY high (16-bit Register Access)	3	5	Sys Clk
	WEn low to RDY high (32-bit Register Access) 1 st 16-bit	2	4	Sys Clk
	WEn low to RDY high (32-bit Register Access) 2 nd 16-bit	3	7	Sys Clk
	WEn low to RDY high (FIFO Access, with DMAREQ) 1 st 16-bit	3	4	Sys Clk
	WEn low to RDY high (FIFO Access, with DMAREQ) 2 nd 16-bit	3	4	Sys Clk
t_acsn_rdy	ACSn low to RDY low		7	ns
t_acsn_rdy_z	ACSn high to RDY high-Z		7	ns
t_wen_datav	Delay time, WEn low to Data valid		1-5ns	Sys Clk

Synchronous Burst Read Access



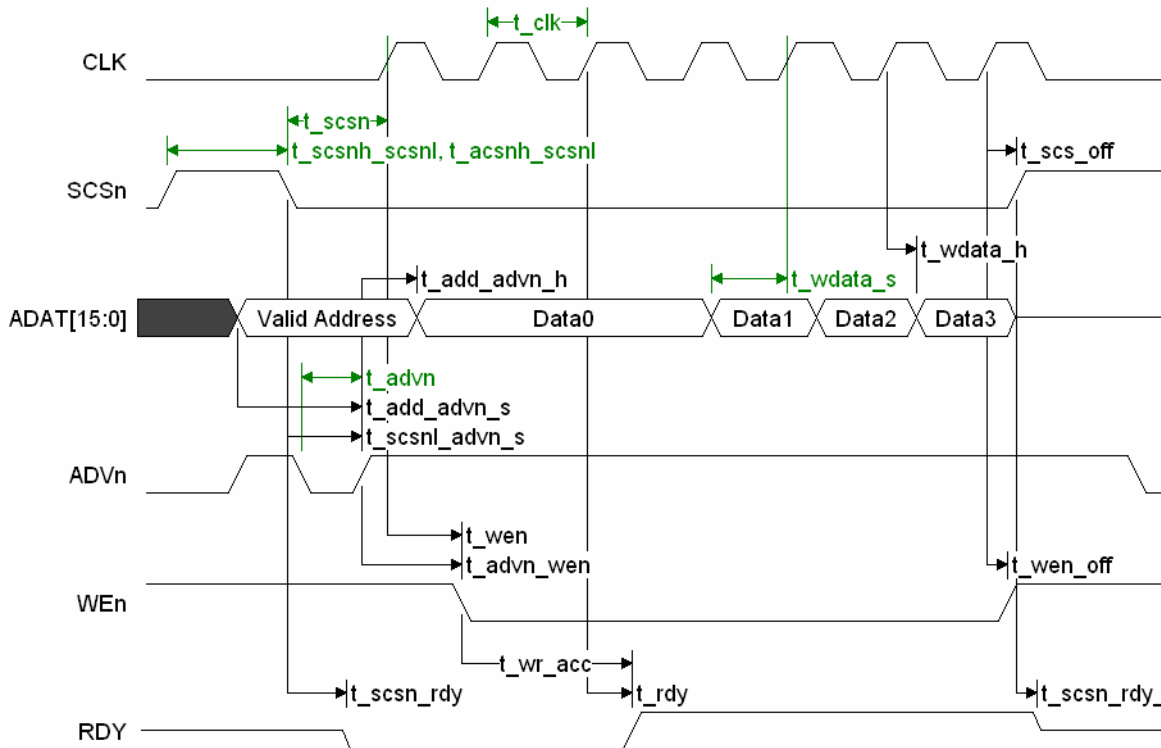
Notes: RDY going low is asynchronous to t_{scsn_rdy} . Going high, it is synchronous to CLK. Read Data output and RDY going high are synchronous to CLK. Valid Data Time programmable through Device Wait Count Register. Wait Count is not used for non-DMA synchronous reads.

PARAMETER		MIN	MAX	UNIT
t_{clk}	Cycle Time (max 67.5 MHz)	14.8		ns
t_{scsnh_scsnl}	Delay time, SCSn high to SCSn low	8		ns
t_{acsnh_scsnl}	Delay time, ACSn high to SCSn low	8		ns
t_{scsn}	Delay time, SCSn low to first rising edge of CLK	3ns	1+3ns	CLK
t_{scs_off}	CLK to SCSn high	4		ns
t_{rdata}	Read data output delay	2.2	9.2	ns
t_{rdy}	RDY output delay	2.2	8.2	Ns
t_{advn}	ADVn low pulse	7		Ns
t_{advn_oen}	ADVn high to OEn low	3		Ns
t_{oen_off}	CLK to OEn high	4		Ns
t_{oen}	OEn setup to CLK high	3.75		Ns
	OEn hold time	0		
t_{rd_acc}	Valid Data Time (with DMAREQ)	1 ¹	32 ²	CLK
$t_{add_advn_h}$	Addr Hold time to ADVn high	0.8		Ns
$t_{scsnl_advn_s}$	SCSn low Setup to ADVn high	12		Ns
$t_{add_advn_s}$	Address Setup to ADVn high	12		Ns
t_{scsn_rdy}	SCSn low to RDY valid low		7	ns
$t_{scsn_rdy_z}$	SCSn high to RDY high-Z		7	ns
$t_{oen_data_z}$	OEn high to Data high-Z		8	ns

¹Device Wait Count Register = 0 or 1.

²Device Wait Count Register = 31.

Synchronous Burst Write Access



Note: RDY going low is asynchronous to t_{scsn_rdy} . Going high, it is synchronous to CLK. Valid Data Time programmable through Device Wait Count Register. For Wait Count values other than 0 or 1 (when DMAREQ is used), t_{wr_acc} = Wait Count + 1.

PARAMETER		MIN	MAX	UNIT
t_{clk}	Cycle Time (max 67.5 MHz)	14.8		ns
t_{scsnh_scsnl}	Delay time, SCSn high to SCSn low	8		ns
t_{acsnh_scsnl}	Delay time, ACSn high to SCSn low	8		ns
t_{scsn}	Delay time, SCSn low to first rising edge of CLK	3ns	1+3ns	CLK
t_{scs_off}	CLK to SCSn high	1+3ns		Sys Clk
t_{wdata_s}	Data setup to CLK high	3.75		ns
t_{wdata_h}	Data hold time	0.6		ns
t_{rdy}	CLK to RDY output delay	2.2	8.2	ns
$t_{add_advn_h}$	Address Hold	0.8		ns
$t_{scsnl_advn_s}$	SCSn low Setup to ADVn high	12		ns
$t_{add_advn_s}$	Address Setup to ADVn high	12		ns
t_{advn}	ADVn low pulse	7		ns
t_{advn_wen}	ADVn high to WEn low	1+3ns		CLK
t_{wen_off}	CLK to WEn high	1+3ns		Sys Clk
t_{wen}	WEn setup to CLK high	3.75		ns
	WEn hold time	0		
t_{wr_acc}	Valid Data Time (with DMAREQ)	1 ¹	32 ²	CLK
t_{scsn_rdy}	SCSn low to RDY valid low		7	ns
$t_{scsn_rdy_z}$	SCSn high to RDY high-Z		7	ns

¹Device Wait Count Register = 0 or 1.

²Device Wait Count Register = 31.

Pin Descriptions

TERMINAL		TYPE	I/O	RESET STATE	DESCRIPTION
NAME	BALL				
VDD15	A1	Supply	-	-	Digital core power supply, 1.5 V
VSS	A2	Supply	-	-	Ground
CLK_24_SEL	A3	LVC MOS Failsafe ¹	I	In with Pull-up	CLKIN_19_2_24 Frequency Select at Reset CLK 24 SEL = HIGH, 19.2 MHz CLK 24 SEL = LOW, RSVD If GPIO6 is low at reset, this pin will have no effect on clock selection.
CLKIN_38_4	A4	LVC MOS Failsafe ¹	I	In	System Clock In. Connect directly to ground if not used.
CLKIN_19_2_24	A5	LVC MOS Failsafe ¹	I	In	System Clock In. Connect directly to ground if not used.
VSS	A6	Supply	-	-	Ground
VDD18	A7	Supply	-	-	IO Power Supply, 1.8 V
OEn	A8	LVC MOS Failsafe ¹	I	In with Pull-up	Output Enable
VDD15	A9	Supply	-	-	Digital core power supply, 1.5 V
VSSREF	B1	Supply	-	-	Ground reference for the reference circuits
GPIO7	B2	LVC MOS Failsafe ¹	I/O	In with Pull-up	GPIO 7
VDD15	B3	Supply	-	-	Digital core power supply, 1.5 V
VSS	B4	Supply	-	-	Ground
VDD18	B5	Supply	-	-	IO Power Supply, 1.8 V
GPIO2_DMAREQ2	B6	LVC MOS Failsafe ¹	I/O	In with Pull-up	GPIO 2 / DMA Request 2
ADAT15	B7	LVC MOS	I/O	In with Pull-up	Multiplexed ADDRESS.15/DATA.14
ADAT16	B8	LVC MOS	I/O	In with Pull-up	Multiplexed ADDRESS.16/DATA.15
VSS	B9	Supply	-	-	Ground
VDDA3P3	C1	Supply	-	-	3.3V Analog Supply
R1	C2	Bias	I	-	High precision external resistor used for calibration. (R1 value: 10.7 K +/- 1%)
GPIO4_DMAREQ4	C4	LVC MOS Failsafe ¹	I/O	In with Pull-up	GPIO 4 / DMA Request 4
VDD15	C5	Supply	-	-	Digital core power supply, 1.5 V
ADVn	C6	LVC MOS Failsafe ¹	I	In with Pull-up	Address Valid
ADAT12	C7	LVC MOS Failsafe ¹	I/O	In with Pull-up	Multiplexed ADDRESS.12/DATA.11
ADAT14	C8	LVC MOS Failsafe ¹	I/O	In with Pull-up	Multiplexed ADDRESS.14/DATA.13

TUSB6015ZQE

SLLS937
REVISION 1.4 SEPTEMBER 12, 2008

CLK	C9	LVC MOS Failsafe ¹	I	In with Pull-up	NOR Interface Clock
DP	D1	USB	I/O	-	USB Differential Pair
VDDCM1P5	D2	Supply	-	-	1.5V PLL Supply
VSSCM1P5	D3	Supply	-	-	1.5V PLL Ground
TEST	D4	LVC MOS	I	-	Test Mode. Under normal operation this signal should be tied directly to GND.
GPIO1	D5	LVC MOS Failsafe ¹	I/O	In with Pull-up	GPIO 1
WE _n	D6	LVC MOS Failsafe ¹	I	In with Pull-up	Write Enable
ADAT13	D7	LVC MOS Failsafe ¹	I/O	In with Pull-up	Multiplexed ADDRESS.13/DATA.12
ADAT11	D8	LVC MOS Failsafe ¹	I/O	In with Pull-up	Multiplexed ADDRESS.11/DATA.10
VDD15	D9	Supply	-	-	Digital core power supply, 1.5 V
VSSA1P5	E1	Supply	-	-	1.5V Analog Ground
DM	E2	USB	I/O	-	USB Differential Pair
VDDA1P5	E3	Supply	-	-	1.5V Analog Supply
VSSA3P3	E4	Supply	-	-	3.3V Analog Ground
VSS	E5	Supply	-	-	Ground
ADAT2	E6	LVC MOS Failsafe ¹	I/O	In with Pull-up	Multiplexed ADDRESS.2/DATA.1
GPIO5_DMAREQ5	E7	LVC MOS Failsafe ¹	I/O	In with Pull-up	GPIO 5 / DMA Request 5
GPIO3_DMAREQ3	E8	LVC MOS Failsafe ¹	I/O	In with Pull-up	GPIO 3 / DMA Request 3
VSS	E9	Supply	-	-	Ground
VDDD1P5	F1	Supply	-	-	1.5V Digital Supply
ID	F2	USB	I	-	Should be left floating as a USB device.
VBUS	F3	USB	I	-	USB VBUS
VSSD1P5	F4	Supply	-	-	1.5V Digital Ground
GPIO6	F5	LVC MOS Failsafe ¹	I/O	In with Pull-up	GPIO 6 / Input Clock Source Select at reset. GPIO6 = HIGH, 19.2/24 MHz GPIO6 = LOW, 38.4 MHz
ADAT1	F6	LVC MOS Failsafe ¹	I/O	In with Pull-up	Multiplexed ADDRESS.1/DATA.0
ADAT10	F7	LVC MOS Failsafe ¹	I/O	In with Pull-up	Multiplexed ADDRESS.10/DATA.9
ADAT9	F8	LVC MOS Failsafe ¹	I/O	In with Pull-up	Multiplexed ADDRESS.9/DATA.8
VDD15	F9	Supply	-	In with Pull-up	Digital core power supply, 1.5 V
VSS	G1	Supply	-	-	Ground
1.5V_SWEN	G2	LVC MOS	O	0	Switch Enable for 1.5V supply for Vbat/Vbus

		Failsafe ¹			Switch, if applicable
3.3V_SWEN	G3	LVC MOS Failsafe ¹	O	0	Switch Enable for 3.3V supply for Vbat/Vbus Switch, if applicable
ACSn	G4	LVC MOS Failsafe ¹	I	In with Pull-up	Asynchronous Chip Select
ADAT3	G5	LVC MOS Failsafe ¹	I/O	In with Pull-up	Multiplexed ADDRESS.3/DATA.2
ADAT4	G6	LVC MOS Failsafe ¹	I/O	In with Pull-up	Multiplexed ADDRESS.4/DATA.3
RDY	G7	LVC MOS tri-state	O	high z	Ready
SCSn	G8	LVC MOS	I	In with Pull-up	Synchronous Chip Select
VSS	G9	Supply	-	-	Ground
RSTn	H1	LVC MOS Failsafe ¹	I	In with Pull-up	Reset Active Low
CPEN	H2	LVC MOS Failsafe ¹	O	0	5V Charge Pump Enable, if applicable
SLEEP	H3	LVC MOS Failsafe ¹	O	0	Use for external power supply low power mode when idle, if applicable
GPIO0	H4	LVC MOS Failsafe ¹	I/O	In with Pull-up	GPIO 0
ADAT5	H5	LVC MOS Failsafe ¹	I/O	In with Pull-up	Multiplexed ADDRESS.5/DATA.4
ADAT6	H6	LVC MOS Failsafe ¹	I/O	In with Pull-up	Multiplexed ADDRESS.6/DATA.5
ADAT7	H7	LVC MOS Failsafe ¹	I/O	In with Pull-up	Multiplexed ADDRESS.7/DATA.6
ADAT8	H8	LVC MOS Failsafe ¹	I/O	In with Pull-up	Multiplexed ADDRESS.8/DATA.7
VDD18	H9	Supply	-	-	IO Power Supply, 1.8 V
VDD18	J1	Supply	-	-	IO Power Supply, 1.8 V
VSS	J2	Supply	-	-	Ground
VDD15	J3	Supply	-	-	Digital core power supply, 1.5 V
VSS	J4	Supply	-	-	Ground
DMAREQ1	J5	LVC MOS Failsafe ¹	O	1	DMA Request 1
VDD18	J6	Supply	-	-	IO Power Supply, 1.8 V
DMAREQ0	J7	LVC MOS Failsafe ¹	O	1	DMA Request 0
VSS	J8	Supply	-	-	Ground
INT	J9	LVC MOS Failsafe ¹	O	1	Interrupt

¹Failsafe means that the signal can toggle when VDD18 is not present without damaging the device.

External Components

USB PHY Voltage and Current Bias Resistor Pin: R1

This signal must connect to a precision external resistance to set the internal operating reference currents and cable driver output currents. A resistance of $10.7\text{ k}\Omega \pm 1\%$ (temperature coefficient $\pm 100\text{ppm}/^\circ\text{C}$) is necessary to meet requirements set forth in the Universal Serial Bus Revision 2.0 specification.

The side of the resistor not connected to the R1 signal should connect through a low impedance path to the circuit board ground plane.

USB PHY Voltage and Current Reference Ground: VSSREF

This signal is the reference ground for the voltage and current reference circuitry internal to the Data/Port macro. This signal must connect to the low impedance circuit board ground plane.

USB PHY Power Connections: VDDCM1P5, VDDA1P5, VDDD1P5, VDDA3P3

Decoupling capacitors are required to suppress high-frequency switching noise and stabilize the supply voltage. A decoupling capacitor is most effective when it is close to the chip. This minimizes the inductance of the circuit board wiring and interconnects.

The USB 2.0 PHY Macro has two power rails, 1.5V (VDDCM1P5, VDDD1P5, VDDA1P5) and 3.3V (VDDA3P3). Each power connection has its own associated ground connection, 1.5V (VSSCM1P5, VSSD1P5, VSSA1P5) and 3.3V (VSSA3P3). Each supply is isolated from the others to provide noise isolation.

A combination of high-frequency capacitors near each terminal is suggested, such as paralleled 1 μF , 0.01 μF , and 0.001 μF capacitors. A lower frequency 10 μF filter capacitor is also recommended. A series inductor on the analog supplies is also recommended. All ground pins must connect through a low impedance path to the circuit board ground plane. All grounds can be connected to each other.

- VDDCM1P5 (Common Module 1.5V Supply) - (1) 1 μf , (1) 0.1 μf , 0.01 μf , (1) 0.001 μf , (1) 10 μf
- VSSCM1P5 (Common Module Ground)
- VDDD1P5 (Digital 1.5V Supply) - (1) 0.1 μf , (1) 0.001 μf , (1) 10 μf
- VSSD1P5 (Digital 1.5V Ground)
- VDDA1P5 (Analog 1.5V Supply) - (1) 0.1 μf , (1) 0.001 μf , (1) 10 μf , with a series inductor between the main supply and the device, the caps between the inductor and the device.
- VSSA1P5 (Analog 1.5V Ground)
- VDDA3P3 (Analog 3.3V Supply) - (1) 0.1 μf , (1) 0.001 μf , (1) 10 μf , with a series inductor between the main supply and the device, the caps between the inductor and the device.
- VDDA3P3 (Analog 3.3V Ground)

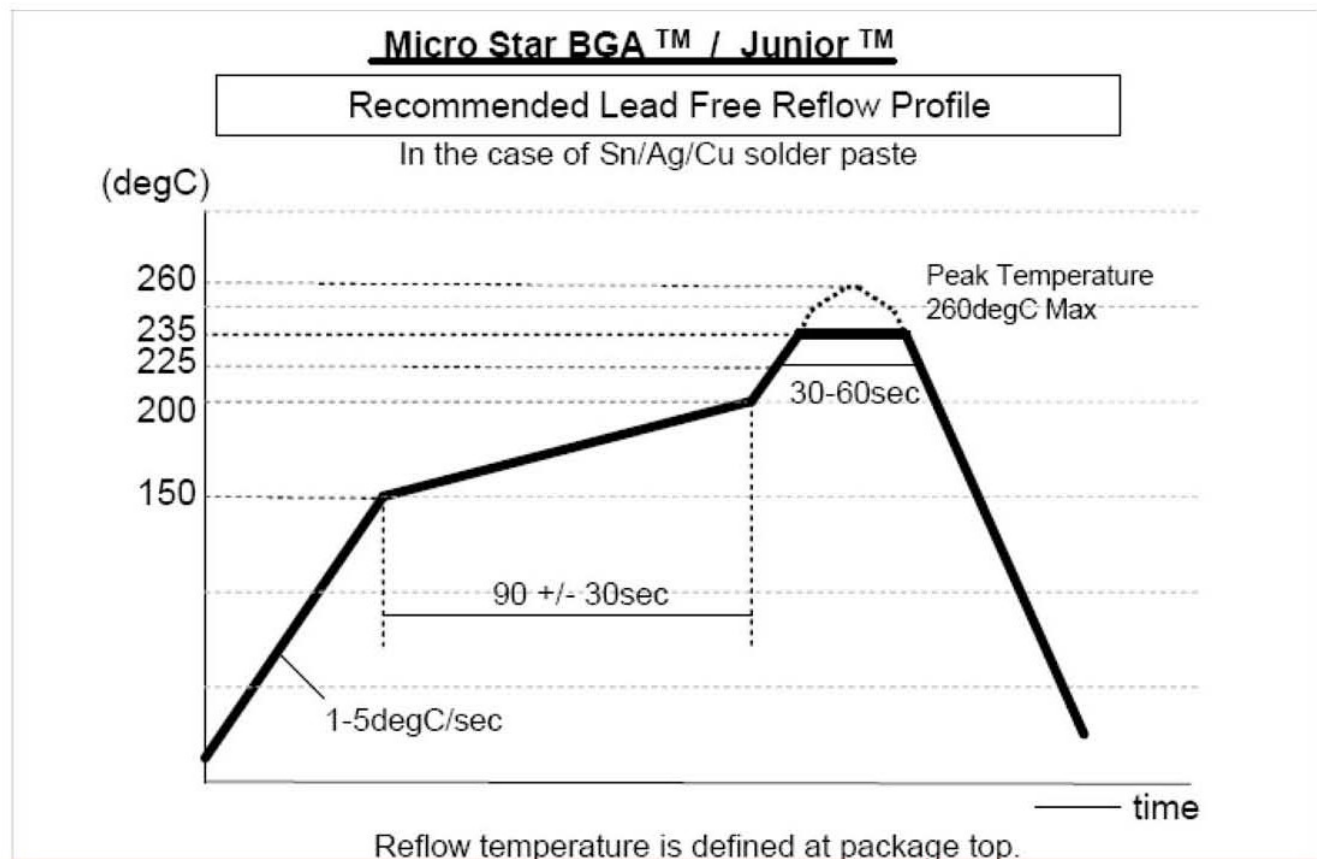
Digital Power Connections: VDD18, VDD15

The digital portion of the TUSB6015 has two power rails, 1.5V (VDD15) and 1.8V (VDD18). There is one digital ground connection (VSS). Each supply is isolated from the others to provide noise isolation.

A combination of high-frequency capacitors near each terminal is suggested, such as paralleled 0.01uF and 0.001uF capacitors. A lower frequency 10uF filter capacitor is also recommended. All ground pins must connect through a low impedance path to the circuit board ground plane. All grounds can be connected to each other.

- VDD15 (Digital Core Voltage 1.5V Supply) - (5) 0.1μf, (5) 0.001μf, (1) 10μf
- VDD18 (Digital IO Voltage 1.8V Supply) - (5) 0.1μf, (5) 0.001μf, (1) 10μf
- VSS (Digital Ground)

Reflow Conditions



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TUSB6015IZQE	NRND	BGA MI CROSTA R JUNI OR	ZQE	80	360	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
TUSB6015IZQER	NRND	BGA MI CROSTA R JUNI OR	ZQE	80	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

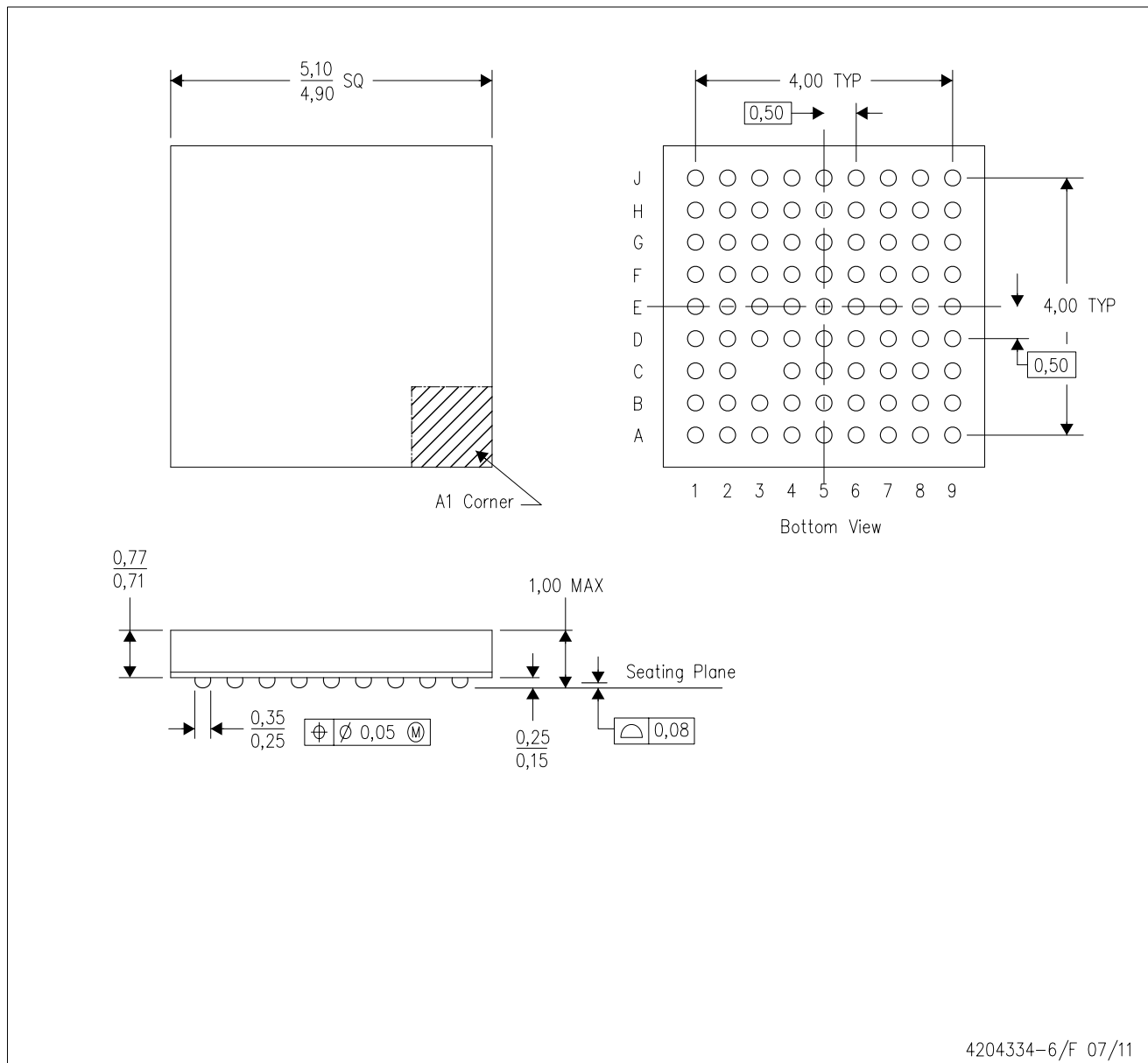
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MECHANICAL DATA

ZQE (S-PBGA-N80)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225
 - D. This is a Pb-free solder ball design.

MicroStar Junior is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated