Precision Low-Voltage, Low-Glitch CMOS Analog Switches

DESCRIPTION

Using BiCMOS wafer fabrication technology allows the DG9421, DG9422 to operate on single and dual supplies.

Designed for optimal performance at single 5 V and dual ± 5 V, the DG9421, DG9422 combine low and flat on-resistance (3 Ω), fast speed (t_{ON} = 38 ns) and is well suited for applications where signal switching accuracy, low noise and low distortion is critical.

The DG9421 and DG9422 respond to opposite control logic as shown in the Truth Table.

FEATURES

- 2.7 V thru 12 V single supply or ± 2.7 V thru ± 6 V dual supply
- Low on-resistance - $R_{DS(on)}$: 2 Ω at 12 V
- Fast switching - t_{ON}: 22 ns
  - t_{OFF}: 28 ns
- TTL and low voltage logic
- Low leakage: 10 pA (typ.)
- > 2000 V ESD protection
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free Available
RoHS* Available
HALOGEN FREE

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

BENEFITS

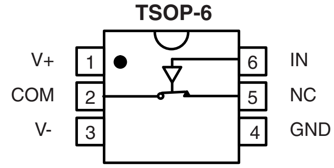
- High accuracy
- High speed, low glitch
- Single and dual supply capability
- Low R_{ON} in small TSOP package
- Low leakage
- Low power consumption

APPLICATIONS

- Automatic test equipment
- Data acquisition
- XDSL and DSLAM
- PBX systems
- Reed relay replacement
- Audio and video signal routing

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

TSOP-6

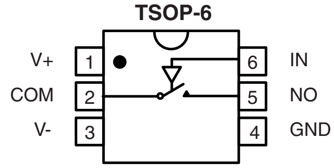


Top View

Device Marking:

DG9421DV = 4Exxx

TSOP-6



Top View

Device Marking:

DG9422DV = 4Fxxx

TRUTH TABLE		
LOGIC	**DG9421**	**DG9422**
0	ON	OFF
1	OFF	ON

Notes

- Logic "0" ≤ 0.8 V
- Logic "1" ≥ 2.4 V
- Switches shown for logic "0" input

ORDERING INFORMATION		
TEMP. RANGE	**PACKAGE**	**PART NUMBER**
-40 °C to +85 °C	6 / Pin TSOP	DG9421DV-T1 DG9421DV-T1-E3
		DG9422DV-T1 DG9422DV-T1-E3

ABSOLUTE MAXIMUM RATINGS			
PARAMETER		LIMIT	UNIT
V+ to V-		-0.3 to +13	V
GND to V-		7	
V_{IN} [a], V_S, V_D		-0.3 to (V+ + 0.3) or 50 mA, whichever occurs first	V/mA
Continuous Current (any terminal)		50	mA
Peak Current, S or D (pulsed at 1 ms, 10 % duty cycle)		100	
Storage Temperature		-65 to +150	°C
Power Dissipation (Packages) [b]	6-Pin TSOP [c]	570	mW

Notes

a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 7 mW/°C above 25 °C.

SPECIFICATIONS [a] (Single Supply 12 V)							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 12 V, V- = 0 V, V_{IN} = 2.4 V, 0.8 V [f]	TEMP. [b]	LIMITS -40 °C to +85°C MIN. [d]	TYP. [c]	MAX. [d]	UNIT
Analog Switch							
Analog Signal Range [a]	V_{ANALOG}		Full	0	-	12	V
Drain-Source On-Resistance	$R_{DS(on)}$	V+ = 10.8 V, V- = 0 V, I_S = 5 mA, V_D = 2 V/9 V	Room	-	2	3	Ω
			Full	-	2	3.4	
Switch Off Leakage Current	$I_{S(off)}$	V_D = 1/11 V, V_S = 11 V/1 V	Room	-1	-	1	nA
			Full	-10	-	10	
	$I_{D(off)}$		Room	-1	-	1	
			Full	-10	-	10	
Channel-On Leakage Current	$I_{D(on)}$	V_S = V_D = 11 V/1 V	Room	-1	-	1	
			Full	-10	-	10	
Digital Control							
Input Current, V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V	Full	-1	0.02	1	µA
Input Current, V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V	Full	-1	0.02	1	
Dynamic Characteristics							
Turn-On Time [e]	t_{ON}	R_L = 300 Ω, C_L = 35 pF, V_S = 5 V see figure 2	Room	-	20	45	ns
			Full	-	-	49	
Turn-Off Time [e]	t_{OFF}		Room	-	25	47	
			Full	-	-	59	
Charge Injection [e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Room	-	43	-	pC
Off-Isolation [e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-60	-	dB
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	Room	-	31	-	pF
Drain Off Capacitance [e]	$C_{D(off)}$		Room	-	30	-	
Channel On Capacitance [e]	$C_{D(on)}$		Room	-	71	-	
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 V or 12 V	Room	-	0.020	1	µA
			Full	-	-	5	
Negative Supply Current	I-		Room	-1	-0.002	-	
			Full	-5	-	-	
Ground Current	I_{GND}		Room	-1	-0.002	-	
			Full	-5	-	-	

SPECIFICATIONS [a] (Dual Supply ± 5 V)							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED $V+ = 5$ V, $V- = -5$ V, $V_{IN} = 2.4$ V, 0.8 V [f]	TEMP. [b]	LIMITS -40 °C to +85 °C MIN. [d]	TYP. [c]	MAX. [d]	UNIT
Analog Switch							
Analog Signal Range [e]	V_{ANALOG}		Full	-5	-	5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V+ = 5$ V, $V- = 5$ V, $I_S = 5$ mA, $V_D = \pm 3.5$ V	Room	-	2.2	3.2	Ω
			Full	-	-	3.6	
Switch Off Leakage Current [g]	$I_{S(off)}$	$V+ = 5.5$ V, $V- = 5.5$ V, $V_D = \pm 4.5$ V, $V_S = \mp 4.5$ V	Room	-1	-	1	nA
			Full	-10	-	10	
	$I_{D(off)}$		Room	-1	-	1	
			Full	-10	-	10	
Channel-On Leakage Current [g]	$I_{D(on)}$	$V+ = 5.5$ V, $V- = -5.5$ V, $V_S = V_D = \pm 4.5$ V	Room	-1	-	1	
			Full	-10	-	10	
Digital Control							
Input Current, V_{IN} Low [e]	I_{IL}	V_{IN} under test = 0.8 V	Full	-1	0.02	1	µA
Input Current, V_{IN} High [e]	I_{IH}	V_{IN} under test = 2.4 V	Full	-1	0.02	1	
Dynamic Characteristics							
Turn-On Time	t_{ON}	$R_L = 300\ \Omega$, $C_L = 35$ pF, $V_S = \pm 3.5$ V see figure 2	Room	-	38	63	ns
			Full	-	-	68	
Turn-Off Time	t_{OFF}		Room	-	45	83	
			Full	-	-	97	
Charge Injection [e]	Q	$V_g = 0$ V, $R_g = 0\ \Omega$, $C_L = 1$ nF	Room	-	207	-	pC
Off-Isolation [e]	OIRR	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz	Room	-	-57	-	dB
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	Room	-	32	-	pF
Drain Off Capacitance [e]	$C_{D(off)}$	f = 1 MHz	Room	-	31	-	pF
Channel On Capacitance [e]	$C_{D(on)}$	f = 1 MHz	Room	-	71	-	pF
Power Supplies							
Positive Supply Current [e]	I+	$V_{IN} = 0$ V or 5 V	Room	-	0.030	1	µA
			Full	-	-	5	
Negative Supply Current [e]	I-		Room	-1	-0.002	-	
			Full	-5	-	-	
Ground Current [e]	I_{GND}		Room	-1	-0.002	-	
			Full	-5	-	-	

SPECIFICATIONS [a] (Single Supply 5 V)							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED $V+ = 5$ V, $V- = 0$ V, $V_{IN} = 2.4$ V, 0.8 V [f]	TEMP. [b]	LIMITS -40 °C to +85 °C MIN. [d]	TYP. [c]	MAX. [d]	UNIT
Analog Switch							
Analog Signal Range [e]	V_{ANALOG}		Full	0	-	5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V+ = 4.5$ V, $I_S = 5$ mA, $V_D = 1$ V, 3.5 V	Room	-	3.6	6	Ω
			Full	-	-	6.6	
Dynamic Characteristics							
Turn-On Time [e]	t_{ON}	$R_L = 300\ \Omega$, $C_L = 35$ pF, $V_S = 3.5$ V, see figure 2	Room	-	43	67	ns
			Hot	-	-	74	
Turn-Off Time [e]	t_{OFF}		Room	-	30	67	
			Hot	-	-	80	
Charge Injection [e]	Q	$V_g = 0$ V, $R_g = 0\ \Omega$, $C_L = 1$ nF	Room	-	25	-	pC
Power Supplies							
Positive Supply Current [e]	I+	$V_{IN} = 0$ V or 5 V	Room	-	0.020	1	µA
			Hot	-	-	5	
Negative Supply Current [e]	I-		Room	-1	-0.002	-	
			Hot	-5	-	-	
Ground Current [e]	I_{GND}		Room	-1	-0.002	-	
			Hot	-5	-	-	

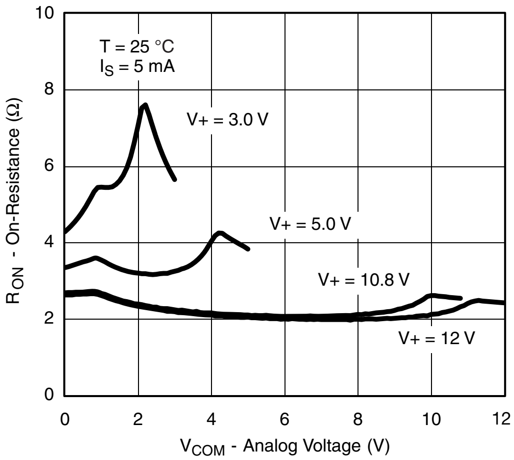
SPECIFICATIONS [a] (Single Supply 3 V)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** $V+ = 3$ V, $V- = 0$ V, $V_{IN} = 0.4$ V [f]	**TEMP.** [b]	**LIMITS** -40 °C to +85 °C			**UNIT**
				MIN. [d]	**TYP.** [c]	**MAX.** [d]	
Analog Switch							
Analog Signal Range [e]	V_{ANALOG}		Full	0	-	3	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V+ = 2.7$ V, $V- = 0$ V $I_S = 5$ mA, $V_D = 0.5$ V, 2.2 V	Room	-	7.3	8.8	Ω
			Full	-	-	10.1	
Switch Off Leakage Current [g]	$I_{S(off)}$	$V+ = 3.3$ V, $V- = 0$ V $V_S = 1, 2$ V, $V_D = 2$ V, 1 V	Room	-1	-	1	nA
			Full	-10	-	10	
	$I_{D(off)}$		Room	-1	-	1	
			Full	-10	-	10	
Channel-On Leakage Current [g]	$I_{D(on)}$	$V+ = 3.3$ V, $V- = 0$ V $V_D = V_S = 1$ V, 2 V	Room	-1	-	1	
			Full	-10	-	10	
Digital Control							
Input Current, V_{IN} Low [e]	I_{IL}	V_{IN} under test = 0.4 V	Full	-1	0.02	1	µA
Input Current, V_{IN} High [e]	I_{IH}	V_{IN} under test = 2.4 V	Full	-1	0.02	1	
Dynamic Characteristics							
Turn-On Time	t_{ON}	$R_L = 300\ \Omega$, $C_L = 35$ pF, $V_S = 1.5$ V see figure 2	Room		90	110	ns
			Full			125	
Turn-Off Time	t_{OFF}		Room		32	84	
			Full			99	
Charge Injection [e]	Q	$V_g = 0$ V, $R_g = 0\ \Omega$, $C_L = 1$ nF	Room		31		pC
Off-Isolation e	OIRR	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz	Room		-60		dB
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	Room		35		pF
Drain Off Capacitance [e]	$C_{D(off)}$		Room		34		
Channel On Capacitance [e]	$C_{D(on)}$		Room		77		

Notes

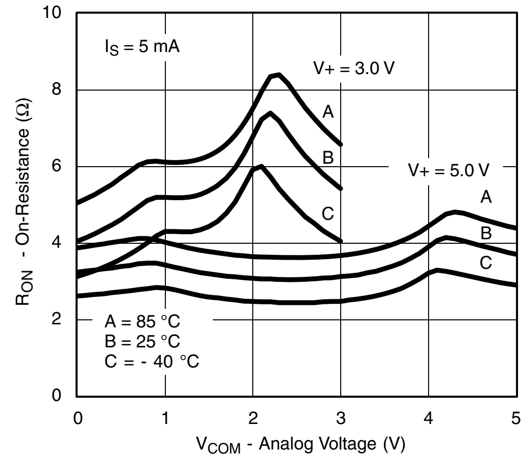
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. Leakage parameters are guaranteed by worst case test conditions and not subject to test.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

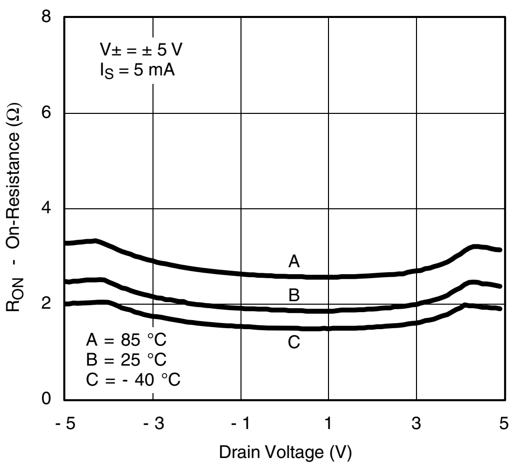
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



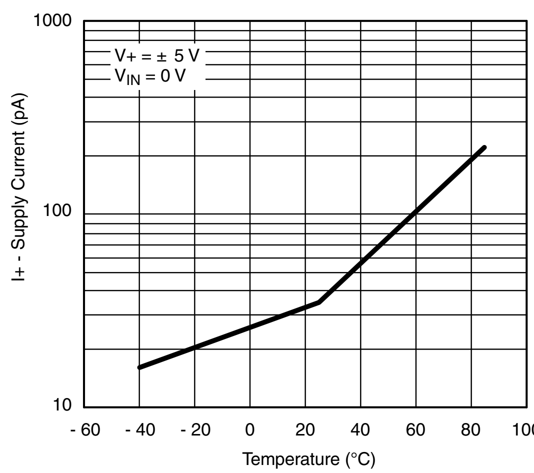
R_{ON} vs. V_{COM} and Supply Voltage



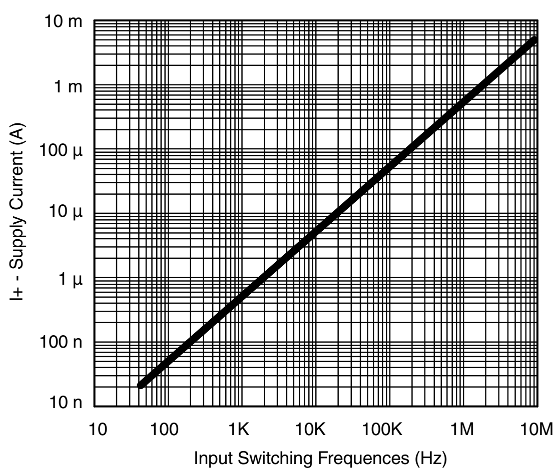
R_{ON} vs. Analog Voltage and Temperature



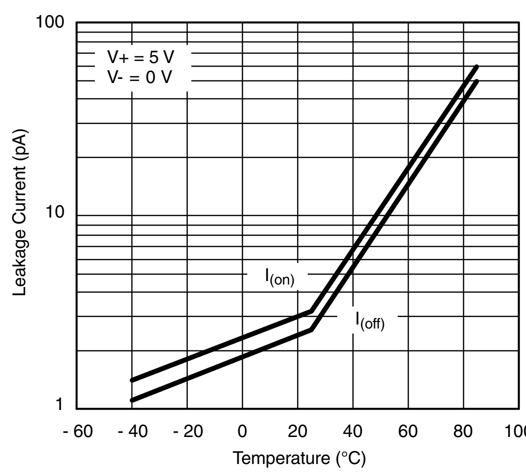
R_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Temperature

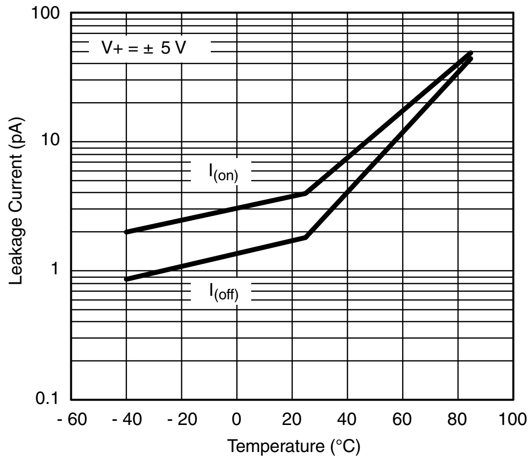


Supply Current vs. Input Switching Frequency

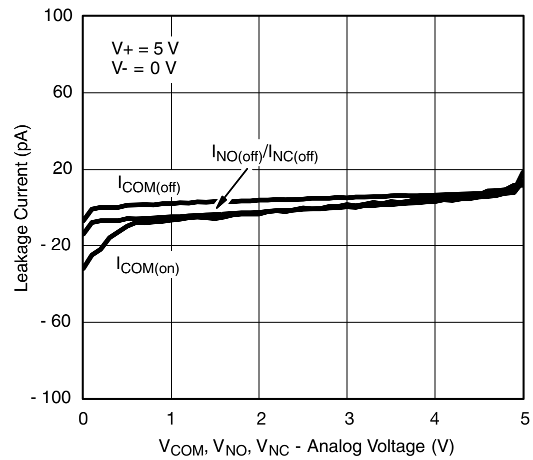


Leakage Current vs. Temperature

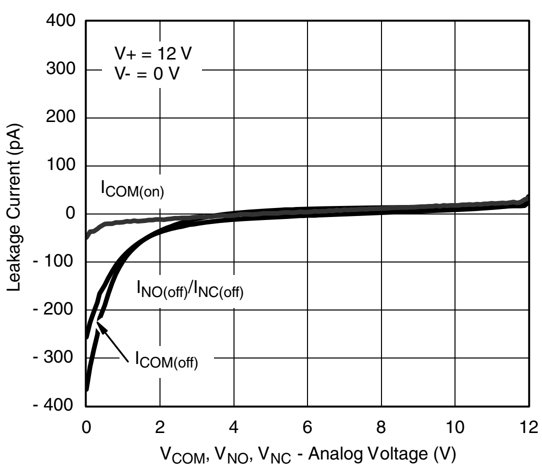
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



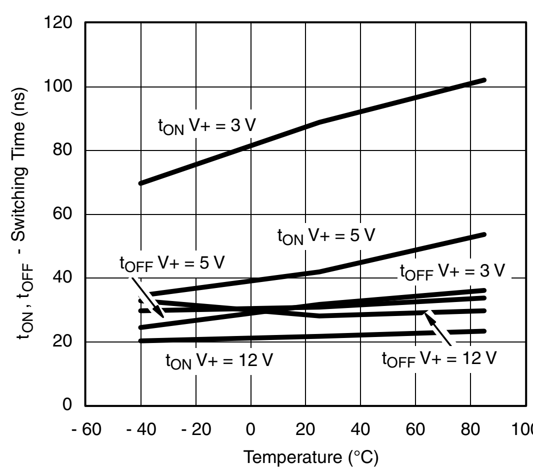
Leakage Current vs. Temperature



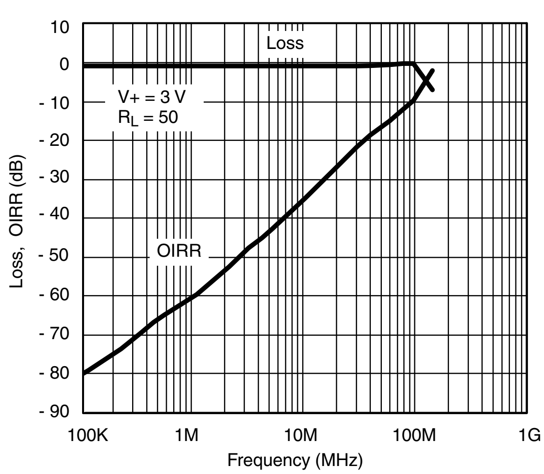
Leakage vs. Analog Voltage



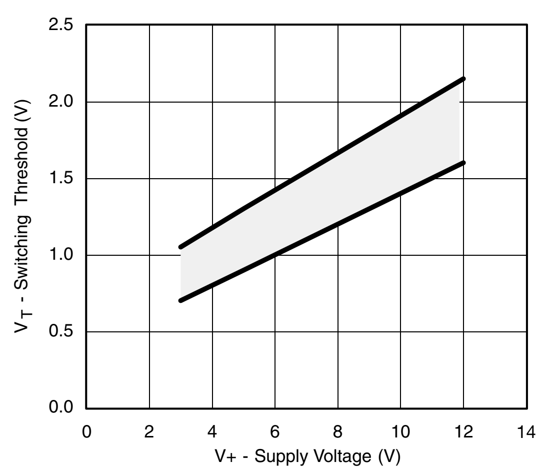
Leakage vs. Analog Voltage



Switching Time vs. Temperature and Supply Voltage (DG9421)



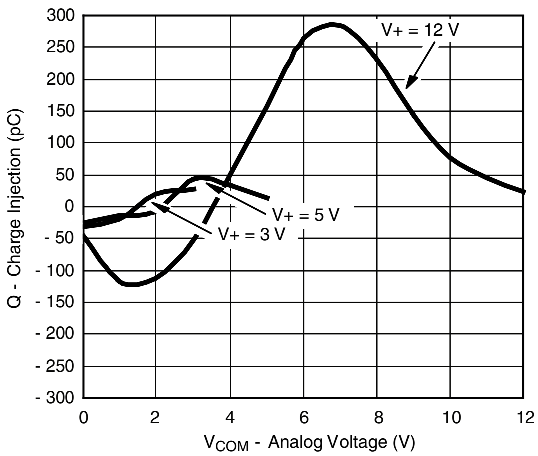
Insertion Loss, Off Isolation vs. Frequency



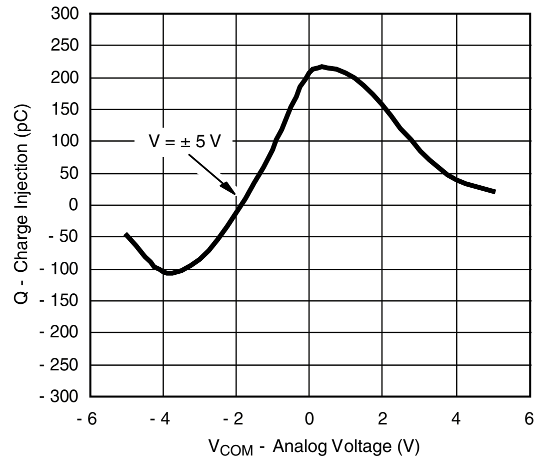
Switching Threshold vs. Supply Voltage

For technical questions, contact: powerictechsupport@vishay.com

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Charge Injection vs. Analog Voltage



Charge Injection vs. Analog Voltage

SCHEMATIC DIAGRAM (Typical Channel)

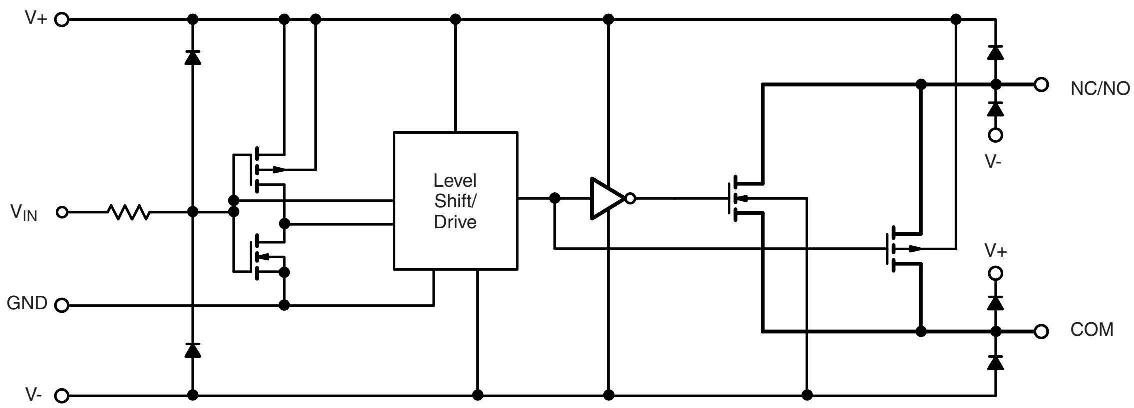
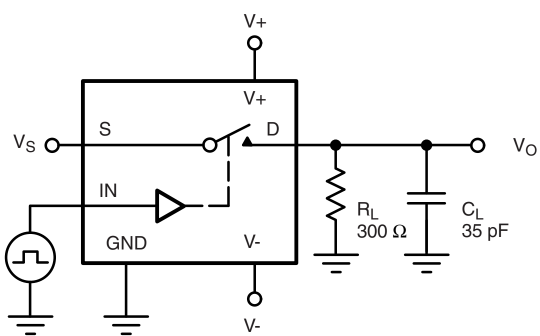


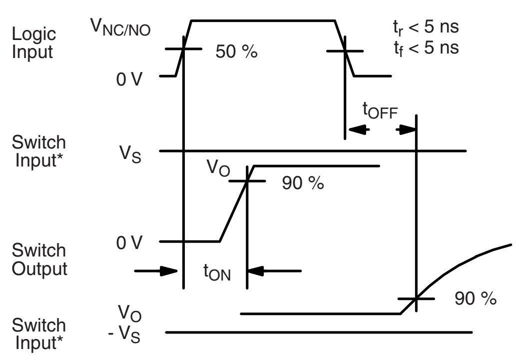
Fig. 1

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



Note: * Logic input waveform is inverted for switches that have the opposite logic sense control

Fig. 2 - Switching Time

TEST CIRCUITS

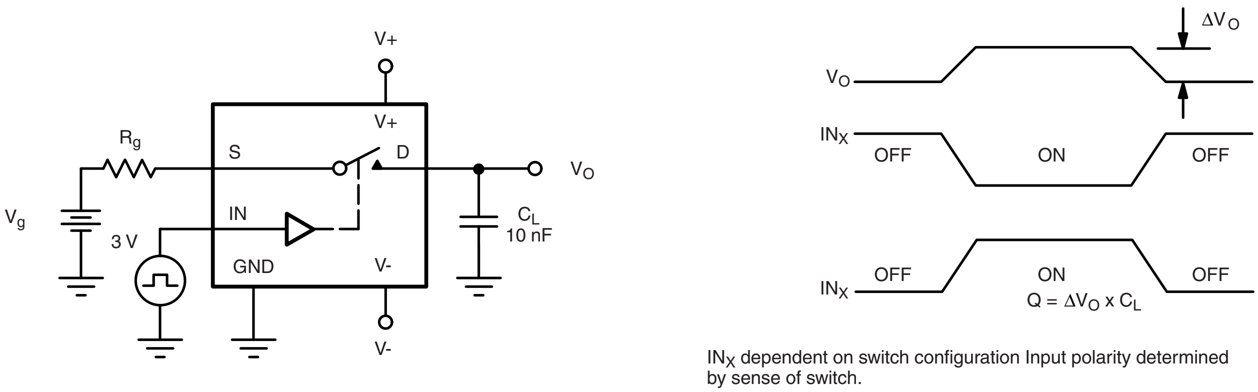


Fig. 3 - Charge Injection

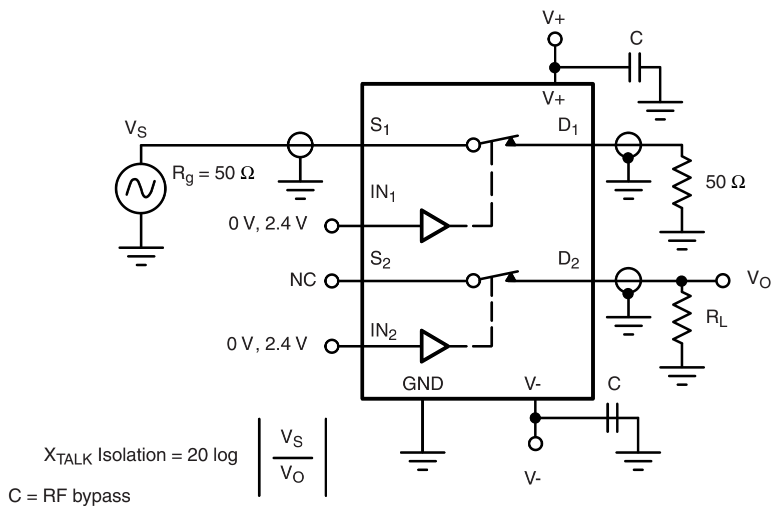


Fig. 4 - Crosstalk

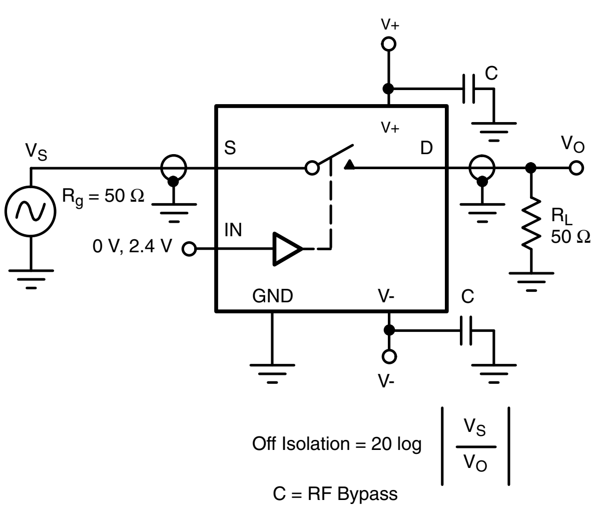


Fig. 5 - Off Isolation

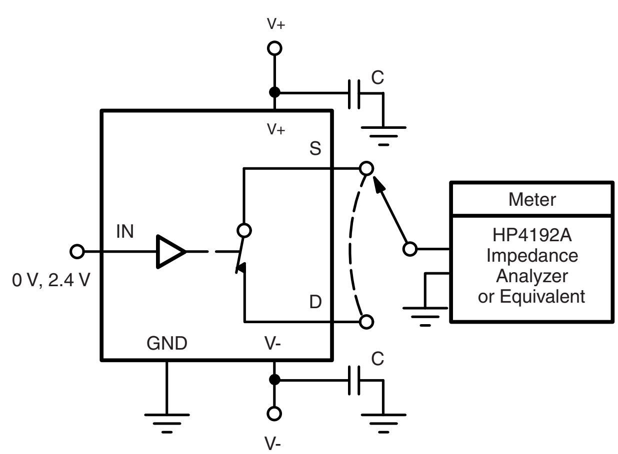
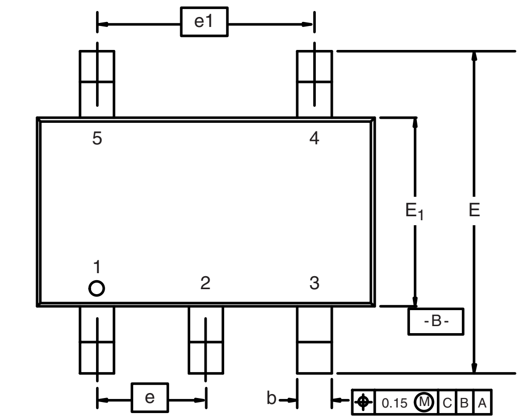


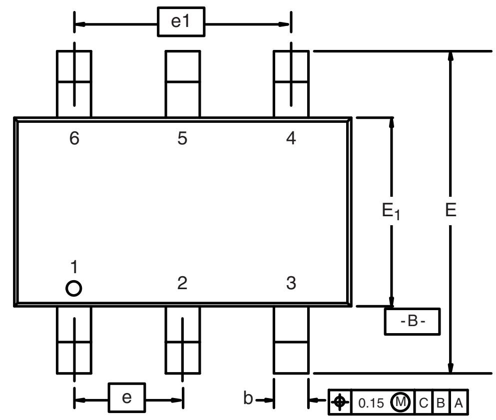
Fig. 6 - ource/Drain Capacitances

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70679.

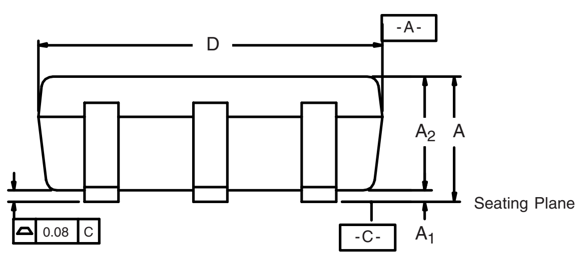
TSOP: 5/6–LEAD
JEDEC Part Number: MO-193C

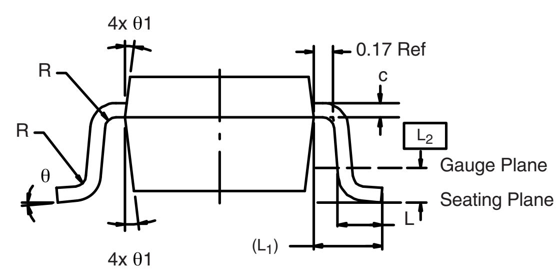


5-LEAD TSOP



6-LEAD TSOP





	MILLIMETERS			INCHES		
Dim	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	0.91	-	1.10	0.036	-	0.043
A_1	0.01	-	0.10	0.0004	-	0.004
A_2	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e_1	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L_1	0.60 Ref			0.024 Ref		
L_2	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ_1	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540						

Mounting LITTLE FOOT® TSOP-6 Power MOSFETs

Surface mounted power MOSFET packaging has been based on integrated circuit and small signal packages. Those packages have been modified to provide the improvements in heat transfer required by power MOSFETs. Leadframe materials and design, molding compounds, and die attach materials have been changed. What has remained the same is the footprint of the packages.

The basis of the pad design for surface mounted power MOSFET is the basic footprint for the package. For the TSOP-6 package outline drawing see http://www.vishay.com/doc?71200 and see http://www.vishay.com/doc?72610 for the minimum pad footprint. In converting the footprint to the pad set for a power MOSFET, you must remember that not only do you want to make electrical connection to the package, but you must made thermal connection and provide a means to draw heat from the package, and move it away from the package.

In the case of the TSOP-6 package, the electrical connections are very simple. Pins 1, 2, 5, and 6 are the drain of the MOSFET and are connected together. For a small signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

Figure 1 shows the copper spreading recommended footprint for the TSOP-6 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlays the basic pattern on pins 1,2,5, and 6. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. Notice that the planar copper is shaped like a "T" to move heat away from the drain leads in all directions. This pattern uses all the available area underneath the body for this purpose.

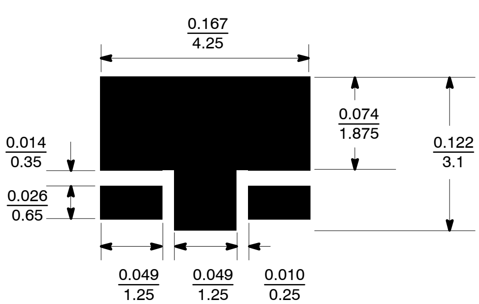


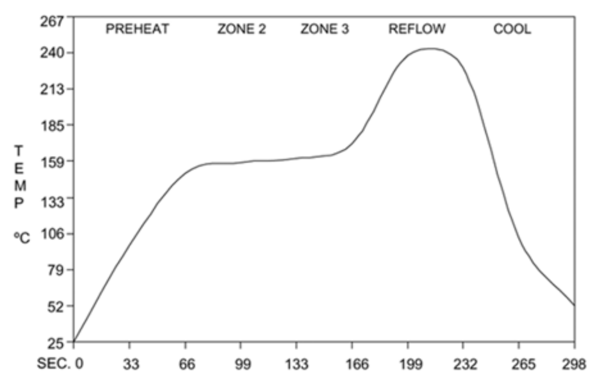
FIGURE 1. Recommended Copper Spreading Footprint

Since surface mounted packages are small, and reflow soldering is the most common form of soldering for surface mount components, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

REFLOW SOLDERING

Vishay Siliconix surface-mount packages meet solder reflow reliability requirements. Devices are subjected to solder reflow as a test preconditioning and are then reliability-tested using temperature cycle, bias humidity, HAST, or pressure pot. The solder reflow temperature profile used, and the temperatures and time duration, are shown in Figures 2 and 3.



Ramp-Up Rate	+6°C/Second Maximum
Temperature @ 155 ± 15°C	120 Seconds Maximum
Temperature Above 180°C	70 – 180 Seconds
Maximum Temperature	240 +5/–0°C
Time at Maximum Temperature	20 – 40 Seconds
Ramp-Down Rate	+6°C/Second Maximum

FIGURE 2. Solder Reflow Temperature Profile

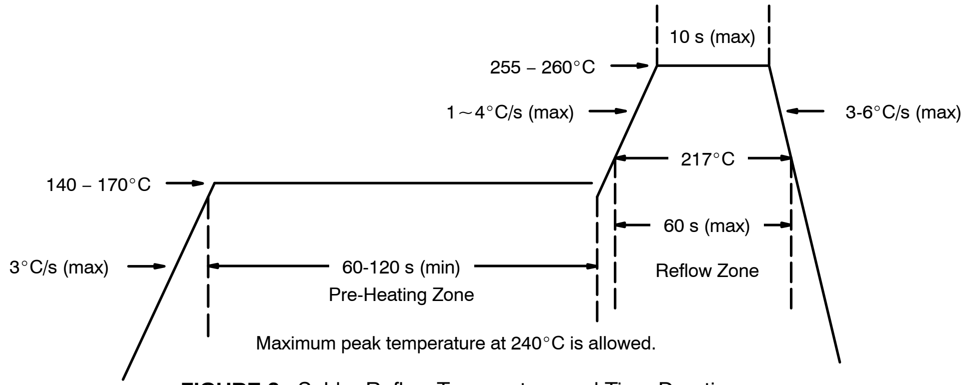


FIGURE 3. Solder Reflow Temperature and Time Durations

THERMAL PERFORMANCE

A basic measure of a device's thermal performance is the junction-to-case thermal resistance, $R\theta_{jc}$, or the junction-to-foot thermal resistance, $R\theta_{jf}$. This parameter is measured for the device mounted to an infinite heat sink and is therefore a characterization of the device only, in other words, independent of the properties of the object to which the device is mounted. Table 1 shows the thermal performance of the TSOP-6.

TABLE 1.	
Equivalent Steady State Performance—TSOP-6	
Thermal Resistance $R\theta_{jf}$	30°C/W

SYSTEM AND ELECTRICAL IMPACT OF TSOP-6

In any design, one must take into account the change in MOSFET $r_{DS(on)}$ with temperature (Figure 4).

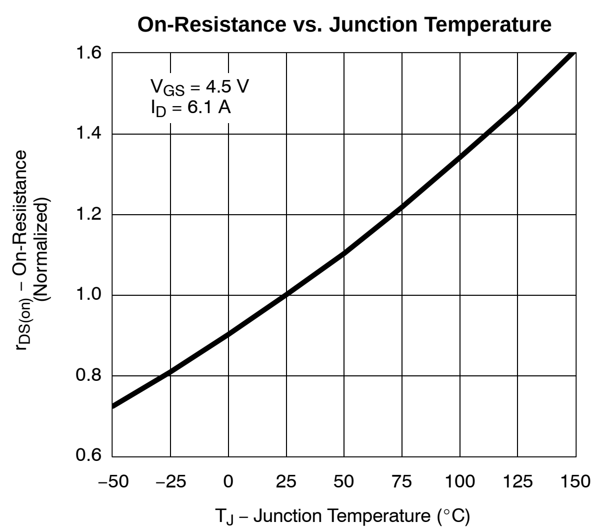
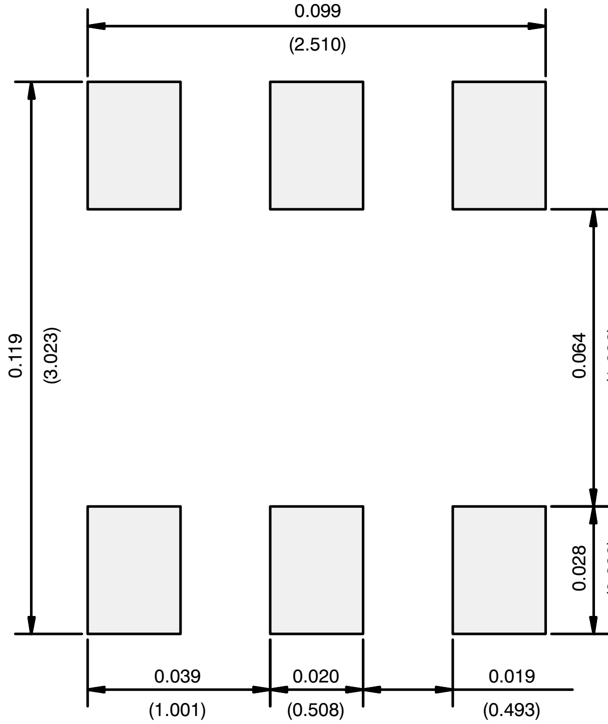


FIGURE 4. Si3434DV

RECOMMENDED MINIMUM PADS FOR TSOP-6



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay’s knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer’s responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer’s technical experts. Product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.