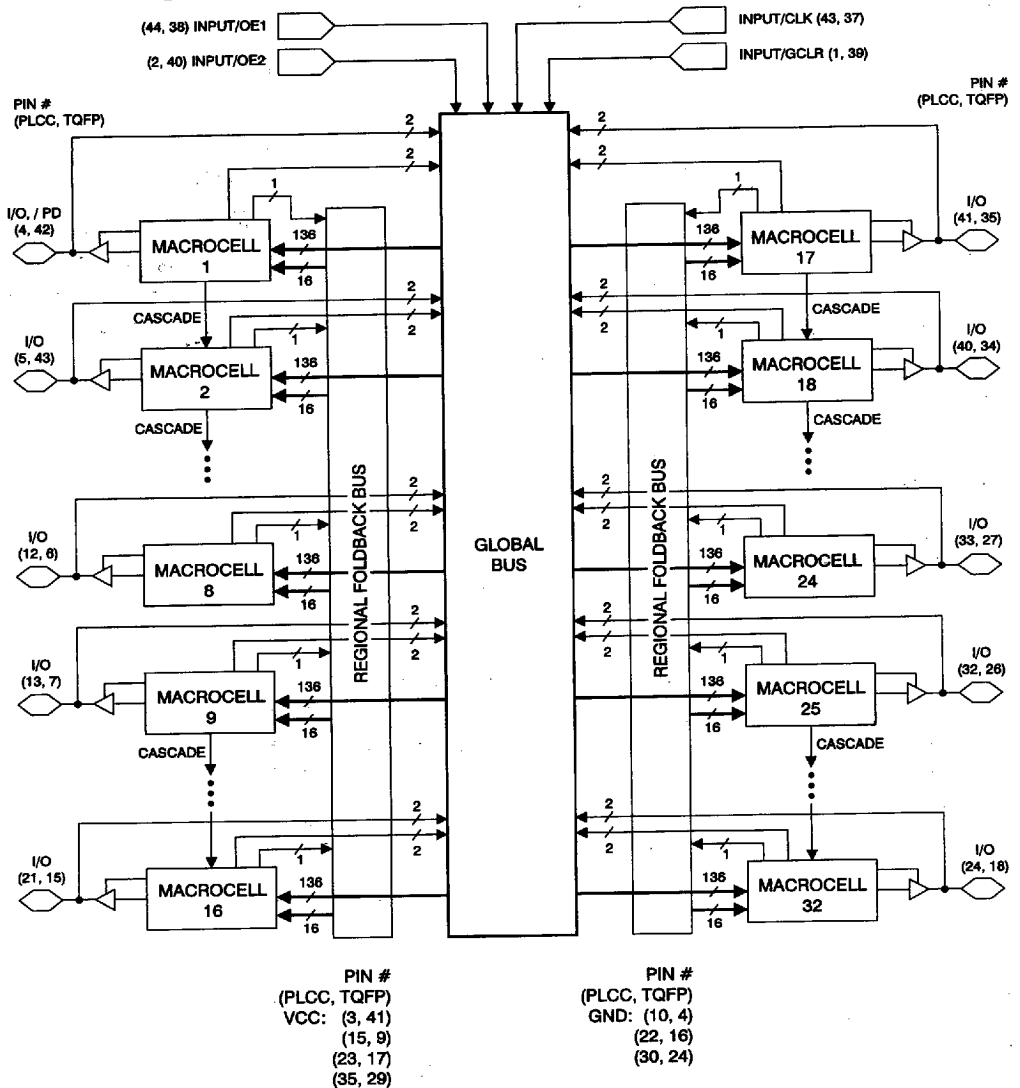




# Functional Logic Diagram<sup>(1)</sup>



Note: 1. Arrows connecting macrocells indicate direction and groupings of CASIN/CASOUT data flow.

## Description (Continued)

Each of the 32 logic macrocells generates a buried feedback, which goes to the global bus. Each input and I/O pin also feeds into the global bus. Because of this global bussing, each of these signals is always available to all 32 macrocells in the device.

Each macrocell also generates a foldback logic term, which goes to a regional bus. All signals within a regional bus are connected to all 16 macrocells within the region.

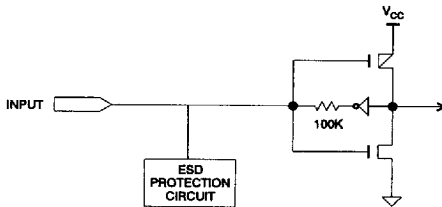
Cascade logic between macrocells in the ATF1500 allows fast, efficient generation of complex logic functions. The ATF1500 contains 4 such logic chains, each capable of creating sum term logic with a fan in of up to 40 product terms.

## Bus Friendly Pin-Keeper Input and I/O's

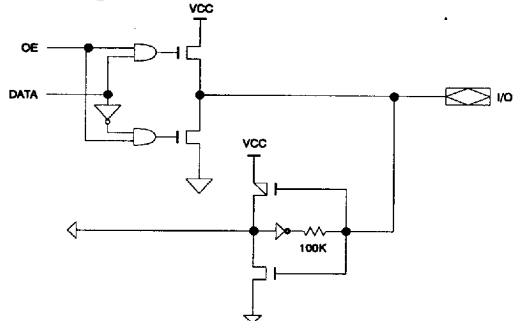
All Input and I/O pins on the ATF1500 have bus friendly "data keeper" circuits. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level.

This circuitry prevents unused Input and I/O lines from floating to intermediate voltage levels, which cause unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

## Input Diagram



## I/O Diagram



## Speed/Power Management

The ATF1500 has several built-in speed and power management features. The ATF1500L contains circuitry that automatically puts the device into a low power stand-by mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides a proportional power savings for most applications running at system speeds below 50 MHz.

All ATF1500s also have an optional pin-controlled power down mode. In this mode, current drops to below 10  $\mu$ A. When the power down option is selected, the PD pin is used to power down the part. The power down option is selected in the design source file. When enabled, the device goes into power down when the PD pin is high. In the power down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD is brought low. When the power down feature is enabled, the PD cannot be used as a logic input or output. However, the PD pin's macrocell may still be used to generate buried foldback and cascade logic signals.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

## Design Software Support

ATF1500 designs are supported by several 3rd party tools. Automated fitters allow logic synthesis using a variety of high level description languages and formats.





### Flip Flop

The ATF1500's flip flop has very flexible data and control functions. The data input can come from either the XOR gate or from a separate product term. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell.

In addition to D, T, JK and SR operation, the flip flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can be either the global CLK pin or an individual product term. The flip flop changes state on the clock's rising edge. When the CLK pin is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored.

The flip flop's asynchronous reset signal (AR) can be either the pin global clear (GCLR), a product term, or always off. AR can also be a logic OR of GCLR with a product term. The asynchronous preset (AP) can be a product term or always off.

### Output Select and Enable

The ATF1500 macrocell output can be selected as registered or combinatorial. When the output is registered, the same registered signal is fed back internally to the global bus. When the output is combinatorial, the buried feedback can be either the

same combinatorial signal or it can be the register output if the separate product term is chosen as the flip flop input.

The output enable multiplexer (MOE) controls the output enable signals. Any buffer can be permanently enabled for simple output operation. Buffers can also be permanently disabled to allow use of the pin as an input. In this configuration all the macrocell resources are still available, including the buried feedback, expander and CASCADE logic.

The output enable for each macrocell can also be selected as either of the two OE pins or as an individual product term.

### Global/Regional Busses

The global bus contains all Input and I/O pin signals as well as the buried feedback signal from all 32 macrocells. Together with the complement of each signal, this provides a 136 bit bus as input to every product term. Having the entire global bus available to each macrocell eliminates any potential routing problems. With this architecture designs can be modified without requiring pinout changes.

Each macrocell also generates a foldback product term. This signal goes to the regional bus, and is available to 16 macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The 16 foldback terms in each region allow generation of high fan-in sum terms (up to 21 product terms) with a small additional delay.





## Absolute Maximum Ratings\*

Temperature Under Bias.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground.....	-2.0 V to +7.0 V <sup>(1)</sup>
Voltage on Input Pins with Respect to Ground During Programming.....	-2.0 V to +14.0 V <sup>(1)</sup>
Programming Voltage with Respect to Ground.....	-2.0 V to +14.0 V <sup>(1)</sup>

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Note:

1. Minimum voltage is -0.6 V dc, which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is  $V_{CC} + 0.75$  V dc, which may overshoot to 7.0 V for pulses of less than 20 ns.

## D.C. and A.C. Operating Conditions

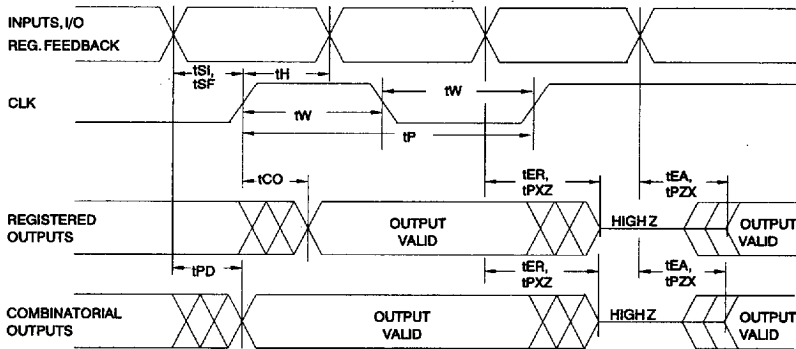
	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V <sub>CC</sub> Power Supply	5 V ± 5%	5 V ± 10%

## D.C. Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I <sub>IL</sub>	Input or I/O Low Leakage Current	0 ≤ V <sub>IN</sub> ≤ V <sub>IL</sub> (max)			-10	μA
I <sub>IH</sub>	Input or I/O High Leakage Current	V <sub>IH,min</sub> < V <sub>IN</sub> ≤ V <sub>CC</sub>			10	μA
I <sub>CC1</sub> <sup>(1)</sup>	Power Supply Current, Standby	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0, V <sub>CC</sub>	ATF1500	Com.	70	mA
				Ind.	100	mA
			ATF1500L	Com.	3	mA
				Ind.	5	mA
I <sub>CC2</sub> <sup>(1)</sup>	Power Supply Current, Power Down Mode	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0, V <sub>CC</sub>		Com.	10	μA
				Ind..	15	μA
I <sub>CC3</sub> <sup>(1)</sup>	Clocked Power Supply Current	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0, V <sub>CC</sub>	ATF1500L	Com.	1	mA/MHz
				Ind.	1	mA/MHz
I <sub>OS</sub>	Output Short Circuit Current	V <sub>OUT</sub> = 0.5 V			-130	mA
V <sub>IL</sub>	Input Low Voltage	V <sub>CC</sub> , min < V <sub>CC</sub> < V <sub>CC</sub> , max		-0.5	0.8	V
V <sub>IH</sub>	Input High Voltage			2.0	V <sub>CC</sub> + 1	V
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> = MIN I <sub>OL</sub> = 8 mA			0.45	V
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> = MIN I <sub>OH</sub> = -4 mA		2.4		V

Note: 1. All I<sub>CC</sub> parameters measured with outputs open, and a 16-bit loadable, up/down counter programmed into each region.

# A.C. Waveforms



## Register A.C. Characteristics, Input Pin Clock

Symbol	Parameter	-7		-10		-12		-15		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{COS}^{(1)}$	Clock to Output	4.5		2	5	2	6	2	8	2	12	ns
$t_{CFS}$	Clock to Feedback	2		2		2		2		2		ns
$t_{SIS}$	I, I/O Setup Time	6		8		10		11		13		ns
$t_{SFS}$	Feedback Setup Time	6		8		10		11		13		ns
$t_{HS}$	Input, I/O, Feedback Hold Time	0		0		0		0		0		ns
$t_{PS}$	Clock Period	6		8		9		10		12		ns
$t_{WS}$	Clock Width	3		4		4.5		5		6		ns
FMAXS	External Feedback $1/(t_{SIS} + t_{COS})$	95		76.9		62.5		52.6		40		MHz
	Internal Feedback $1/(t_{SFS} + t_{CFS})$	125		100		90.9		76.9		66		MHz
	No Feedback $1/(t_{PS})$	166.7		125		125		100		83		MHz
$t_{RPRS}$	Reset Pin Recovery Time	2		3		3		4		5		ns
$t_{RTRS}$	Reset Term Recovery Time	6		9		10		12		14		ns

Notes: 1. For slow slew outputs, add  $t_{SSO}$ .



## Register A.C. Characteristics, Product Term Clock

Symbol	Parameter	-7		-10		-12		-15		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tCOA <sup>(1)</sup>	Clock to Output	7.5		10		12		15		25		ns
tCFA	Clock to Feedback	5		7		7		9		11		ns
tSIA	I, I/O Setup Time	3		3		4		4		5		ns
tSFA	Feedback Setup Time	3		3		4		4		5		ns
tHA	Input, I/O, Feedback Hold Time	2		3		4		4		5		ns
tPA	Clock Period	6		8		10		12		16		ns
tWA	Clock Width	3		4		5		6		8		ns
FMAXA	External Feedback 1/(tSIA+tCOA)	95.2		76.9		62.5		52.6		33.3		MHz
	Internal Feedback 1/(tSFA+ tCFA)	125		100		90.9		76.9		62.5		MHz
	No Feedback 1/(tPA)	166.7		125		100		83.3		62.5		MHz
tRPRA	Reset Pin Recovery Time	0		0		0		0		0		ns
tRTRA	Reset Term Recovery Time	4		5		6		6		8		ns

## A.C. Characteristics

Symbol	Parameter	-7		-10		-12		-15		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPD <sup>(1)</sup>	I, I/O or FB to Non-Registered Output	2	7.5	3	10	3	12	3	15	3	25	ns
tPD2	I, I/O to Feedback	5		7		8		9		14		ns
tPD3 <sup>(1)</sup>	Feedback to Non-Registered Output	2	7.5	3	10	3	12	3	15	3	25	ns
tPD4	Feedback to Feedback	5		7		8		9		14		ns
tEA <sup>(1)</sup>	OE Term to Output Enable	2	7.5	3	10	3	12	3	15	3	25	ns
tER	OE Term to Output Disable	2	7.5	2	10	2	12	2	15	2	25	ns
tPZX <sup>(1)</sup>	OE Pin to Output Enable	2	5.5	2	7	2	8	2	9	2	11	ns
tPXZ	OE Pin to Output Disable	1.5	5.5	1.5	7	1.5	8	1.5	9	1.5	11	ns
tPW	Preset Width	3		4		4		5		6		ns
tPF	Preset To Feedback	6		9		9		12		20		ns
tPO <sup>(1)</sup>	Preset to Registered Output	8.5		12		14		20		25		ns
tRPW	Reset Pin Width	3		4		4		5		6		ns
tRPF	Reset Pin to Feedback	3		4		3		5		6		ns
tRPO <sup>(1)</sup>	Reset Pin to Registered Output	5.5		7		8		11		15		ns
tRTW	Reset Term Width	3		4		4		5		6		ns
tRTF	Reset Term to Feedback	6		9		9		12		20		ns
tRTO <sup>(1)</sup>	Reset Term to Registered Output	8.5		12		14		20		25		ns
tCAS	Cascade Logic Delay	0.8		0.8		1		1		1.5		ns
tSSO	Slow Slew Output Adder	3		3		3		4		4		ns
tFLD	Foldback Term Delay	4		5		7		8		12		ns

Notes: 1. For slow slew outputs, add tSSO.

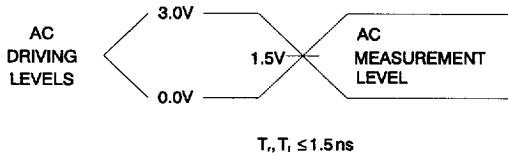


# Power Down A.C. Characteristics

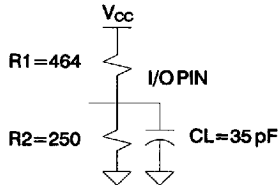
Symbol	Parameter	-7		-10		-12		-15		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tIVDH	Valid I, I/O Before PD High	7		10		12		15		25		ns
tGVDH	Valid OE(2) Before PD High	7		10		12		15		25		ns
tCVDH	Valid Clock <sup>(2)</sup> Before PD High	7		10		12		15		25		ns
tDHIX	I, I/O Hold After PD High		15		20		22		25		35	ns
tDHGX	OE <sup>(2)</sup> Hold After PD High		15		20		22		25		35	ns
tDHCX	Clock <sup>(2)</sup> Hold After PD High		15		20		22		25		35	ns
tDLIV	PD Low to Valid I, I/O		1		1		1		1		1	μs
tDLGV	PD Low to Valid OE (Pin or Term)		1		1		1		1		1	μs
tDLCV	PD Low to Valid Clock (Pin or Term)		1		1		1		1		1	μs
tDLOV	PD Low to Valid Output		1		1		1		1		1	μs

Notes: 1. For slow slew outputs, add tSSQ.  
2. Pin or Product Term.

## Input Test Waveforms and Measurement Levels:



## Output Test Load:



## Pin Capacitance ( $f = 1 \text{ MHz}$ , $T = 25^\circ\text{C}$ )<sup>(1)</sup>

	Typ	Max	Units	Conditions
C <sub>IN</sub>	5	8	pF	$V_{IN} = 0 \text{ V}$
C <sub>OUT</sub>	6	8	pF	$V_{OUT} = 0 \text{ V}$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

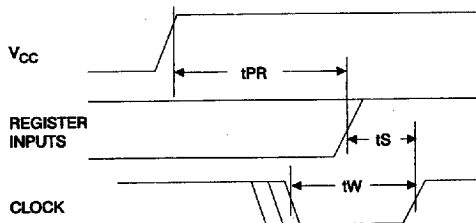


## Power Up Reset

The ATF1500's registers are designed to reset during power up. At a point delayed slightly from  $V_{CC}$  crossing  $V_{RST}$ , all registers will be reset to the low state. As a result, the registered output state will always be low on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how  $V_{CC}$  actually rises in the system, the following conditions are required:

- 1) The  $V_{CC}$  rise must be monotonic,
- 2) After reset occurs, all input and feedback setup times must be met before driving the clock signal high, and
- 3) Signals from which clocks are derived must remain stable during  $t_{PR}$ .



Parameter	Description	Typ	Max	Units
$t_{PR}$	Power-Up Reset Time	2	10	$\mu s$
$V_{RST}$	Power-Up Reset Voltage	3.8	4.5	V

## Power Down Mode

The ATF1500 includes an optional pin controlled power down feature. When this mode is enabled, the PD pin acts as the power down pin. When the PD pin is high, the device supply current is reduced to less than 10  $\mu A$ . During power down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs which were in a HI-Z state at the onset of power down will remain at HI-Z. During power down, all input signals except the power down pin are blocked. Input and I/O hold latches remain active to insure that pins do not float to indeterminate levels, further reducing system power. The power down pin feature is enabled in the logic design file. Designs using the power down pin may not use the PD pin logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

## Register Preload

The ATF1500's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with preload vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically when vectors are run by any approved programmers. The preload mode is enabled by raising an input pin to a high voltage level. Contact Atmel PLD Applications for PRELOAD pin assignments, timing and voltage requirements.

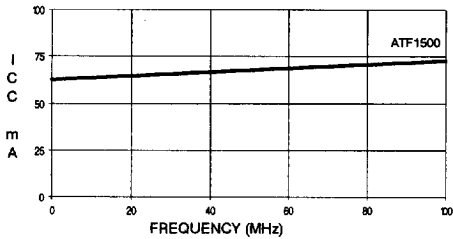
## Security Fuse

A single fuse is provided to prevent unauthorized copying of the ATF1500 fuse patterns. Once programmed, fuse verify and pre-load are inhibited.

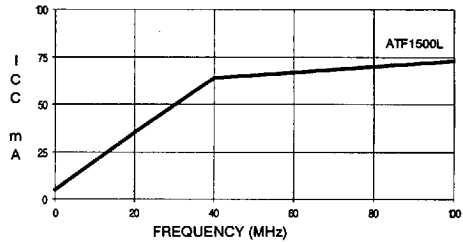
## Output Slew Rate Control

Each ATF1500 macrocell contains a configuration bit for each I/O to control its output slew rate. This allows selected data paths to operate at maximum throughput while reducing system noise from outputs that are not speed-critical. Outputs default to slow edges, and may be individually set to fast in the design file. Output transition times for outputs configured as slow have a  $T_{SSO}$  delay adder.

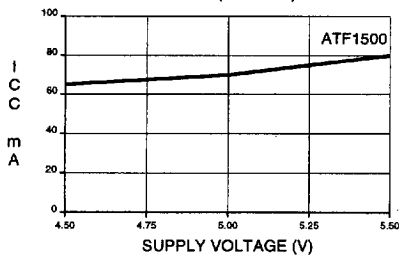
SUPPLY CURRENT vs. INPUT FREQUENCY  
ATF1500 (VCC=5V, TA=25°C)



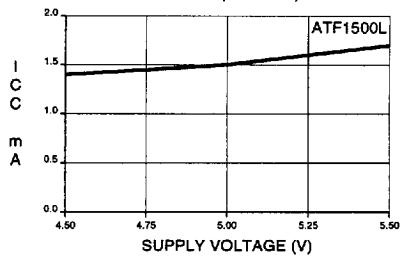
SUPPLY CURRENT vs. INPUT FREQUENCY  
ATF1500L (VCC=5V, TA=25°C)



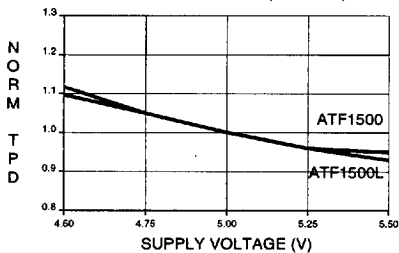
SUPPLY CURRENT vs. SUPPLY VOLTAGE  
ATF1500 (TA = 25°C)



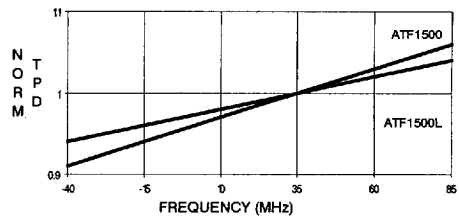
SUPPLY CURRENT vs. SUPPLY VOLTAGE  
ATF1500L (TA = 25°C)



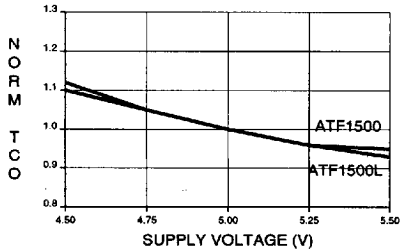
NORMALIZED TPD  
vs. SUPPLY VOLTAGE (TA = 25°C)



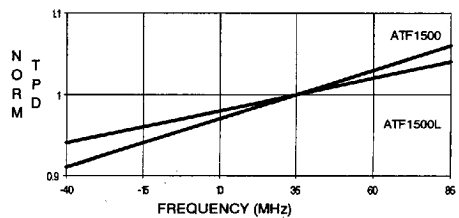
NORMALIZED TPD  
vs. AMBIENT TEMPERATURE (VCC=5V)



NORMALIZED TCO  
vs. SUPPLY VOLTAGE (TA = 25°C)



NORMALIZED TPD  
vs. AMBIENT TEMPERATURE (VCC=5V)





## Ordering Information

tpd (ns)	tcos (ns)	FMAXS (MHz)	Ordering Code	Package	Operation Range
7.5	4.5	95	ATF1500-7AC ATF1500-7JC	44A 44J	Commercial (0°C to 70°C)
10	5	76.9	ATF1500-10AC ATF1500-10JC	44A 44J	Commercial (0°C to 70°C)
			ATF1500-10JI	44J	Industrial (-40°C to 85°C)
12	6	62.5	ATF1500-12AC ATF1500-12JC	44A 44J	Commercial (0°C to 70°C)
15	8	52.6	ATF1500-15AC ATF1500-15JC	44A 44J	Commercial (0°C to 70°C)
			ATF1500-15JI	44J	Industrial (-40°C to 85°C)
15	8	52.6	ATF1500L-15AC ATF1500L-15JC	44A 44J	Commercial (0°C to 70°C)
			ATF1500L-15JI	44J	Industrial (-40°C to 85°C)
25	12	40	ATF1500L-25AC ATF1500L-25JC	44A 44J	Commercial (0°C to 70°C)
			ATF1500L-25JI	44J	Industrial (-40°C to 85°C)

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)

1-96

**ATF1500**

■ 1074177 0008614 955 ■