450mA, Low Noise Current Mode Step-Down DC/DC Converters

FEATURES

- **High Efficiency: Up to 93%**
- **Constant Frequency Adaptive Power™ Operation**
- **Input Voltage Range: 3V to 13.5V**
- Internal 0.6Ω Power Switch (V_{IN} = 10V)
- **Low Dropout Operation: 100% Duty Cycle**
- Low-Battery Detector
- Internal Power-On Reset Timer
- Current Mode Operation for Excellent Line and Load Transient Response
- Low Quiescent Current: 470µA
- Shutdown Mode Draws Only 15µA Supply Current
- ±1% Reference Accuracy
- Available in 16- and 20-Lead Narrow SSOP

APPLICATIONS

- Cellular Telephones
- Portable Instruments
- Wireless Modems
- RF Communications
- Distributed Power Systems
- Scanners
- Battery-Powered Equipment

DESCRIPTION

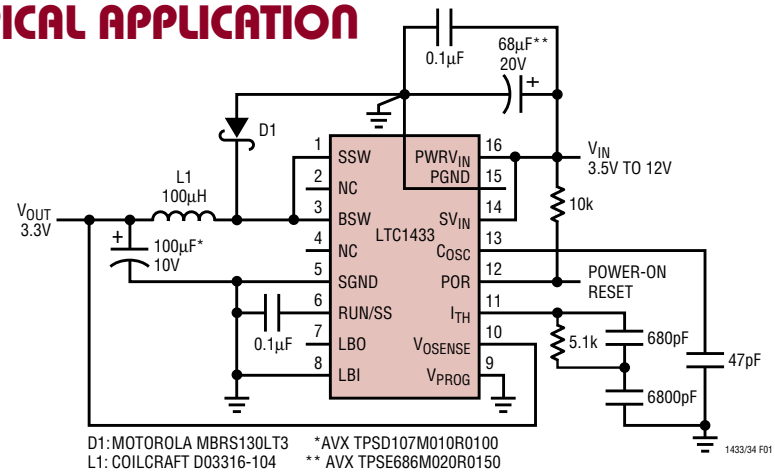
The LTC®1433/LTC1434 are monolithic pulse width modulated step-down DC/DC converters. By utilizing current mode switching techniques, they provide excellent AC and DC load and line regulation. Both devices operate at a fixed frequency with the LTC1434 phase-lockable to an external clock signal.

Both devices incorporate two internal P-channel power MOSFETs with a parallel combined resistance of 0.6Ω (at a supply of 10V). The Adaptive Power output stage selectively drives one or both of the switches at frequencies up to 700kHz to reduce switching losses and maintain high efficiencies at low output currents.

The LTC1433/LTC1434 are capable of supplying up to 450mA of output current and boasts a ±2.4% output voltage accuracy. An internal low-battery detector has the same level of accuracy as the output voltage. A power-on reset timer (POR) is included which generates a signal delayed by 65536/f_{CLK} (300ms typ) after the output is within 5% of the regulated output voltage.

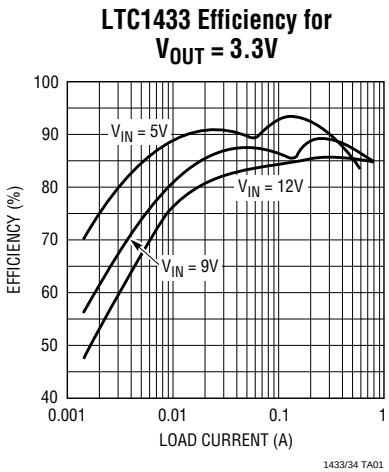
Ideal for current sensitive applications, the devices draw only 470µA of quiescent current. In shutdown the devices draw a mere 15µA. To further maximize the life of the battery source, the internal P-channel MOSFET switch is turned on continuously in dropout.

TYPICAL APPLICATION



D1: MOTOROLA MBRS130LT3 *AVX TPSD107M010R0100
L1: COILCRAFT D03316-104 ** AVX TPSE686M020R0150

Figure 1. High Efficiency Step-Down Converter

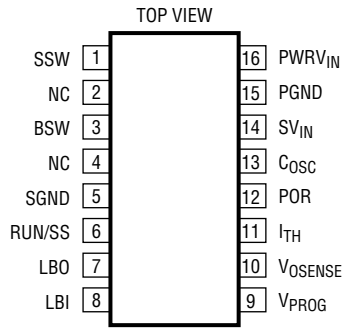


ABSOLUTE MAXIMUM RATINGS (Note 1)

(Voltages Referred to PGND Pin)

Input Supply Voltage ($PWRV_{IN}$, SV_{IN}) ... 13.5V to –0.3V
DC Small Switch Current (SSW) 100mA
Peak Small Switch Current (SSW) 300mA
Small Switch Voltage
(SSW) ..... (V_{IN} + 0.3V) to (V_{IN} – 13.5V)
DC Large Switch Current (BSW) 600mA
Peak Large Switch Current (BSW) 1.2A
Large Switch Voltage
(BSW) ..... (V_{IN} + 0.3V) to (V_{IN} – 13.5V)
PLLIN, PLL LPF, I_{TH}, C_{OSC} ..... 2.7V to –0.3V
POR, LBO ..... 12V to –0.3V
LBI, V_{OSENSE} ..... 10V to –0.3V
RUN/SS, V_{PROG} Voltages
$V_{IN} \geq 11.7V$ ..... 12V to –0.3V
$V_{IN} < 11.7V$ ..... (V_{IN} + 0.3V) to –0.3V
Commercial Temperature Range
LTC1433C/LTC1434C ..... 0°C to 70°C
Extended Commercial Operating Temperature
Range (Note 2) ..... –40°C to 85°C
Industrial Temperature Range (Note 3)
LTC1433I/LTC1434I ..... –40°C to 85°C
Junction Temperature (Note 4) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

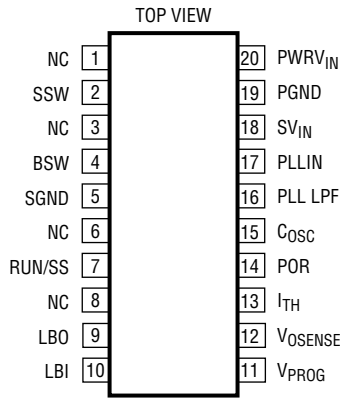


GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

LTC1433CGN
LTC1433IGN



GN PACKAGE
20-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

LTC1434CGN
LTC1434IGN

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V, $V_{RUN/SS}$ = 5V, unless otherwise noted. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
I_{IN} V_{OSENSE}	Feedback Current	V_{PROG} Pin Open (Note 5)			10	50	nA
V_{OSENSE}	Regulated Output Voltage 1.19V (Adjustable) Selected 3.3V Selected 5V Selected	(Note 5) V_{PROG} Pin Open V_{PROG} = 0V V_{PROG} = V_{IN}	 ● ● ●	 1.178 3.220 4.880	 1.190 3.300 5.000	 1.202 3.380 5.120	 V V V
V_{OVL}	Output Overvoltage Lockout	V_{PROG} Pin Open		1.24	1.28	1.32	V
ΔV_{OSENSE}	Reference Voltage Line Regulation	V_{IN} = 3.6V to 13V (Note 5), V_{PROG} Pin Open			0.002	0.01	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	I_{TH} Sinking 5µA (Note 5) I_{TH} Sourcing 5µA (Note 5)	● ●		0.5 –0.5	0.8 –0.8	% %

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V, $V_{RUN/SS}$ = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{PROG}	V_{PROG} Input Current	0.5V > V_{PROG} V_{IN} – 0.5V < V_{PROG} < V_{IN}			–4 4	–10 10	µA µA
Main Control Loop							
I_Q	Input DC Supply Current Normal Mode Shutdown, Reference Alive Complete Shutdown	(Note 6) 3.6V < V_{IN} < 13V $V_{RUN/SS}$ = 0V, 3.6V < V_{IN} < 13V, LBI > 0.9V $V_{RUN/SS}$ = 0V, 3.6V < V_{IN} < 13V, LBI ≤ 0.48V			 470 35 15	 70 30	 µA µA µA
$V_{RUN/SS}$	RUN/SS Threshold		●	0.8	1.3	2	V
$I_{RUN/SS}$	Soft Start Current Source	$V_{RUN/SS}$ = 0V		1.2	3	4.5	µA
Oscillator and Phase-Locked Loop							
f_{OSC}	Oscillator Frequency V_{CO} High	C_{OSC} = 100pF (Note 7) $V_{PLL\ LPF}$ = 2.4V		112 200	125 240	142	kHz kHz
R_{PLLIN}	PLL Input Resistance				50		kΩ
$I_{PLL\ LPF}$	Phase Detector Output Current Sinking Capability Sourcing Capability	 f_{PLLIN} < f_{OSC} f_{PLLIN} > f_{OSC}		 10 10	 15 15	 20 20	 µA µA
Power-On Reset							
V_{SATPOR}	POR Saturation Voltage	I_{POR} = 1.6mA, V_{OSENSE} = 1V, V_{PROG} Open			0.6	1.0	V
I_{LPOR}	POR Leakage	V_{POR} = 10V, V_{OSENSE} = 1.2V, V_{PROG} Open			0.2	1.0	µA
V_{TRPOR}	POR Trip Voltage from Regulated Output	V_{PROG} Pin Open, V_{OSENSE} Ramping Negative		–11	–7.5	–4	%
t_{DPOR}	POR Delay	V_{PROG} Pin Open			65536		Cycles
Low-Battery Comparator							
V_{SATLBO}	LBO Saturation Voltage	I_{LBO} = 1.6mA, V_{LBI} = 1.1V			0.6	1.0	V
I_{LLBO}	LBO Leakage	V_{LBO} = 10V, V_{LBI} = 1.4V			0.01	1.0	µA
V_{TRLBI}	LBI Trip Voltage	High to Low Transition on LBO		1.16	1.19	1.22	V
V_{HYSTLB}	Low-Battery Comparator Hysteresis				40		mV
V_{SDLB}	Low-Battery Shutdown Trip Point				0.74		V
I_{INLBI}	LBI Input Current	V_{LBI} = 1.19V			1	50	nA
P-Channel Power FETs Characteristics							
R_{SMFET}	$R_{DS(ON)}$ of Small FET	I_{SSW} = 15mA			3.3	4.1	Ω
R_{BIGFET}	$R_{DS(ON)}$ of Big FET	I_{BSW} = 150mA			0.8	1.2	Ω
I_{LSSW}	Small FET Leakage	$V_{RUN/SS}$ = 0V	●		7	1000	nA
I_{LBSW}	Big FET Leakage	$V_{RUN/SS}$ = 0V	●		5	1000	nA

The ● denotes specifications which apply over the specified temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: C-grade device specifications are guaranteed over the 0°C to 70°C temperature range. In addition, C-grade device specifications are assured over the –40°C to 85°C temperature range by design or correlation, but are not production tested.

Note 3: I-grade device specifications are guaranteed over the –40°C to 85°C temperature range by design, testing or correlation.

Note 4: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC1433/LTC1434: $T_J = T_A + (P_D)(150°C/W)$

Note 5: The LTC1433/LTC1434 are tested in a feedback loop which servos V_{OSENSE} to the feedback point for the error amplifier (V_{ITH} = 1.19V).

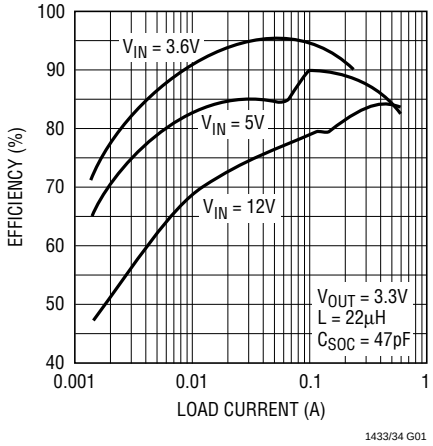
Note 6: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 7: Oscillator frequency is tested by measuring the C_{OSC} charge and discharge currents and applying the formula:

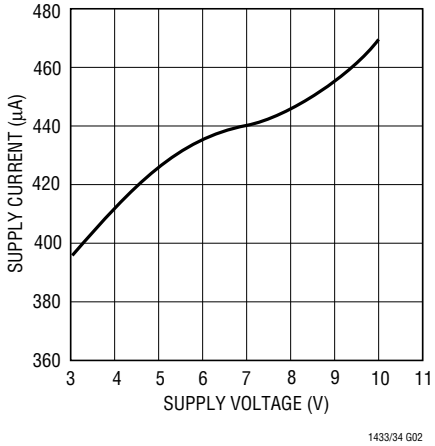
$$f_{OSC}\ (kHz) = \left(\frac{8.4(10^8)}{C_{OSC}\ (pF) + 11}\right)\left(\frac{1}{I_{CHG}} + \frac{1}{I_{DIS}}\right)^{-1}$$

TYPICAL PERFORMANCE CHARACTERISTICS

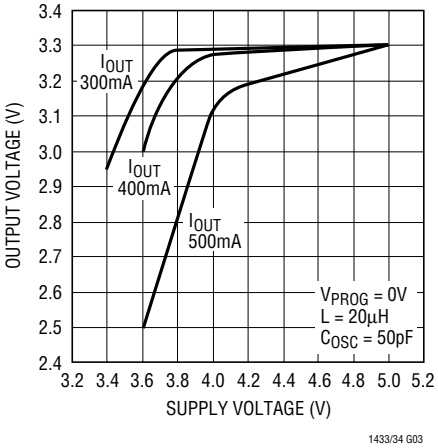
Efficiency of Figure 1 for L = 22µH



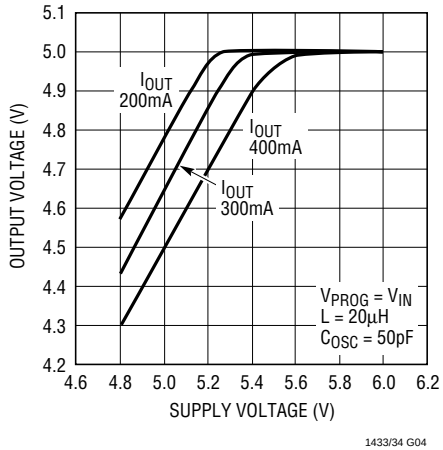
Supply Current vs Supply Voltage



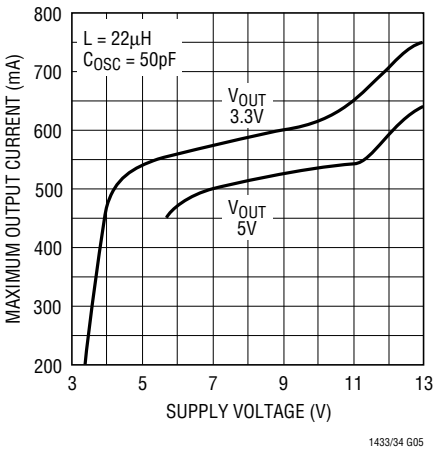
Dropout Characteristics at Different Load Currents (V_{OUT} = 3.3V)



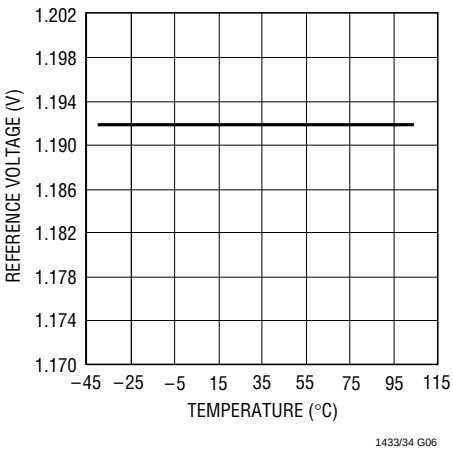
Dropout Characteristics at Different Load Currents (V_{OUT} = 5V)



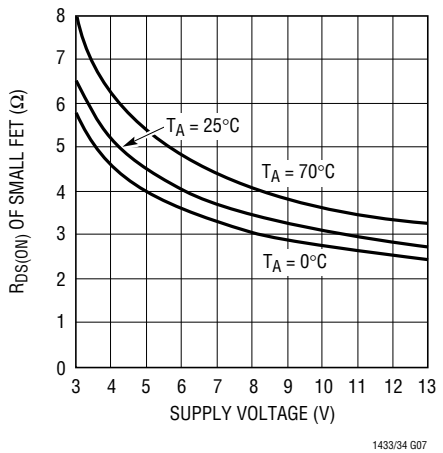
Maximum Output Current vs Input Supply



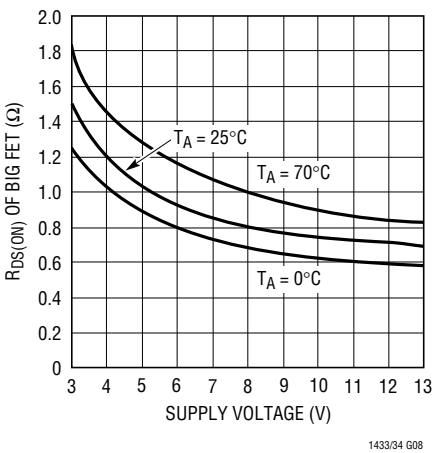
Reference Voltage vs Temperature



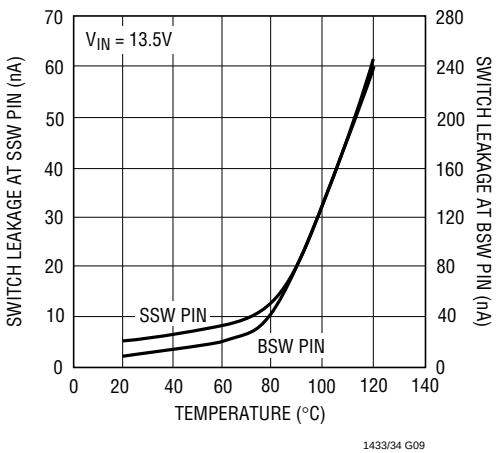
Switch Resistance of Small FET



Switch Resistance of Big FET



Switch Leakage Current vs Temperature



PIN FUNCTIONS (LTC1433/LTC1434)

SSW (Pin 1/Pin 2): Drain of the Small P-Channel MOSFET Switch.

BSW (Pin 3/Pin 4): Drain of the Large P-Channel MOSFET Switch.

SGND (Pin 5): Small-Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

RUN/SS (Pin 6/Pin 7): Combination of Soft Start and Run Control Inputs. A capacitor to ground at this pin sets the ramp time to full current output. The time is approximately 0.5s/μF. Forcing this pin below 1.3V causes all circuitry to be shut down except the low-battery comparator. For input voltages above 6V this pin is clamped by a 6V Zener (see Functional Diagram). Applying voltages greater than 6V to this pin will cause additional current to flow into this pin.

LBO (Pin 7/Pin 9): Open-Drain Output of an N-Channel Pull-Down. This pin will sink current when LBI goes below 1.19V.

LBI (Pin 8/Pin 10): The (+) Input of the Low-Battery Voltage Comparator. The (–) input is connected to the 1.19V reference. When LBI is grounded along with RUN/SS, this comparator will shut down along with the rest of the control circuitry. LBO will go to high impedance.

V_{PROG} (Pin 9/Pin 11): The voltage at this pin selects the output voltage. When V_{PROG} = 0V or V_{PROG} = V_{IN}, the output is set to 3.3V and 5V respectively, with V_{OSENSE} connected to the output. Leaving V_{PROG} open (DC) allows the output voltage to be set by an external resistive divider. V_{OSENSE} is then connected to the common node of the resistive divider.

V_{OSENSE} (Pin 10/Pin 12): This pin receives the feedback voltage either from the output or from an external resistive divider across the output. The V_{PROG} pin determines at which point V_{OSENSE} must be connected.

V_{PROG} = 0V	V_{OUT} = 3.3V
V_{PROG} = V_{IN}	V_{OUT} = 5V
V_{PROG} = Open (DC)	V_{OUT} = Adjustable

I_{TH} (Pin 11/Pin 13): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 2.4V.

POR (Pin 12/Pin 14): Open-Drain Output of an N-Channel Pull-Down. This pin sinks current when the output voltage is 7.5% out of regulation. When the output rises to –5% of its regulated value, the pin goes into high impedance after 2^{16} (65536) oscillator cycles. The POR output is asserted when the device is in shutdown, independent of V_{OUT}.

C_{OSC} (Pin 13/Pin 15): External capacitor connects between this pin and ground to set the operating frequency.

PLL LPF (Pin 16 LTC1434): Output of the Phase Detector and Control Input of the Oscillator. Normally a series RC lowpass network is connected from this pin to ground. Tie this pin to SGND in applications which do not use the phase-locked loop. Can be driven by a 0V to 2.4V logic signal for a frequency shifting option.

PLLIN (Pin 17 LTC1434): External Synchronizing Input to the Phase Detector. This pin is internally terminated to SGND with 50kΩ. Tie this pin to SGND in applications which do not use the phase-locked loop.

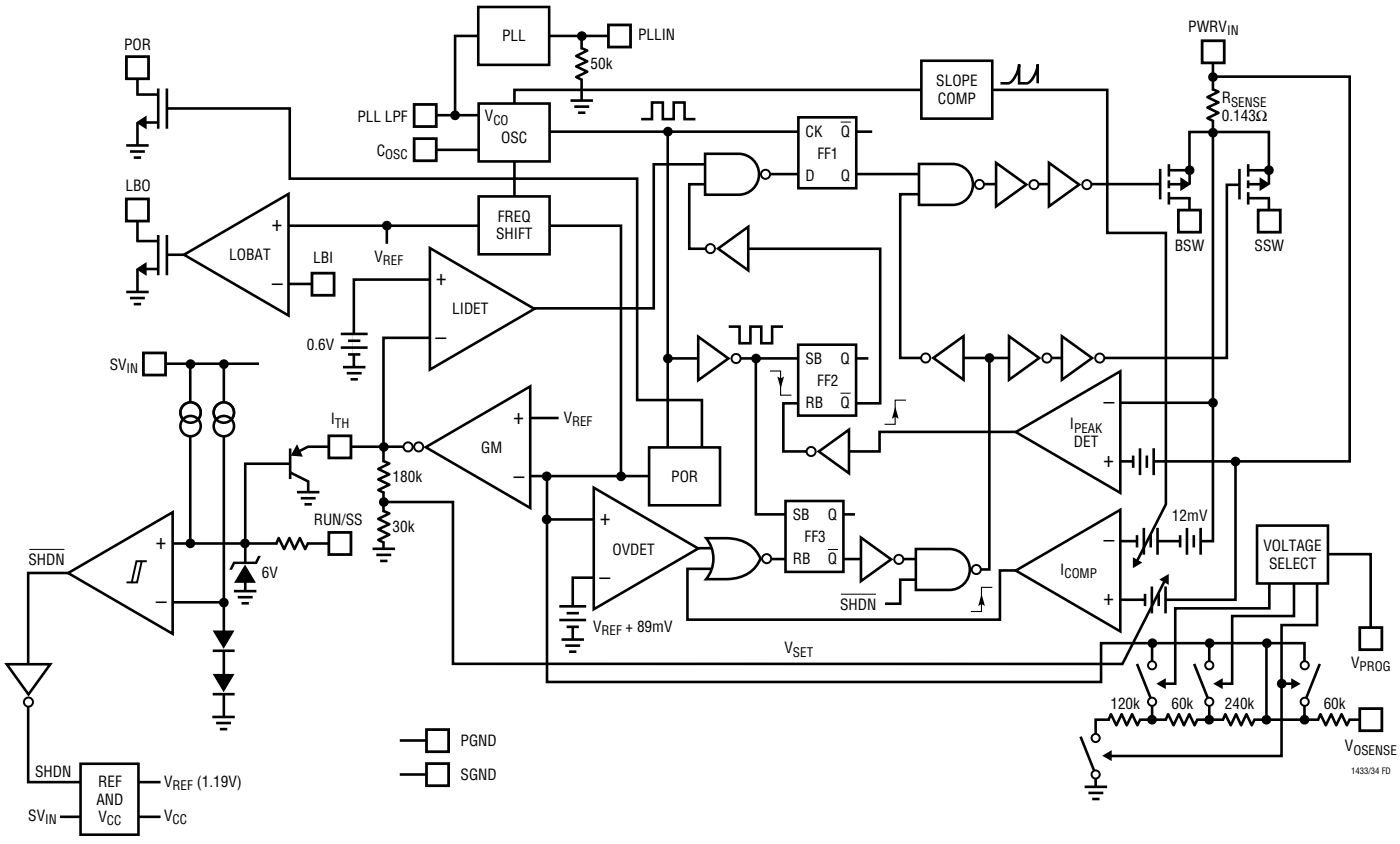
SV_{IN} (Pin 14/Pin 18): Main Supply for All the Control Circuitry.

PGND (Pin 15/Pin 19): Switch Driver Ground. Connects to the (–) terminal of C_{IN}. Anode of the Schottky diode must be connected close to this pin.

$PWRV_{IN}$ (Pin 16/Pin 20): Supply for the Internal Power MOSFETs and Switch Drivers. Must decouple this pin properly to ground.

NC (Pins 2, 4,/Pins 1, 3, 6, 8): No Connection.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC1433/LTC1434 is a constant frequency, pulse-width modulated current mode switching regulator. During normal operation, the internal P-channel power MOSFET is turned on each cycle when the oscillator sets the RS latch FF3, and turned off when the main current comparator I_{COMP} resets the latch. The peak inductor current at which the I_{COMP} resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of error amplifier GM. Pins V_{PROG} and V_{OSENSE}, described in the Pin Functions section, allow GM to receive an output feedback voltage V_{FB} from either the internal or external resistive dividers. When the load current increases, it causes a slight decrease in V_{FB} relative to the 1.19V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current.

The main control loop is shut down by pulling the RUN/SS pin low. Releasing RUN/SS allows an internal 3µA current source to charge up the soft start capacitor C_{SS}. When C_{SS} reaches 1.3V, the main control loop is enabled with the I_{TH} voltage clamped at approximately 30% of its maximum value. As C_{SS} continues to charge, I_{TH} is gradually released allowing normal operation to resume.

Comparator OVDET guards against transient overshoots > 7.5% by turning off the P-channel power MOSFETs and keeping them off until the fault is removed.

Low Current Operation

The LTC1433/LTC1434 have two internal P-channel MOSFETs sized for low and high load current conditions. At low load current, only the small MOSFET will be turned on while at high load current both MOSFETs will be on.

OPERATION (Refer to Functional Diagram)

Having only the small MOSFET on with low load current reduces switching and gate charge losses, hence boosting efficiency. For the device to go into low current mode, two conditions must be satisfied: the peak current of the inductor should not exceed 260mA and the voltage at the I_{TH} pin should not exceed 0.6V. When either one of the conditions is exceeded, the big MOSFET will be turned on at the next clock cycle.

Dropout Operation

When the input supply voltage decreases toward the output voltage, the rate of change of inductor current during the on cycle decreases. This reduction means that the P-channel MOSFETs will remain on for more than one oscillator cycle since the I_{COMP} is not tripped. Further reduction in input supply voltage will eventually cause the P-channel MOSFET to be turned on 100%, i.e., DC. The output voltage will then be determined by the input voltage minus the voltage drop across the MOSFETs. Typically under dropout, both the power MOSFETs are on since the voltage on the I_{TH} pin is greater than 0.6V.

Frequency Synchronization

A phase-locked loop (PLL) is available on the LTC1434 to allow the oscillator to be synchronized to an external source connected to the PLLIN pin. The output of the phase detector at the PLL LPF pin is also the control input of the oscillator, which operates over a 0V to 2.4V range corresponding to –30% to +30% in the oscillator's center frequency. When locked, the PLL aligns the turn-on of the MOSFETs to the rising edge of the synchronizing signal. When the PLLIN is left open, PLL LPF goes low, forcing the oscillator to minimum frequency.

Power-On Reset

The POR pin is an open-drain output which pulls low when the regulator is out of regulation. When the output voltage rises to within 5% of regulation, a timer is started which releases POR after 2^{16} (65536) oscillator cycles. In shutdown the POR output is pulled low.

Short-Circuit Protection

When the output is shorted to ground, the frequency of the oscillator will be reduced to about 1/4.5 of its designed rate. This low frequency allows the inductor current to discharge, thereby preventing runaway. The oscillator's frequency will gradually increase to its designed rate when the output voltage increases above 0.65V.

APPLICATIONS INFORMATION

The basic LTC1434 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of C_{OSC} and L. Next, the Schottky diode D1 is selected followed by C_{IN} and C_{OUT}.

C_{OSC} Selection for Operating Frequency

The LTC1433/LTC1434 use a constant frequency architecture with the frequency determined by an external oscillator capacitor C_{OSC}. During the on-time, C_{OSC} is charged by a fixed current plus an additional current which is proportional to the output voltage of the phase detector ($V_{PLL\ LPF}$ on LTC1434). When the voltage on the C_{OSC} capacitor reaches 1.19V, it is reset to ground. The process then repeats.

The value of C_{OSC} is calculated from the desired operating frequency. Assume the phase-locked loop has no external oscillator input, i.e. $V_{PLL\ LPF}$ = 0V.

$$C_{OSC}\left(pF\right) = \left[\frac{1.37\left(10^4\right)}{\text{Frequency}\left(kHz\right)}\right] - 11$$

A graph for selecting C_{OSC} vs Frequency is given in Figure 2. For the LTC1433, the expression above is also applicable since its oscillator is internally set up to run at a condition equal to $V_{PLL\ LPF}$ = 0V. Therefore when using the graph for determining the capacitance value for the oscillator frequency, the $V_{PLL\ LPF}$ = 0V curve should be used for LTC1433.

APPLICATIONS INFORMATION

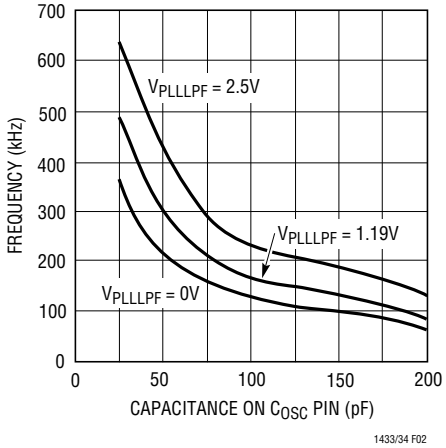


Figure 2. Selecting C_{OSC} for Oscillator Frequency

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency. The maximum recommended switching frequency is 700kHz. When using Figure 2 for synchronizable applications, the value of C_{OSC} is selected corresponding to a frequency 30% below your center frequency (see Phase-Locked Loop and Frequency Synchronization).

Low Supply Operation

The LTC1433/LTC1434 can function down to 3V and the maximum allowable output current is also reduced at low input voltages. Figure 3 shows the amount of change as the supply is reduced down to 2.5V. The minimum guaranteed input supply is 3V.

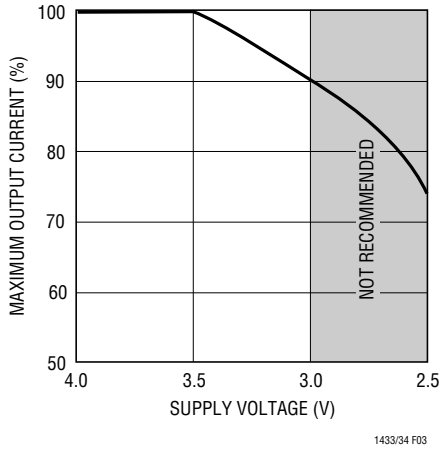


Figure 3. Maximum Allowable Output Current vs Supply Voltage

Another important point to note is that at a low supply voltages, the $R_{DS(ON)}$ of the P-channel switch increases (see Typical Performance Characteristics). Therefore, the user should calculate the power dissipation when the LTC1433/LTC1434 are used at 100% duty cycle with low input voltages.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies permit the use of a smaller inductor for the same amount of inductor ripple current. However, this is at the expense of efficiency due to an increase in MOSFET gate charge losses.

The inductor value has a direct effect on ripple current. The ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Core losses are dependent on the peak-to-peak ripple current and core material. Hence, by choosing a larger inductance the peak-to-peak inductor ripple current will decrease, therefore decreasing core loss. To further reduce losses, low core loss material such as molypermalloy or Kool Mμ® can be chosen as the inductor core material.

An indirect way that the inductor affects efficiency is through the usage of the big P-channel at low load currents. Lower inductance values will result in high peak inductor current. Because one of the conditions that determines the turning on of the large P-channel is peak current, this will result in the usage of the large P-channel even though the load current is low. Hence, efficiency at low load current will be affected. See Efficiency Considerations.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Kool Mμ is a registered trademark of Magnetics, Inc.

APPLICATIONS INFORMATION

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. **Do not allow the core to saturate!**

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, designs for surface mount are available which do not increase the height significantly.

Catch Diode Selection

The catch diode carries load current during the off-time. The average diode current is therefore dependent on the P-channel switch duty cycle. At high input voltages the diode conducts most of the time. As V_{IN} approaches V_{OUT} the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output is short circuited. Under this condition the diode must safely handle I_{PEAK} at close to 100% duty cycle. A fast switching diode must also be used to optimize efficiency. Schottky diodes are a good choice for low forward drop and fast switching times. Most LTC1433/LTC1434 circuits will be well served by either a 1N5818, an MBRS130LT3 or an MBRM5819 Schottky diode.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \approx I_{MAX} \frac{\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement is satisfied the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{4fC_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. For the LTC1433/LTC1434, the general rule for proper operation is:

C_{OUT} required ESR < 0.25Ω

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR/size ratio of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, Nichicon PL series and Panasonic SP series. Consult the manufacturer for other specific recommendations.

APPLICATIONS INFORMATION

Efficiency Considerations

Since there are two separate pins for the drain of the small and large P-channel switch, we could utilize two inductors to further enhance the efficiency of the regulator over the low load current range. Figure 4 shows the circuit connection.(Also refer to the Typical Applications section.)

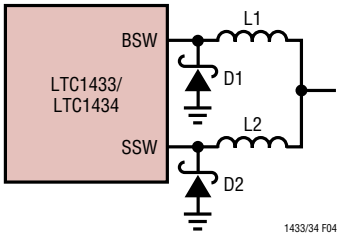


Figure 4. Using Two Inductors for Higher Low Current Efficiency

To reduce core losses, the user can use a higher value inductor on the small P-channel switch. Since this switch only carries a small part of the overall current, the user can still use a small physical size inductor without sacrificing on copper losses. The Schottky diode can also be chosen with a lower current rating. For the graph in Figure 5, a Coilcraft DT1608C series inductor is used along with a MBRS0520LT3 Schottky diode on the SSW pin. As can be seen from Figure 5, the average efficiency gain over the region where the small P-channel is on is about 3%.

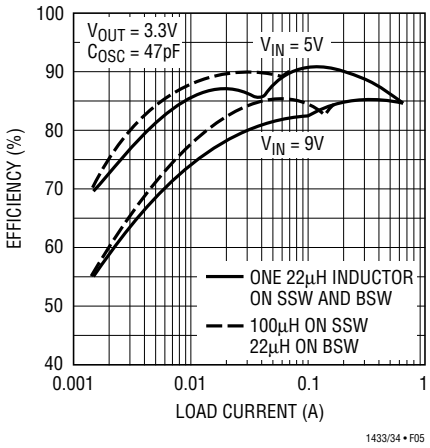


Figure 5. Efficiency Comparison Between Single Inductor and Dual Inductor

Hence, the dual inductor configuration is good for the user who requires as high an efficiency as possible at low load while retaining constant frequency operation.

Output Voltage Programming

The LTC1433/LTC1434 family all have pin selectable output voltage programming. The output voltage is selected by the V_{PROG} pin as follows:

V_{PROG} = 0V	V_{OUT} = 3.3V
V_{PROG} = V_{IN}	V_{OUT} = 5V
V_{PROG} = Open (DC)	V_{OUT} = Adjustable

The LTC1433/LTC1434 family also has remote output voltage sense capability. The top of the internal resistive divider is internally connected to V_{OSENSE}. For fixed output voltage applications, the V_{OSENSE} pin is connected to the output voltage as shown in Figure 6. When using an external resistive divider, the V_{PROG} pin is left open DC and the V_{OSENSE} pin is connected to the feedback resistors as shown in Figure 7. To prevent stray pickup, a 100pF capacitor is suggested across R1 located close to the LTC1433/LTC1434.

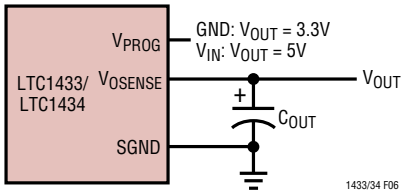


Figure 6. LTC1433/LTC1434 Fixed Output Applications

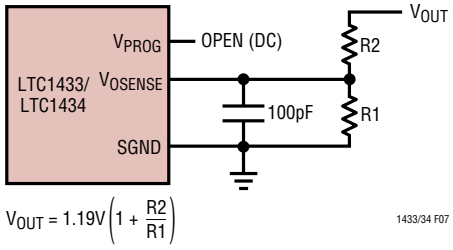


Figure 7. LTC1433/LTC1434 Adjustable Applications

APPLICATIONS INFORMATION

Power-On Reset Function (POR)

The power-on reset function monitors the output voltage and turns on an open-drain device when it is out of regulation. An external pull-up resistor is required on the POR pin.

When power is first applied or when coming out of shutdown, the POR output is pulled to ground. When the output voltage rises above a level which is 5% below the regulated output value, an internal counter starts. After counting 2^{16} (65536) clock cycles the POR pull-down device turns off.

The POR output will go low whenever the output voltage drops below 7.5% of its regulated value for longer than approximately 30µs, signaling an out-of-regulation condition. In shutdown the POR output is pulled low even if the regulator's output is held up by an external source.

Run/Soft Start Function

The RUN/SS pin is a dual purpose pin which provides the soft start function and a means to shut down the LTC1433/LTC1434. Soft start reduces input surge currents by providing a gradual ramp-up of the internal current limit. Power supply sequencing can also be accomplished using this pin.

An internal 3µA current source charges up an external capacitor C_{SS}. When the voltage on RUN/SS reaches 1.3V the LTC1433/LTC1434 begins operating. As the voltage on RUN/SS continues to ramp from 1.3V to 2.4V the internal current limit is also ramped at a proportional linear rate. The current limit begins at approximately 350mA (at $V_{RUN/SS}$ = 1.3V) and ends at 1.2A ($V_{RUN/SS}$ = 2.4V). The output voltage thus ramps up slowly, charging the output capacitor while input surge currents are reduced. If RUN/SS has been pulled all the way to ground there is a delay of approximately 0.5s/µF before starting, followed by a like time to reach full current.

$$t_{DELAY} = 5(10^5)C_{SS} \text{ seconds}$$

By pulling the RUN/SS pin below 1.3V, the LTC1433/LTC1434 are put in low current shutdown. This pin can be driven directly from logic as shown in Figure 8. Diode D1 in Figure 8 reduces the start delay but allows C_{SS} to ramp up slowly providing the soft start function. This diode can be deleted if soft start is not needed. The RUN/SS pin has an internal 6V Zener clamping the voltage on this pin (see Functional Diagram).

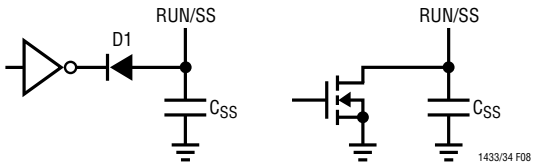


Figure 8. RUN/SS Pin Interfacing

Phase-Locked Loop and Frequency Synchronization

The LTC1434 has an internal voltage-controlled oscillator and phase detector comprising a phase-locked loop. This allows the MOSFET turn-on to be locked to the rising edge of an external source. The frequency range of the voltage-controlled oscillator is ±30% around the center frequency f_O. The value of C_{OSC} is calculated from the desired operating frequency (f_O) with the following expression (assuming the phase-locked loop is locked, i.e $V_{PLL\ LPF}$ = 1.19V):

$$C_{OSC}\left(pF\right) = \left[\frac{2.06\left(10^4\right)}{\text{Frequency}\left(kHz\right)}\right] - 11$$

Instead of using the above expression, Figure 2 graphically shows the relationship between the oscillator frequency and the value of C_{OSC} under various voltage conditions at the PLL LPF pin.

The phase detector used is an edge sensitive digital type which provides zero degrees phase shift between the external and internal oscillators. This type of phase detector will not lock up on input frequencies close to the harmonics of the V_{CO} center frequency. The PLL hold-in range Δf_H is equal to the capture range, $\Delta f_H = \Delta f_C = \pm 0.3 f_O$.

The output of the phase detector is a pair of complementary current sources charging or discharging the external filter network on the PLL LPF pin. The relationship between the voltage on the PLL LPF pin and operating frequency is shown in Figure 9. A simplified block diagram is shown in Figure 10.

APPLICATIONS INFORMATION

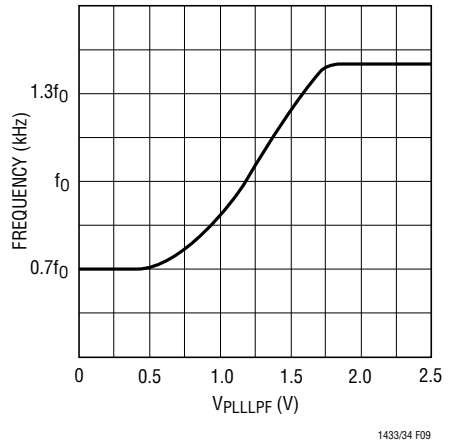


Figure 9. Relationship Between Oscillator Frequency and Voltage at PLL LPF Pin

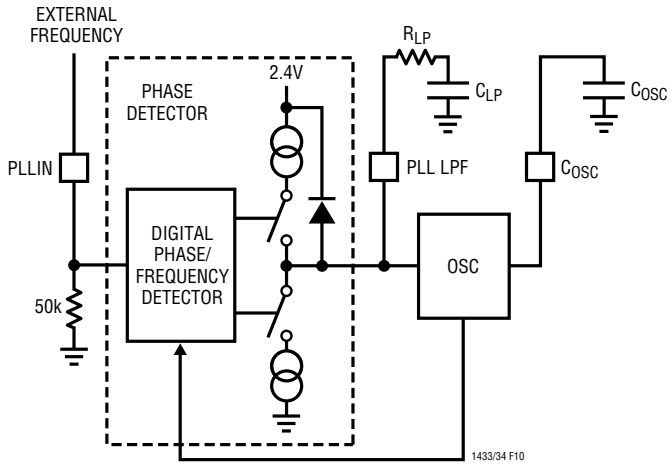


Figure 10. Phase-Locked Loop Block Diagram

If the external frequency (V_{PLLIN}) is greater than the center frequency f_0, current is sourced continuously, pulling up the PLL LPF pin. When the external frequency is less than f_0, current is sunk continuously, pulling down the PLL LPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus the voltage on the PLL LPF pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point the phase comparator output is open and the filter capacitor C_{LP} holds the voltage.

The loop filter components C_{LP} and R_{LP} smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} = 10k and C_{LP} is 0.01µF to 0.1µF. Be sure to connect the low side of the filter to SGND.

The PLL LPF pin can be driven with external logic to obtain a 1:1.9 frequency shift. The circuit shown in Figure 11 will provide a frequency shift from f_0 to $1.9f_0$ as the voltage $V_{PLL\ LPF}$ increases from 0V to 2.4V. *Do not exceed 2.4V on $V_{PLL\ LPF}$.*

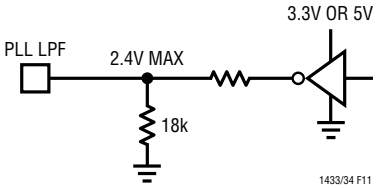


Figure 11. Directly Driving PLL LPF Pin

Low-Battery Comparator

The LTC1433/LTC1434 have an on-chip, low-battery comparator which can be used to sense a low-battery condition when implemented as shown in Figure 12. The resistor divider R3/R4 sets the comparator trip point as follows:

$$V_{LBTRIP} = 1.19\left(\frac{R4}{R3} + 1\right)$$

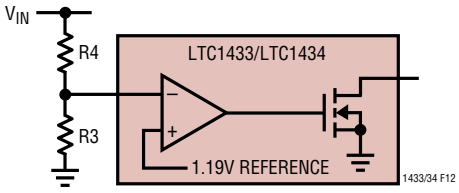


Figure 12. Low-Battery Comparator

The divided down voltage at the negative (–) input to the comparator is compared to an internal 1.19V reference. A 40mV hysteresis is built in to assure rapid switching. The output is an open-drain MOSFET and requires a pull-up resistor to operate. This comparator is active in shutdown. To save more shutdown quiescent current, this comparator can be shut down by taking the LBI pin below 0.74V,

APPLICATIONS INFORMATION

further reducing the current to 15μA. The low side of the resistive divider should connect to SGND.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1433/LTC1434. These items are also illustrated graphically in the layout diagram of Figure 13. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1433/LTC1434 signal ground pin must return to the (–) plate of C_{OUT}. The power ground returns to the anode of the Schottky diode and the (–) plate of C_{IN}, which should have as short lead lengths as possible.
2. Does the LTC1433/LTC1434 V_{OSENSE} pin connect to the (+) plate of C_{OUT}? In adjustable applications, the resistive divider R1/R2 must be connected between the (+) plate of C_{OUT} and signal ground.
3. Does the (+) plate of C_{IN} connect to the power V_{IN} as close as possible? This capacitor provides the AC current to the internal P-channel MOSFETs and their drivers.
4. Is the Schottky diode closely connected between the power ground and switch pin?
5. Keep the switching nodes, SSW and BSW away from sensitive small-signal nodes V_{OSENSE}, PLLIN, PLL LPF, C_{OSC}, I_{TH} and LBI.

Design Example

As a design example, assume V_{IN} = 6V, V_{OUT} = 5V, I_{MAX} = 400mA and f_{OSC} = 200kHz. With these requirements we can start choosing all of the important components.

With no frequency synchronization required, the LTC1433 can be used for this circuit. From Figure 2, the $V_{PLL\ LPF}$ = 0V curve is used to determine the value of the oscillator capacitor. From the graph a value of 50pF will provide the desired frequency.

Next the inductor value is selected. From the Maximum Output Current vs Input Supply graph in the Typical Performance Characteristics section, a value of L = 22μH would be able to meet the requirement for the output load current.

For the catch diode, a MBRS130LT3 is selected.

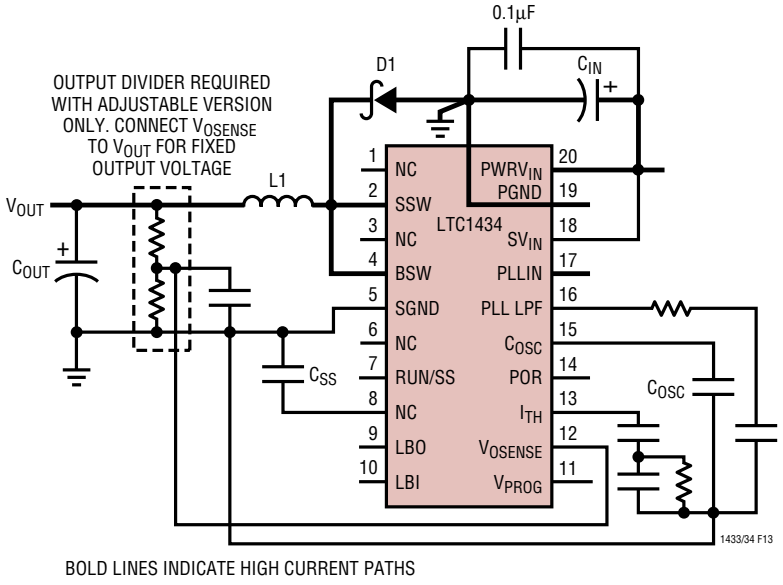


Figure 13. LTC1434 Layout Diagram (See Board Layout Check List)

APPLICATIONS INFORMATION

C_{IN} will require an RMS current rating of at least 0.2A at temperature and C_{OUT} will require an ESR of less than 0.25Ω. In most of the applications, the requirements for these capacitors are fairly similar.

Figure 14 shows the complete circuit along with its efficiency curve.

Latchup Prevention (Figure 15)

In applications where the input supply can momentarily dip below the output voltage, it is recommended that a Schottky diode (D2) be connected from V_{OUT} to V_{IN}. This diode will prevent the output capacitor from forward biasing the parasitic diode of the internal monolithic power MOSFET, preventing a large amount of current from flowing into the substrate to create a potential latchup condition.

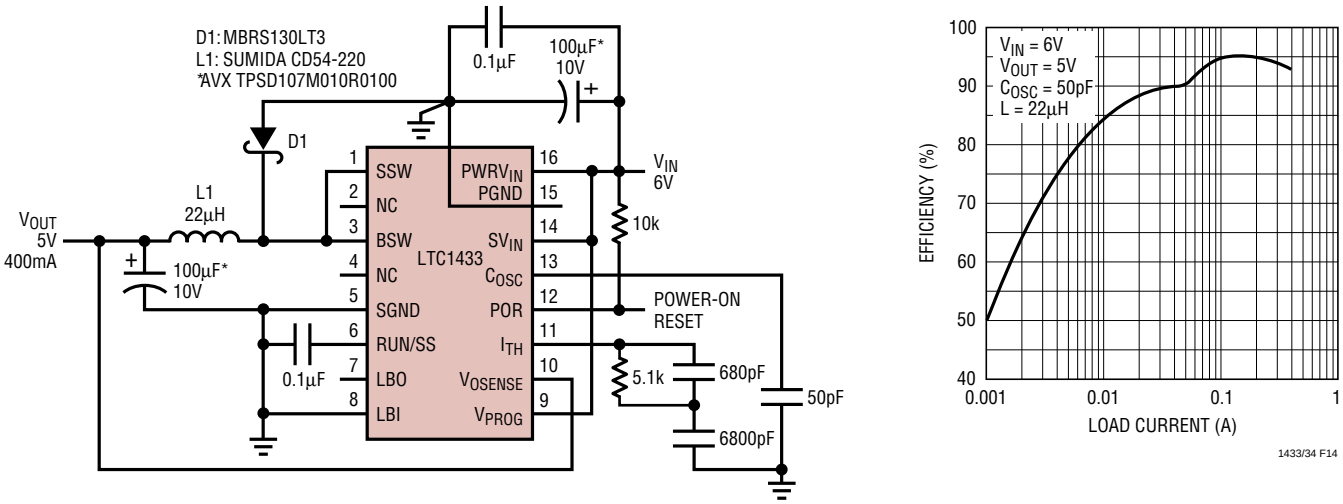


Figure 14. Design Example Circuit and its Efficiency Curve

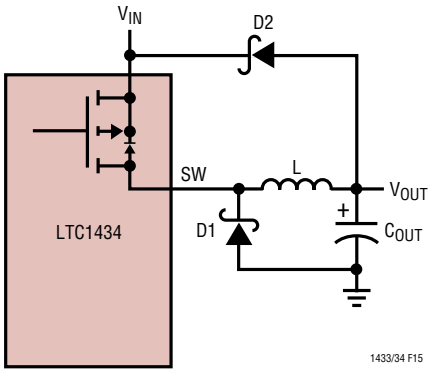
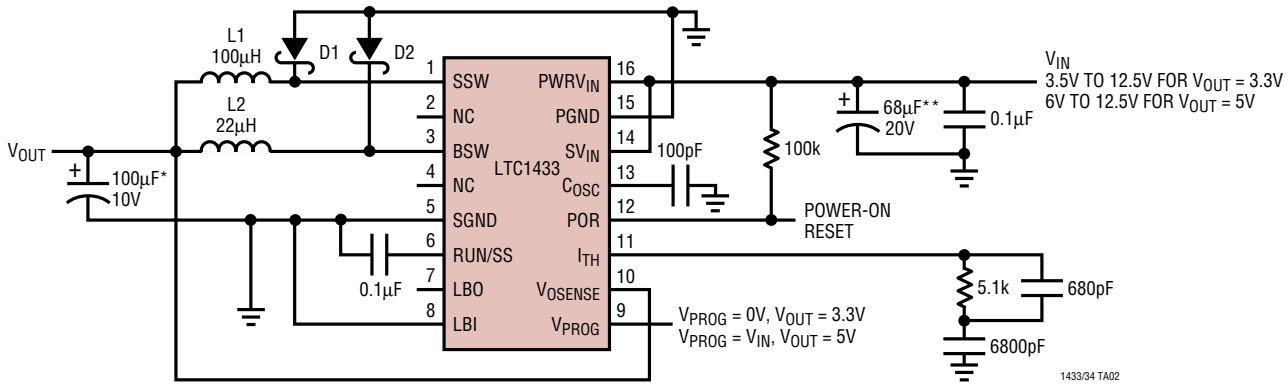


Figure 15

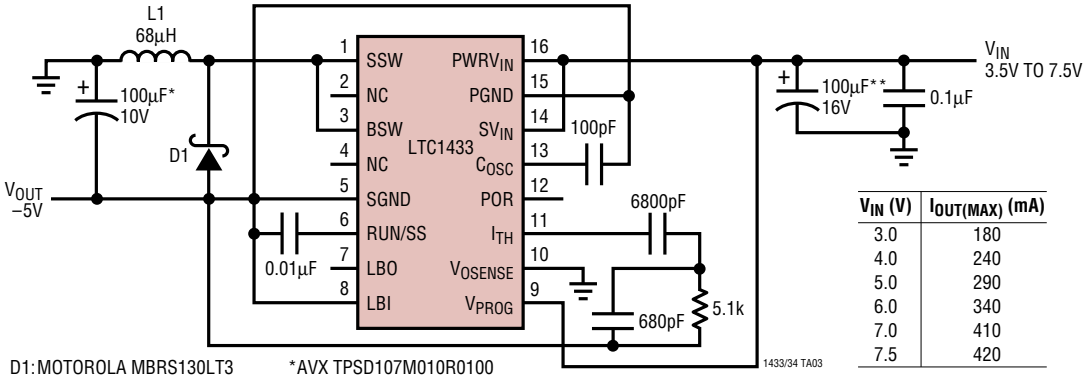
TYPICAL APPLICATIONS

Highest Efficiency 3.3V/5V Converter



D1: MOTOROLA MBRS0520LT3 *AVX TPSD107M010R0100
D2: MOTOROLA MBRS130LT3 ** AVX TPSE686M020R0150
L1: COILCRAFT DT1608C SERIES
L2: SUMIDA CD54 SERIES

Positive-to-Negative –5V Converter

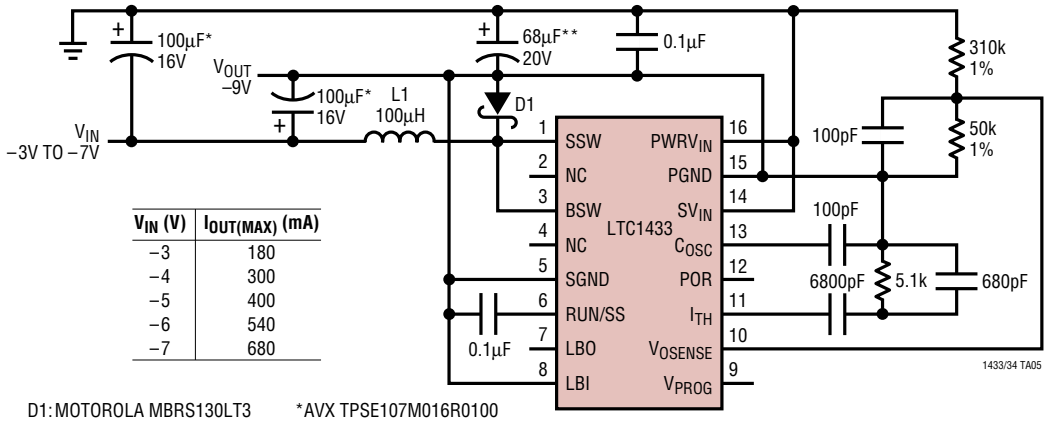


VIN (V)	IOUT(MAX) (mA)
3.0	180
4.0	240
5.0	290
6.0	340
7.0	410
7.5	420

D1: MOTOROLA MBRS130LT3 *AVX TPSD107M010R0100
L1: COILCRAFT DO3316 SERIES ** AVX TPSE107M016R0100

TYPICAL APPLICATIONS

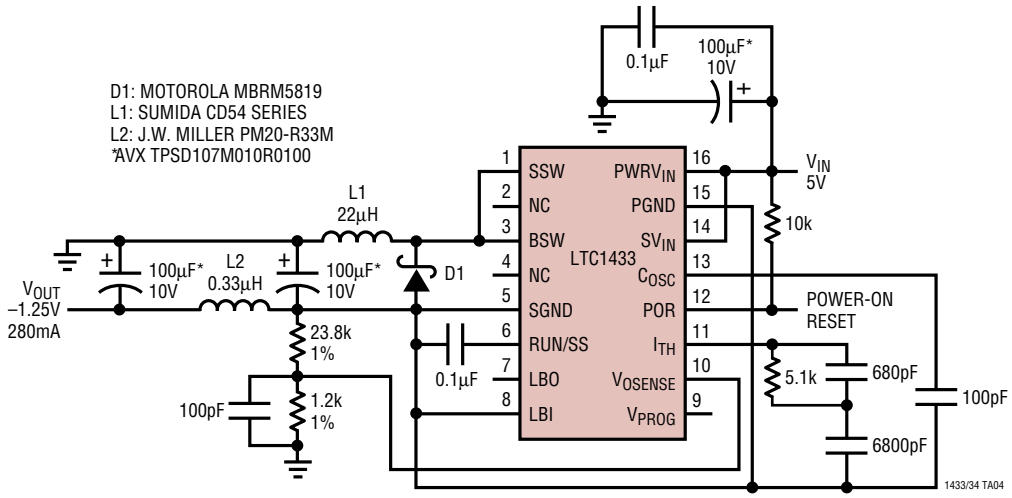
Negative Boost Converter



V_{IN} (V)	$I_{OUT(MAX)}$ (mA)
–3	180
–4	300
–5	400
–6	540
–7	680

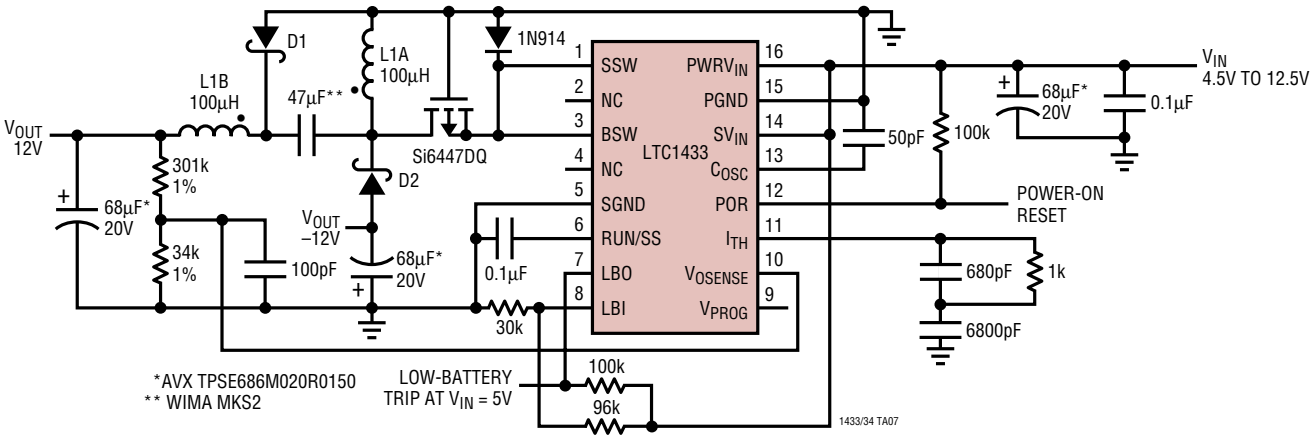
D1: MOTOROLA MBRS130LT3 *AVX TPSE107M016R0100
L1: COILCRAFT DO3316 SERIES ** AVX TPSE686M020R0150

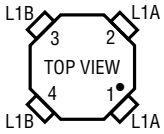
Ultralow Output Ripple 5V to –1.25V MR Head Amplifier Supply



TYPICAL APPLICATIONS

9V to 12V, –12V Outputs





D1, D2: MOTOROLA MBRS130LT3
L1A, L1B:

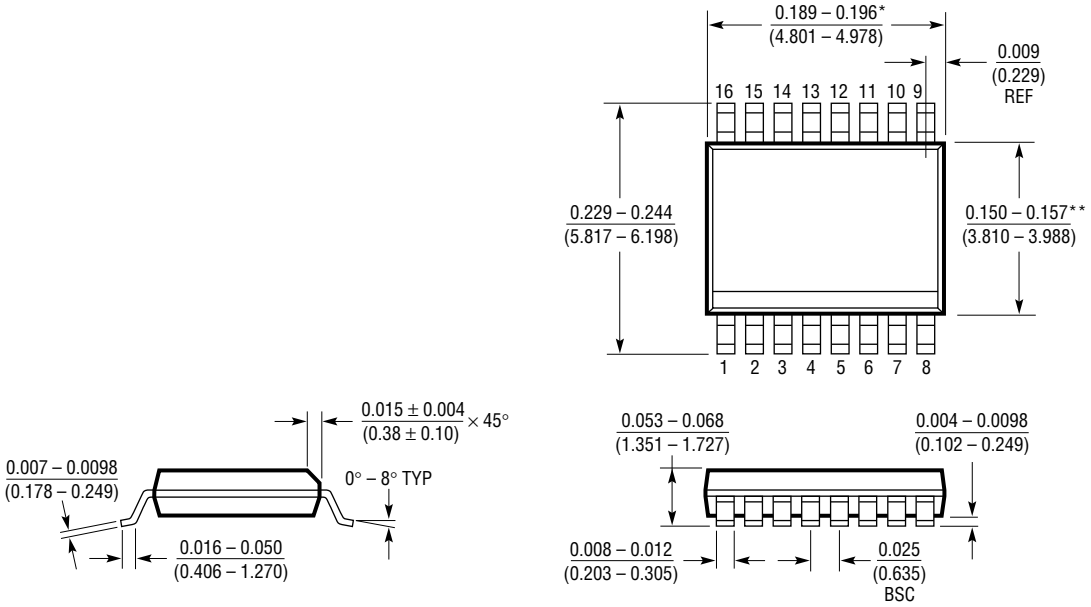
MANUFACTURER	PART NO.
COILTRONICS	CTX100-4
DALE	LPT4545-101LA

V_{IN} (V)	EACH OUTPUT $I_{OUT(MAX)}$ (mA)
4.5	50
5.0	60
6.0	70
7.0	100
8.0	110
9.0	130
10.0	145
11.0	160
12.0	200
12.5	205

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



GN16 (SSOP) 0398

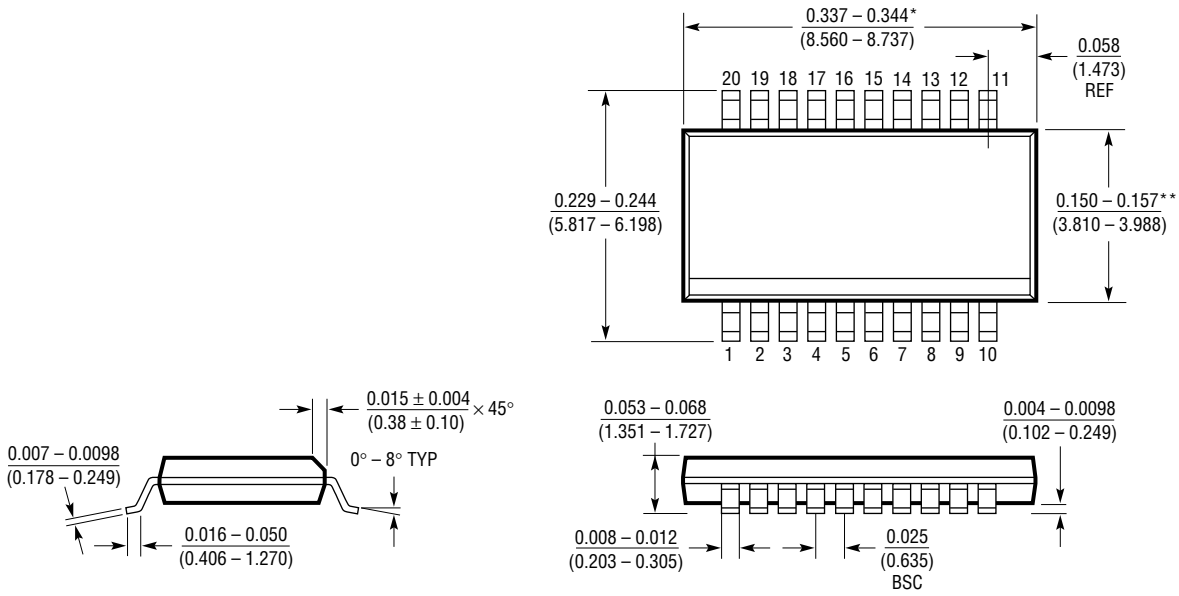
* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
20-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



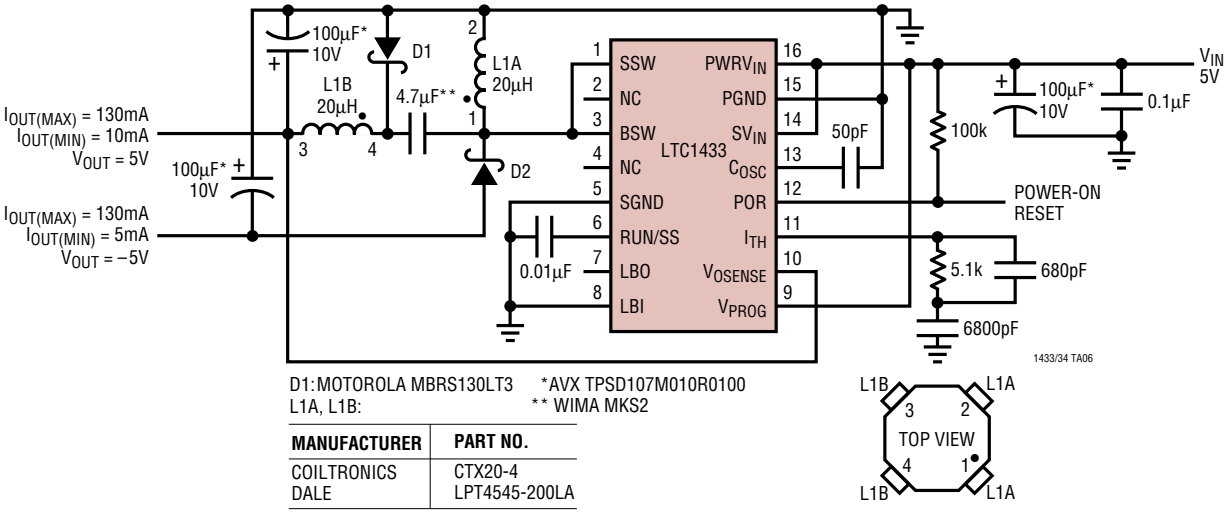
GN20 (SSOP) 0398

* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

5V to ±5V Outputs



D1: MOTOROLA MBRS130LT3 *AVX TPSD107M010R0100
L1A, L1B: ** WIMA MKS2

MANUFACTURER	PART NO.
COILTRONICS	CTX20-4
DALE	LPT4545-200LA

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1074/LT1076	Step-Down Switching Regulators	100kHz, 5A (LT1074) or 2A (LT1076) Internal Switch
LTC1174/LTC1174-3.3/ LTC1174-5	High Efficiency Step-Down and Inverting DC/DC Converters	Burst Mode™ Operation
LTC1265	1.2A High Efficiency Step-Down DC/DC Converter	Burst Mode Operation
LT1375/LT1376	1.5A, 500kHz Step-Down Switching Regulators	High Frequency, Small Inductor, High Efficiency Switchers, 1.5A Switch
LTC1474	High Efficiency Step-Down Converter	Low I_Q = 10µA, 8-Pin MSOP
LTC1435	High Efficiency Synchronous Step-Down Controller	16-Pin Narrow SO and SSOP
LTC1436/LTC1436-PLL	High Efficiency Low Noise Synchronous Step-Down Controllers	24-Pin Narrow and 28-Pin SSOP
LTC1438/LTC1439	Dual High Efficiency Low Noise Synchronous Step-Down Controllers	Up to Four Outputs Capability
LTC1538-AUX	Dual High Efficiency Synchronous Step-Down Controller	Auxiliary Linear Regulator 5V Standby in Shutdown
LTC1539	Dual High Efficiency Low Noise Synchronous Step-Down Controller	Auxiliary Linear Regulator 5V Standby in Shutdown
LTC1627	High Efficiency Monolithic Synchronous DC/DC Converter	Low Supply Voltage: 2.65V to 10V, 0.5A

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