

- **Center  $V_{CC}$  and GND Configuration**  
Provides Minimum Lead Inductance in High Current Switching Applications
- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses With Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High Impedance**
- **Package Options Include Plastic DIPs. Use the 'AS843 for Plastic and Ceramic Chip Carriers and "Small Outline" Package Options**
- **Dependable Texas Instruments Quality and Reliability**

#### description

This 9-bit latch device features three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

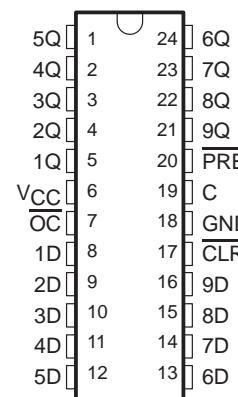
The nine latches are transparent D-type and have noninverting data (D) inputs.

A buffered output control ( $\overline{OC}$ ) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pullup components.

The output control ( $\overline{OC}$ ) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN74AS1843 is characterized for operation from 0°C to 70°C.

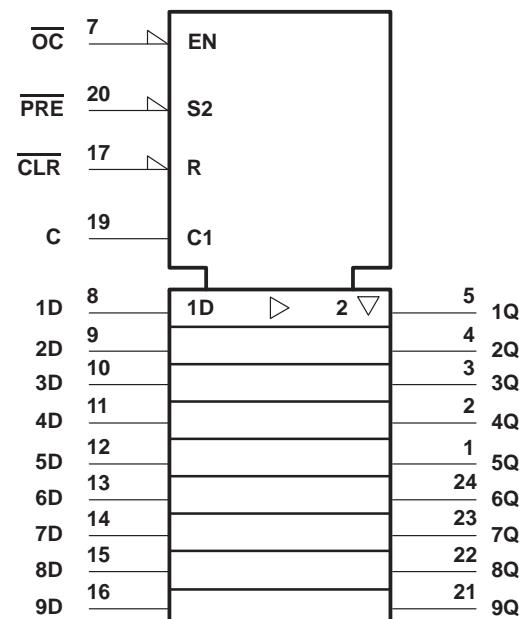
NT Package  
(Top View)



FUNCTION TABLE

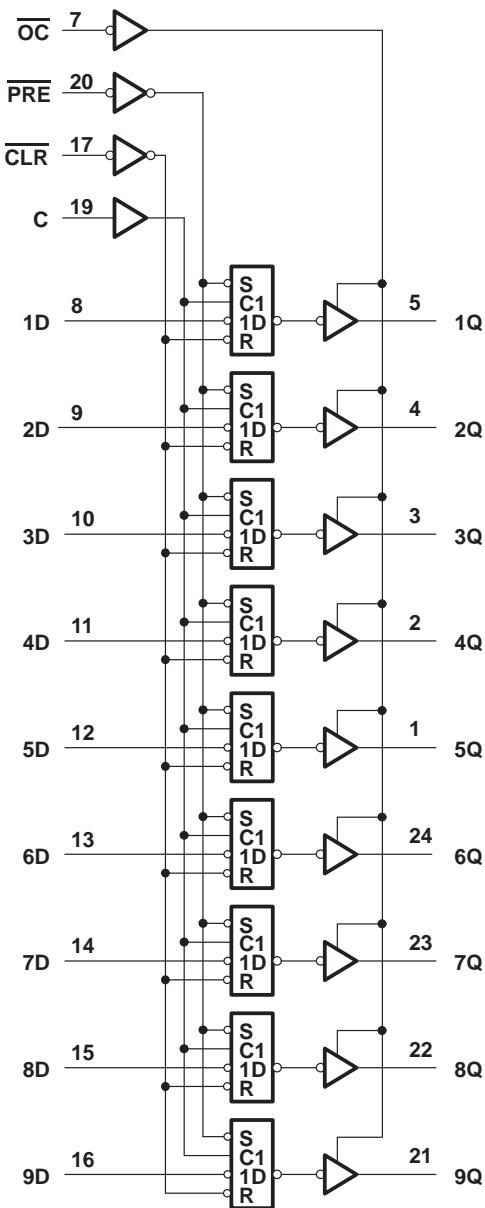
| INPUTS |     |                 |   |   | OUTPUT |
|--------|-----|-----------------|---|---|--------|
| PRE    | CLR | $\overline{OC}$ | C | D | Q      |
| L      | X   | L               | X | X | H      |
| H      | L   | L               | X | X | L      |
| H      | H   | L               | H | L | L      |
| H      | H   | L               | H | H | H      |
| H      | H   | L               | L | X | $Q_O$  |
| X      | X   | H               | X | X | Z      |

logic symbol †



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12,

## logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|  |                |
|--|----------------|
| Supply voltage, $V_{CC}$ (see Note 1) .....        | 7 V            |
| Input voltage .....                                | 7 V            |
| Voltage applied to a disabled 3-state output ..... | 5.5 V          |
| Operating free-air temperature range .....         | 0°C to 70°C    |
| Storage temperature range .....                    | -65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

**recommended operating conditions**

|          |                                    | MIN                         | NOM | MAX | UNIT |
|----------|------------------------------------|-----------------------------|-----|-----|------|
| $V_{CC}$ | Supply voltage                     | 4.5                         | 5   | 5.5 | V    |
| $V_{IH}$ | High-level input voltage           |                             | 2   |     | V    |
| $V_{IL}$ | Low-level input voltage            |                             |     | 0.8 | V    |
| $I_{OH}$ | High-level output current          |                             |     | -24 | mA   |
| $I_{OL}$ | Low-level output current           |                             |     | 48  | mA   |
| $t_w$    | Pulse duration, enable C high      | CLR or $\overline{PRE}$ low | 4   |     | ns   |
|          |                                    | C high                      | 4   |     |      |
| $t_{su}$ | Setup time, data before enable C ↓ |                             | 2.5 |     | ns   |
| $t_h$    | Hold time, data after enable C ↓   |                             | 2.5 |     | ns   |
| $t_r$    | Recovery time                      | $\overline{PRE}$            | 15  |     | ns   |
|          |                                    | CLR                         | 14  |     |      |
| $T_A$    | Operating free-air temperature     | 0                           |     | 70  | °C   |

**electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)**

| PARAMETER        | TEST CONDITIONS                     | MIN              | TYPT <sup>†</sup> | MAX   | UNIT |
|------------------|-------------------------------------|------------------|-------------------|-------|------|
| $V_{IK}$         | $V_{CC} = 4.5$ V, $I_I = -18$ mA    |                  |                   | -1.2  | V    |
| $V_{OH}$         | $V_{CC} = 4.5$ V, $I_{OH} = -2$ mA  | $V_{CC} - 2$     |                   |       | V    |
|                  | $V_{CC} = 4.5$ V, $I_{OH} = -15$ mA | 2.4              | 3.2               |       |      |
|                  | $V_{CC} = 4.5$ V, $I_{OH} = -24$ mA | 2                |                   |       |      |
|                  | $V_{CC} = 4.5$ V, $I_{OL} = 32$ mA  |                  |                   |       |      |
| $V_{OL}$         | $V_{CC} = 4.5$ V, $I_{OL} = 48$ mA  |                  | 0.35              | 0.5   | V    |
|                  | $V_{CC} = 4.5$ V, $I_{OL} = 48$ mA  |                  |                   |       |      |
| $I_{OZH}$        | $V_{CC} = 5.5$ V, $V_O = 2.7$ V     |                  |                   | 50    | µA   |
| $I_{OZL}$        | $V_{CC} = 5.5$ V, $V_O = 0.4$ V     |                  |                   | -50   | µA   |
| $I_I$            | $V_{CC} = 5.5$ V, $V_I = 7$ V       |                  |                   | 0.1   | mA   |
| $I_{IH}$         | $V_{CC} = 5.5$ V, $V_I = 2.7$ V     |                  |                   | 20    | µA   |
| $I_{IL}$         | $V_{CC} = 5.5$ V, $V_I = 0.4$ V     |                  |                   | -0.05 | mA   |
| $I_O^{\ddagger}$ | $V_{CC} = 5.5$ V, $V_O = 2.25$ V    | -30              |                   | -112  | mA   |
| $I_{CC}$         | $V_{CC} = 5.5$ V,                   | Output high      | 37                | 62    | mA   |
|                  |                                     | Output low       | 56                | 92    |      |
|                  |                                     | Outputs disabled | 56                | 92    |      |

<sup>†</sup> All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

**SN74AS1843****9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS**

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**switching characteristics over recommended ranges of supply voltage and free-air temperature (see Note 2)**

| PARAMETER | FROM<br>(INPUT)         | TO<br>(OUTPUT) | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$<br>$C_L = 50 \text{ pF},$<br>$R_1 = 500 \Omega,$<br>$R_2 = 500 \Omega,$<br>$T_A = \text{MIN to MAX}$ |      | UNIT |
|-----------|-------------------------|----------------|--|------|------|
|           |                         |                | MIN  | MAX  |      |
| $t_{PLH}$ | D                       | Q              | 1  | 6.5  | ns   |
| $t_{PHL}$ |                         |                | 1  | 9    |      |
| $t_{PLH}$ | C                       | Q              | 2  | 12   | ns   |
| $t_{PHL}$ |                         |                | 2  | 12   |      |
| $t_{PLH}$ | $\overline{\text{PRE}}$ | Q              | 2  | 10   | ns   |
| $t_{PHL}$ | $\overline{\text{CLR}}$ | Q              | 2  | 13   | ns   |
| $t_{PZH}$ | $\overline{\text{OC}}$  | Q              | 2  | 10.5 | ns   |
| $t_{PZL}$ |                         |                | 2  | 13.5 |      |
| $t_{PHZ}$ | $\overline{\text{OC}}$  | Q              | 1  | 8    | ns   |
| $t_{PLZ}$ |                         |                | 1  | 8    |      |

NOTE 2: Load circuit and voltage waveforms are shown in Section 1 of the *ALS/AS Logic Data Book, 1986*.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74AS1843NT     | OBsolete              | PDIP         | NT              | 24   |             | TBD                     | Call TI          | Call TI                      |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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