NOT RECOMMENDED FOR NEW DESIGN
USE DMP2101UCB9

Lead-free Green

DMP2100UCB9

DUAL P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary (Typ. @ V_{GS} = -4.5V, T_A = +25°C)

BV_{DSS}	$R_{DS(ON)}$	Q_g	Q_{gd}	I_D
-20V	80mΩ	3.3nC	0.6nC	-4A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{D1D2(ON)}$) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

Applications

- Battery Management
- Load Switch
- Battery Protection

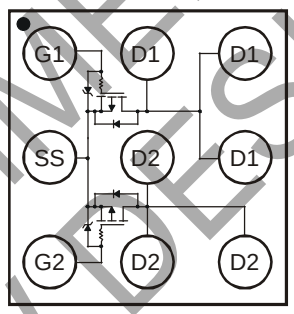
Features and Benefits

- LD-MOS Technology with the Lowest Figure of Merit:
  $R_{DS(ON)}$ = 80mΩ to Minimize On-State Losses
  Q_g = 3.3nC for Ultra-Fast Switching
- $V_{gs(th)}$ = -0.7V Typ. for a Low Turn-On Potential
- CSP with Footprint 1.5mm × 1.5mm
- Height = 0.62mm for Low Profile
- ESD = 3kV HBM Protection of Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: U-WLB1515-9
- Terminal Connections: See Diagram Below
- Weight: 0.0018 grams (Approximate)

ESD PROTECTED TO 3kV



Top View

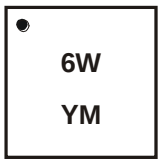
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP2100UCB9-7	U-WLB1515-9	3000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

U-WLB1515-9



6W = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: F = 2018)
M = Month (ex: 9 = September)

Date Code Key

Year	2015	2016	2017	2018	2019	2020	2021
Code	C	D	E	F	G	H	I

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{D1D2}	-20	V
Gate-Source Voltage			V_{GS}	-6	V
Continuous Drain Current (Note 5) V_{GS} = -4.5V	Steady State	T_C = +25°C T_C = +70°C	I_{D1D2}	-3.0 -2.1	A
Continuous Drain Current (Note 6) V_{GS} = -4.5V	Steady State	T_C = +25°C T_C = +70°C	I_{D1D2}	-4.0 -3.0	A
Continuous Source Pin Current (Note 6)			I_S	-2.0	A
Continuous Gate Clamp Current (Note 6)			I_G	-0.4	A
Pulsed Source Pin Current (Pulse Duration 10µs, Duty Cycle ≤ 1%)			I_{SM}	-15	A
Pulsed Drain Current (Pulse Duration 10µs, Duty Cycle ≤ 1%)			I_{DM}	-28	A
Pulsed Gate Clamp Current (Pulse Duration 10µs, Duty Cycle ≤ 1%)			I_{GM}	-6	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	0.8	W
Total Power Dissipation (Note 6)	P_D	1.6	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	152	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	65	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{D1D2}	-20	—	—	V	V_{GS} = 0V, I_{D1D2} = -250µA
Gate-Source Breakdown Voltage	BV_{GSS}	-6.1	—	—	V	I_{GS} = -250µA, V_{D1D2} = 0V
Zero Gate Voltage Drain Current @T_C = +25°C	I_{DDS}	—	—	-1	µA	V_{D1D2} = -16V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	-100	nA	V_{GS} = -6V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.4	-0.7	-0.9	V	V_{D1D2} = V_{GS}, I_{DS} = -250µA
Static Drain-Source On-Resistance	$R_{D1D2(ON)}$	—	80	100	mΩ	V_{GS} = -4.5V, I_{D1D2} = -1A
		—	105	130		V_{GS} = -2.5V, I_{D1D2} = -1A
		—	140	175		V_{GS} = -1.8V, I_{D1D2} = -1A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	5.3	—	S	V_{D1D2} = -10V, I_{D1D2} = -1A
DIODE CHARACTERISTICS						
Diode Forward Voltage (Note 6)	V_{SD}	—	-0.7	-1	V	V_{GS} = 0V, I_{D1D2} = -1A
Reverse Recovery Charge	Q_{rr}	—	18	—	nC	V_{dd} = -9.5V, I_F = -1A, di/dt = 200A/µs
Reverse Recovery Time	t_{rr}	—	34	—	ns	
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	232	310	pF	V_{D1D2} = -10V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	107	150	pF	
Reverse Transfer Capacitance	C_{rss}	—	43.5	55	pF	
Total Gate Charge	Q_g	—	3.3	4.2	nC	V_{GS} = -4.5V, V_{D1D2} = -10V, I_{D1D2} = -1A
Gate-Source Charge	Q_{gs}	—	0.3	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.6	—	nC	
Gate Charge at V_{th}	$Q_{g(th)}$	—	0.2	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	8.5	—	ns	V_{D1D2} = -10V, V_{GS} = -4.5V, I_{D1D2} = -1A, R_G = 30Ω
Turn-On Rise Time	t_R	—	7.0	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	47	—	ns	
Turn-Off Fall Time	t_F	—	28	—	ns	

Notes: 5. Device mounted on FR-4 PCB with minimum recommended pad layout.
6. Device mounted on FR-4 material with 1-inch^2(6.45-cm^2), 2-oz. (0.071-mm thick) Cu.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

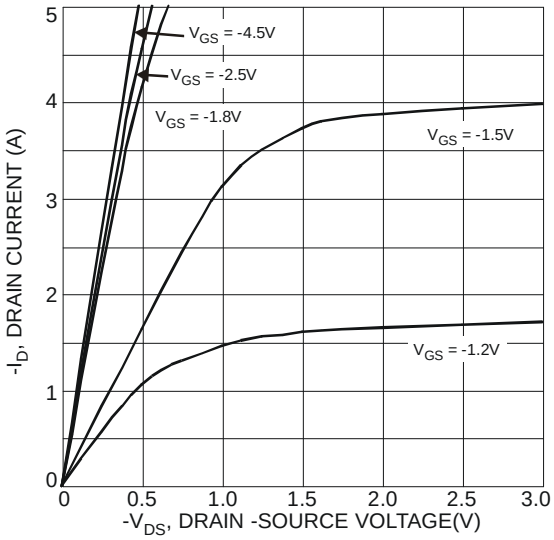


Fig. 1 Typical Output Characteristics

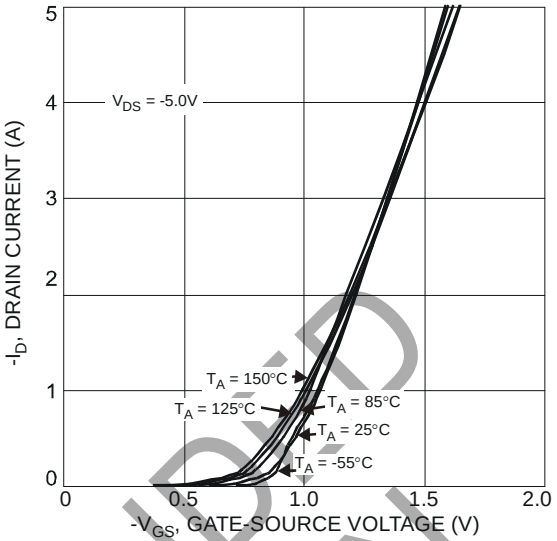


Fig. 2 Typical Transfer Characteristics

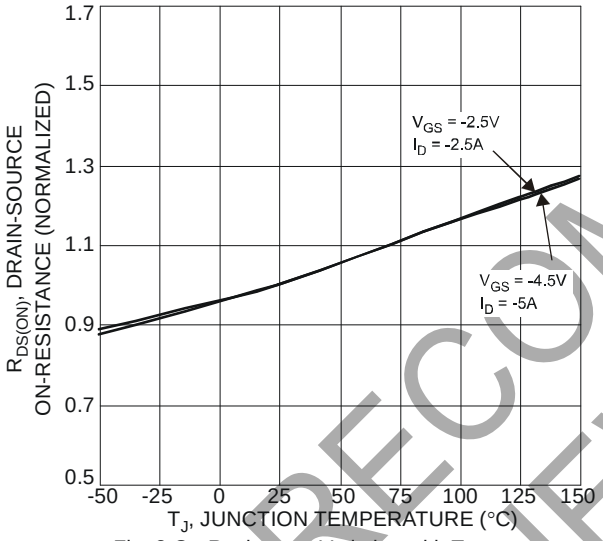


Fig. 3 On-Resistance Variation with Temperature

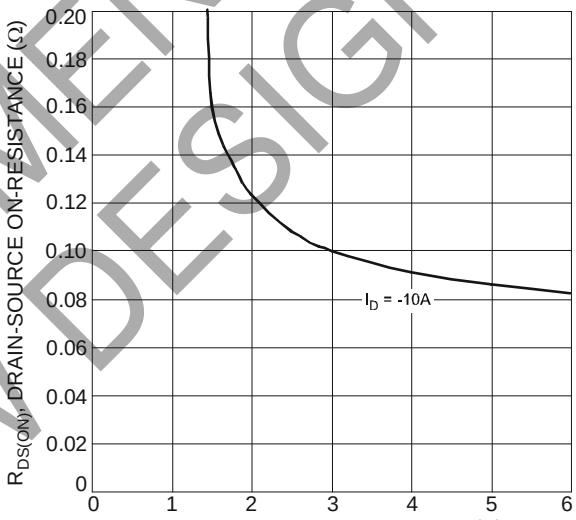


Fig. 4 Typical On-Resistance vs. Drain Current and Gate Voltage

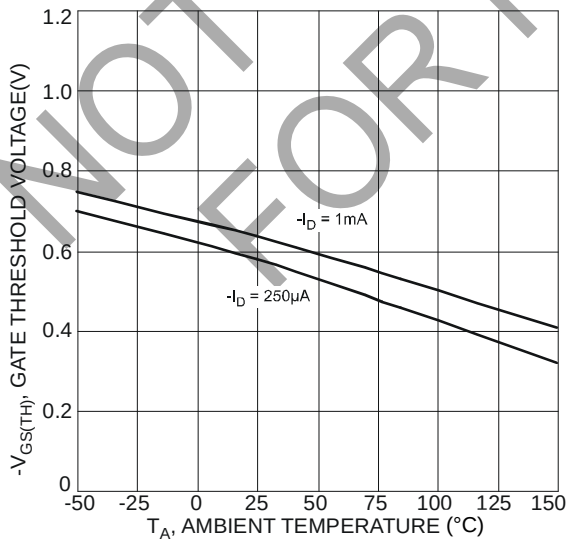


Fig. 5 Gate Threshold Variation vs. Ambient Temperature

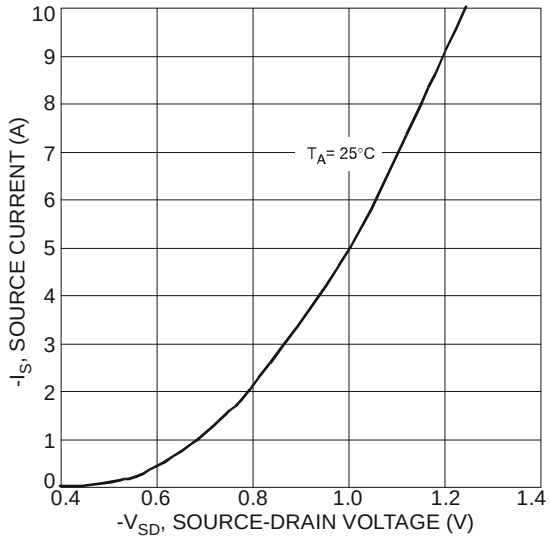


Fig. 6 Diode Forward Voltage vs. Current

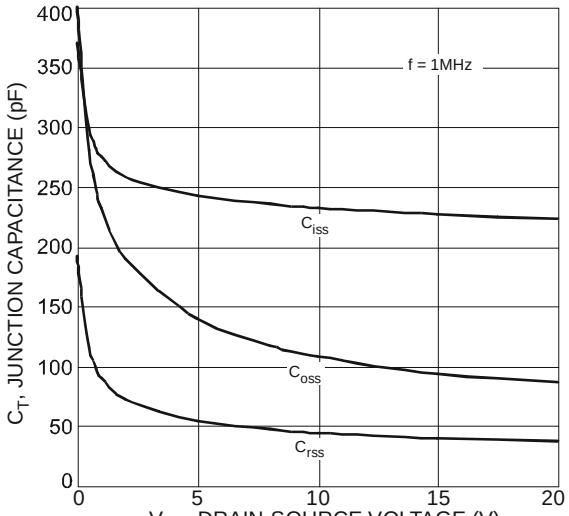


Fig. 7 Typical Junction Capacitance

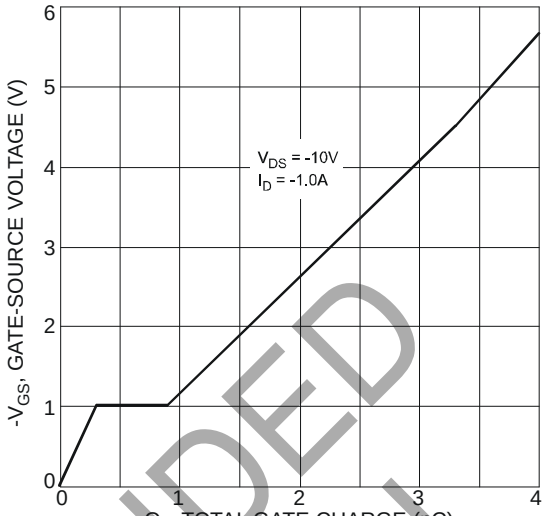


Fig. 8 Gate-Charge Characteristics

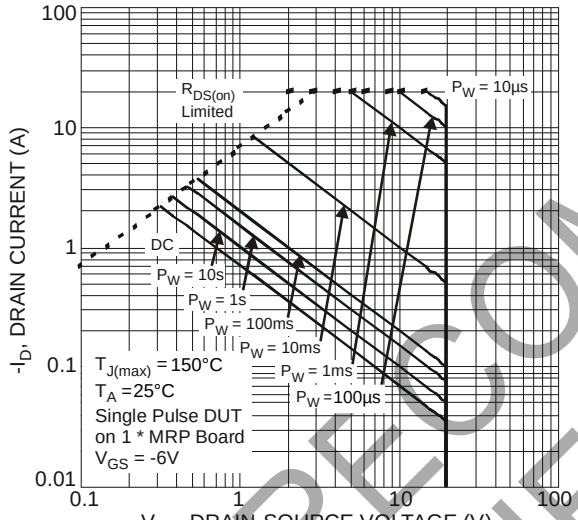


Fig. 9 SOA, Safe Operation Area

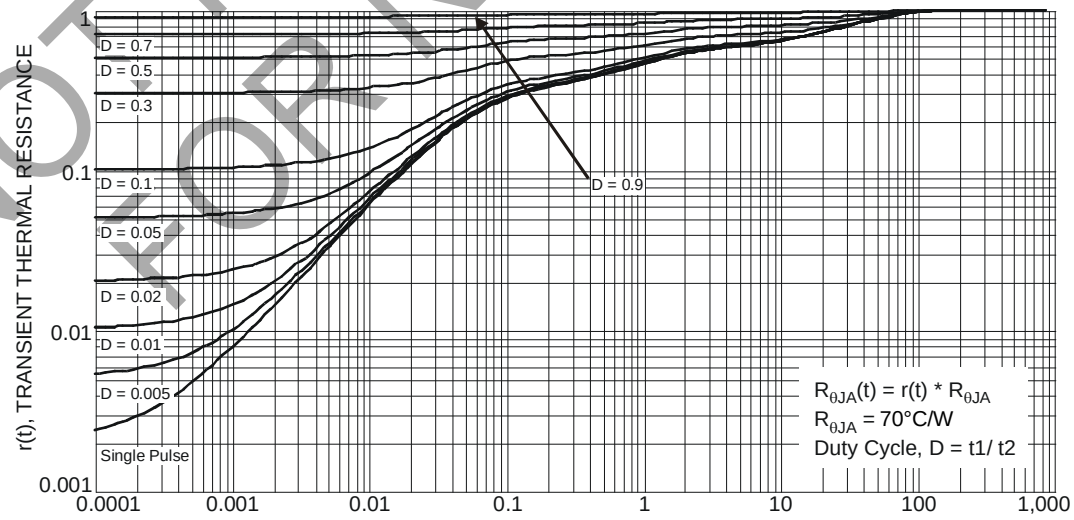
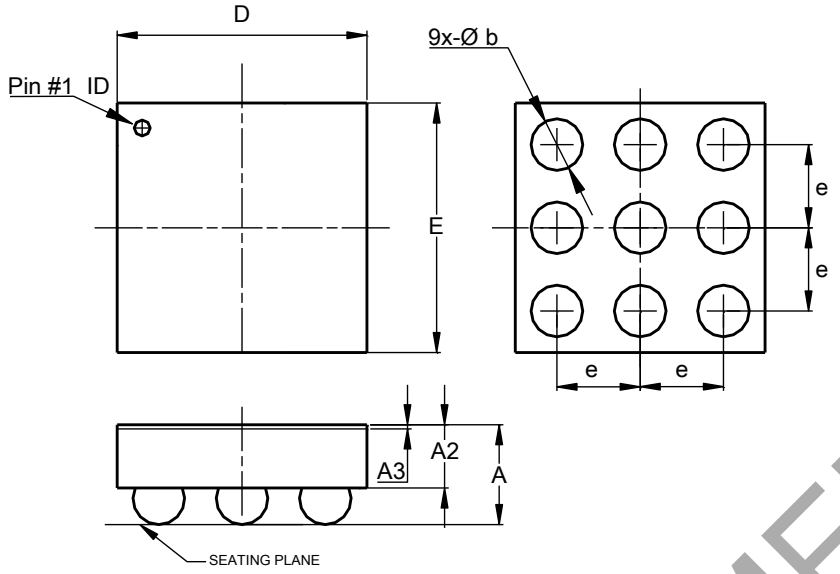


Fig. 10 Transient Thermal Resistance

Package Outline Dimensions

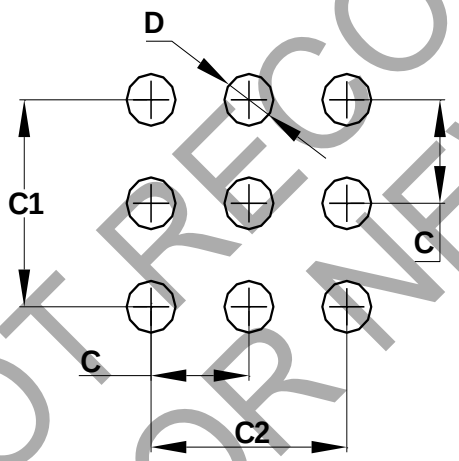
Please see http://www.diodes.com/package-outlines.html for the latest version.



U-WLB1515-9			
Dim	**Min**	**Max**	**Typ**
A	--	0.62	--
A2	--	0.36	0.36
A3	0.020	0.030	0.025
b	0.27	0.37	0.32
D	1.47	1.50	1.49
E	1.47	1.50	1.49
e	--	--	0.50
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.



Dimensions	Value (in mm)
C	0.50
C1	1.00
C2	1.00
D	0.25

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