

General Description

HX3 is a family of USB 3.0 hub controllers compliant with the USB 3.0 specification revision 1.0. HX3 supports SuperSpeed (SS), Hi-Speed (HS), Full-Speed (FS), and Low-Speed (LS) on all the ports. It has integrated termination, pull-up, and pull-down resistors, and supports configuration options through pin-straps to reduce the overall BOM of the system.

HX3 includes the following Cypress-proprietary features:

Shared Link™: Enables extra downstream (DS) ports for on-board connections in embedded applications

Ghost Charge™: Enables charging of devices connected to the DS ports when no host is connected on the upstream (US) port

Features

USB 3.0-Certified Hub, TID# 330000047

Supports up to Four USB 3.0-Compliant DS ports

- All ports support SS (5 Gbps), and are backward-compatible with HS (480 Mbps), FS (12 Mbps), and LS (1.5 Mbps)
- SS and USB 2.0 Link Power Management (LPM)
- Dedicated Hi-Speed Transaction Translators (Multi-TT)
- LED status indicators – suspend, SS, and USB 2.0 operation

Shared Link™ for Embedded Applications

- Each DS port can simultaneously connect to an embedded SS device and a removable USB 2.0 device
- Enables up to eight device connections

Enhanced Battery Charging

- Each DS port complies with the USB Battery Charging v1.2 (BC v1.2) specification
- Ghost Charge™: Each DS port can emulate a Dedicated Charging Port (DCP) when the host is not connected to the US port
- Accessory Charger Adapter Dock (ACA-Dock): Enables charging and simultaneous data transfer for a smart phone or a tablet acting as a host compliant to BC v1.2
- Apple charging supported on all DS ports

Integrated ARM® Cortex™-M0 CPU

- 16 KB RAM, 32 KB ROM
- Configure GPIOs for overcurrent protection, power enable, and LEDs
- Upgrade firmware using (a) I²C EEPROM or (b) an external I²C master

Vendor-Command Support to Implement a USB-to-I²C Bridge

- Firmware upgrade of an external ASSP connected to HX3 through USB
- In-System Programming (ISP) of the EEPROM connected to HX3 through USB

Extensive Configuration Support

- Pin-strap configuration for the following functions:
 - Vendor ID (VID)
 - Charging support for each DS port
 - Number of active ports
 - Number of non-removable devices
 - Ganged or individual power switch enables for DS ports
 - Power switch polarity selection
- Custom configuration modes supported with eFuse, I²C EEPROM, or I²C slave
 - SS and USB 2.0 PHY parameters
 - Product ID (PID)/VID, manufacturer, and product string descriptors
 - Swap DP/DM signals for flexible PCB routing

Software Features

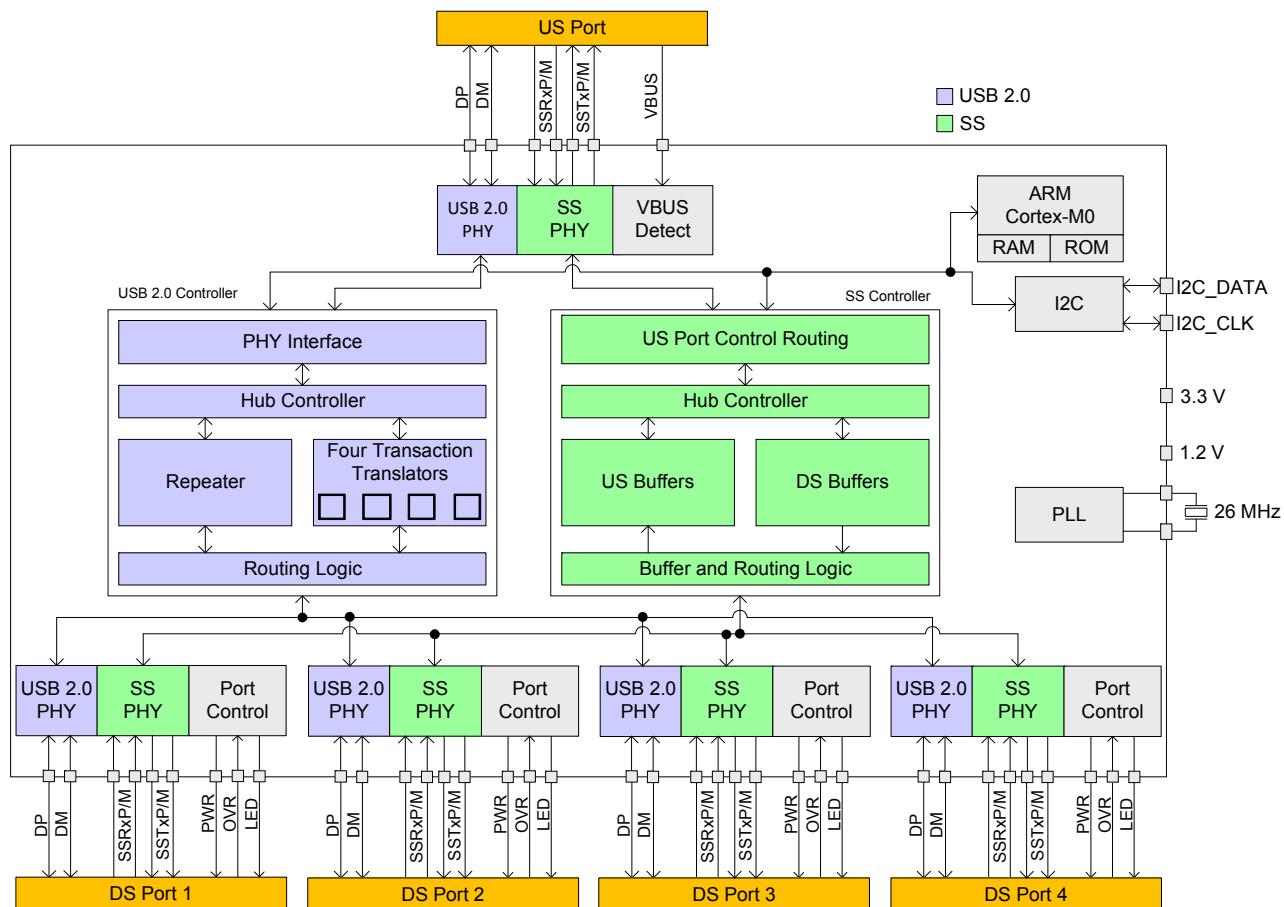
- Microsoft WHQL-certified for Windows XP/Vista/7/8/8.1
- Compatible with Mac OS 10.9 and Linux kernel version 3.11
- Customize configuration parameters with the easy-to-use Cypress's "Blaster Plus" software tool

Flexible Packaging Options

- 68-pin QFN (8 × 8 × 1.0 mm)
- 88-pin QFN (10 × 10 × 1.0 mm)
- Industrial temperature range (–40 °C to +85 °C)

Errata: For information on silicon errata, see [Errata on page 30](#). Details include trigger conditions, devices affected, and proposed workaround.

Block Diagram



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Architecture Overview

The [Block Diagram on page 2](#) shows the HX3 architecture. HX3 consists of two independent hub controllers (SS and USB 2.0), the Cortex-M0 CPU subsystem, an I²C interface, and port controller blocks.

SS Hub Controller

This block supports the SS hub functionality based on the USB 3.0 specification. The SS hub controller supports the following:

- SS link power management (U0, U1, U2, U3 states)
- Full-duplex data transmission

USB 2.0 Hub Controller

This block supports the LS, FS, and HS hub functionalities. It includes the repeater, frame timer, and four transaction translators.

The USB 2.0 hub controller block supports the following:

- USB 2.0 link power management (L0, L1, L2, L3 states)
- Suspend, resume, and remote wake-up signaling
- Multi-TT (one TT for each DS port)

CPU

The ARM Cortex-M0 CPU subsystem is used for the following functions:

- System configuration and initialization
- Battery charging control
- Vendor-specific commands for the USB-to-I²C bridge
- String-descriptor support
- Suspend status indicator
- Shared Link support in embedded systems

I²C Interface

The I²C interface in HX3 supports the following:

- I²C Slave, Master, and Multi-master configurations
 - Configure HX3 by an external I²C master in I²C slave mode
 - Configure HX3 from an I²C EEPROM
 - Multi-master mode to share EEPROM with other I²C masters
- In-System Programming of the I²C EEPROM from HX3's US port

Port Controller

The port controller block controls DS port power to comply with the BC v1.2 and USB 3.0 specifications. This block also controls the US port power in the ACA-Dock mode. Control signals for external power switches are implemented within the chip. HX3 controls the external power switches at power-on to reduce in-rush current.

The port controller block supports the following:

- Overcurrent detection
- SS and USB 2.0 port indicators for each DS port
- Ganged and individual power control modes
- Automatic port numbering based on active ports

Applications

- Standalone hubs
- PC and tablet motherboards
- Docking station
- Hand-held cradles
- Monitors
- Digital TVs
- Set-top boxes
- Printers

Table 1. HX3 Product Options

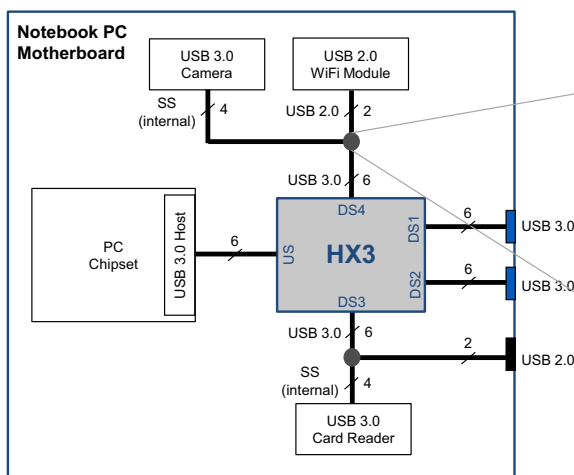
Features	CYUSB3302	CYUSB3304	CYUSB3312	CYUSB3314	CYUSB3326	CYUSB3328
Number of DS ports	2 (USB 3.0)	4 (USB 3.0)	2 (USB 3.0)	4 (USB 3.0)	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	8 (4 SS, 4 USB 2.0)
Number of Shared Link ports	0	0	0	0	2	4
BC v1.2	Yes	Yes	Yes	Yes	Yes	Yes
ACA-Dock	No	No	No	No	No	Yes
External Power Switch Control	Ganged	Ganged	Individual and Ganged	Individual and Ganged	Individual	Individual
Pin-Strap support	No	No	Yes	Yes	Yes	Yes
I ² C	Yes	Yes	Yes	Yes	Yes	Yes
Vendor command	Yes	Yes	Yes	Yes	Yes	Yes
Port indicators	No	No	Yes	Yes	No	No
Packages	68-QFN	68-QFN	88-QFN	88-QFN	88-QFN	88-QFN
Temperature range	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial

Product Features

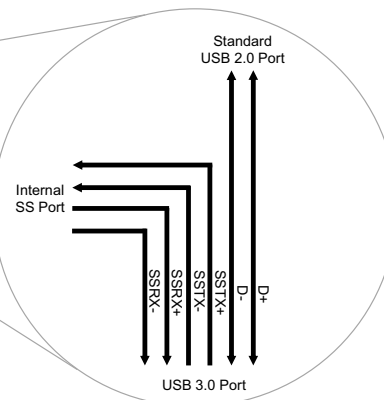
Shared Link

Figure 1. Application of Shared Link in a Notebook

Example: Shared Link Provides Six USB Ports in a Notebook



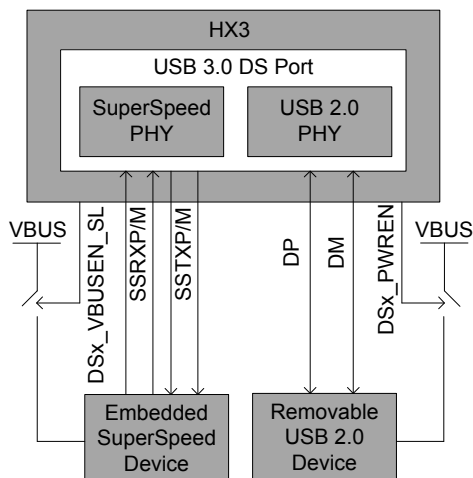
USB 3.0 Port Split Into SS Port and Standard USB 2.0 Port



Shared Link is a Cypress-proprietary feature that enables a USB 3.0 port to be split into an embedded SS port and a standard USB 2.0 port. Shared Link enables a maximum of eight DS ports from a four-port USB 3.0 hub.

For example, if one of the DS ports is connected to an embedded SS device, such as a USB 3.0 camera, HX3 enables the system designer to reuse the USB 2.0 signals of that specific port to connect to a standard USB 2.0 device. [Figure 1](#) shows how Shared Link can be used in an application.

Figure 2. DS Port VBUS Control in Shared Link



The Shared Link mode requires a separate VBUS control for the USB 2.0 device and the embedded SS device. [Figure 2](#) shows the VBUS control implementation.

To ensure that the embedded SS device does not fall back to USB 2.0 operation, an external power switch is required. This

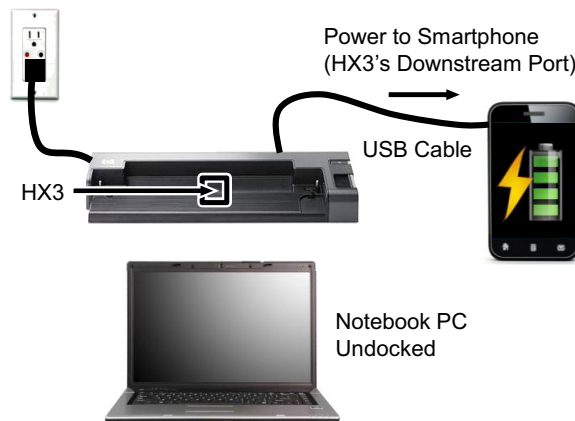
switch is controlled by HX3, which generates an output signal called DSx_VBUSEN_SL. This signal resets the VBUS for the embedded device.

DSx_PWREN is another output signal generated by HX3 and controls VBUS for the removable USB 2.0 device. For example, when an overcurrent condition occurs, DSx_PWREN turns off the port power.

Ghost Charge

Ghost Charge is a Cypress-proprietary feature for charging USB devices on the DS port when the US port is not connected to a host. For example, in a docking station with HX3 as shown in [Figure 3](#), when the laptop is undocked, HX3 will emulate a dedicated charging port (DCP) to provide charge to a phone connected on a DS port.

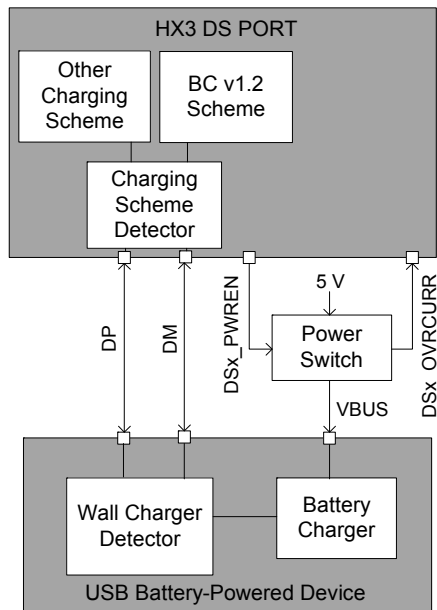
Figure 3. Ghost Charge



Charge a smartphone without docking the notebook

When the US port is disconnected from the host, HX3 detects if any of the DS ports are connected to a device requesting charging. It determines the charging method and then switches to the appropriate signaling based on the detected charging specification as shown in Figure 4. The hub either emulates a USB-compliant dedicated charging port by connecting DP and DM (see the BC v1.2 specification) or other supported proprietary charging schemes.

Figure 4. Ghost Charge Implementation in HX3



Ghost Charge is enabled by default and can be disabled through configuration. Refer to [Configuration Options on page 17](#).

Vendor-Command Support

HX3 supports vendor-specific requests and can also enumerate as a vendor-specific device. The vendor-specific request can be used to (a) bridge USB and I²C and (b) configure HX3. This feature can be used for the following applications:

- Firmware upgrade of an external ASSP connected to HX3 through USB
- In-System programming (ISP) of an EEPROM connected to HX3 through USB

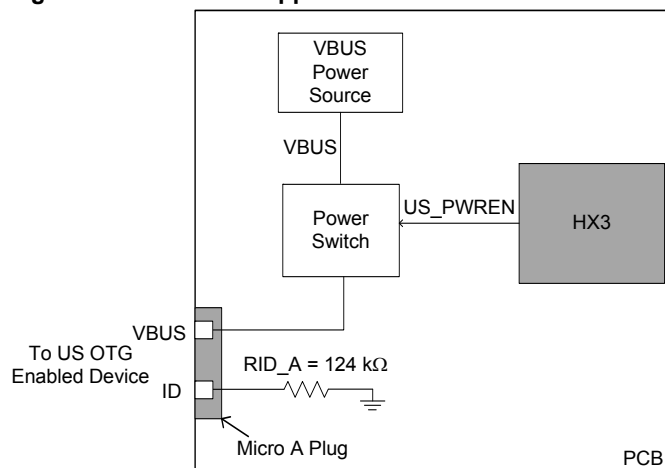
ACA-Dock Support

In traditional USB topologies, the host provides VBUS to enable and charge the connected devices. For OTG hosts, however, an ACA-Dock provides VBUS and a method to charge the host. HX3 supports the ACA-Dock standard (see BC v1.2 specification) by integrating the functions of the adapter controller.

Figure 5 shows the ACA-Dock system. If the ACA-Dock feature is enabled, HX3 turns on the external power switch to drive VBUS on the US port. To inform that the OTG host is connected to an ACA-Dock, the ID pin is tied to ground using a resistor RID_A, as shown in Figure 5. The ACA-Dock feature can be disabled using the [Configuration Options on page 17](#).

For example, a BC v1.2 compliant phone such as a Sony Xperia (neo V) can be docked to a HX3-based ACA-Dock system. The phone acts as an OTG host and the ACA-Dock charges the phone connected to the US port while also powering the four DS ports.

Figure 5. ACA-Dock Support



Pin Information

Figure 6. HX3 68-Pin QFN 2-Port Pinout

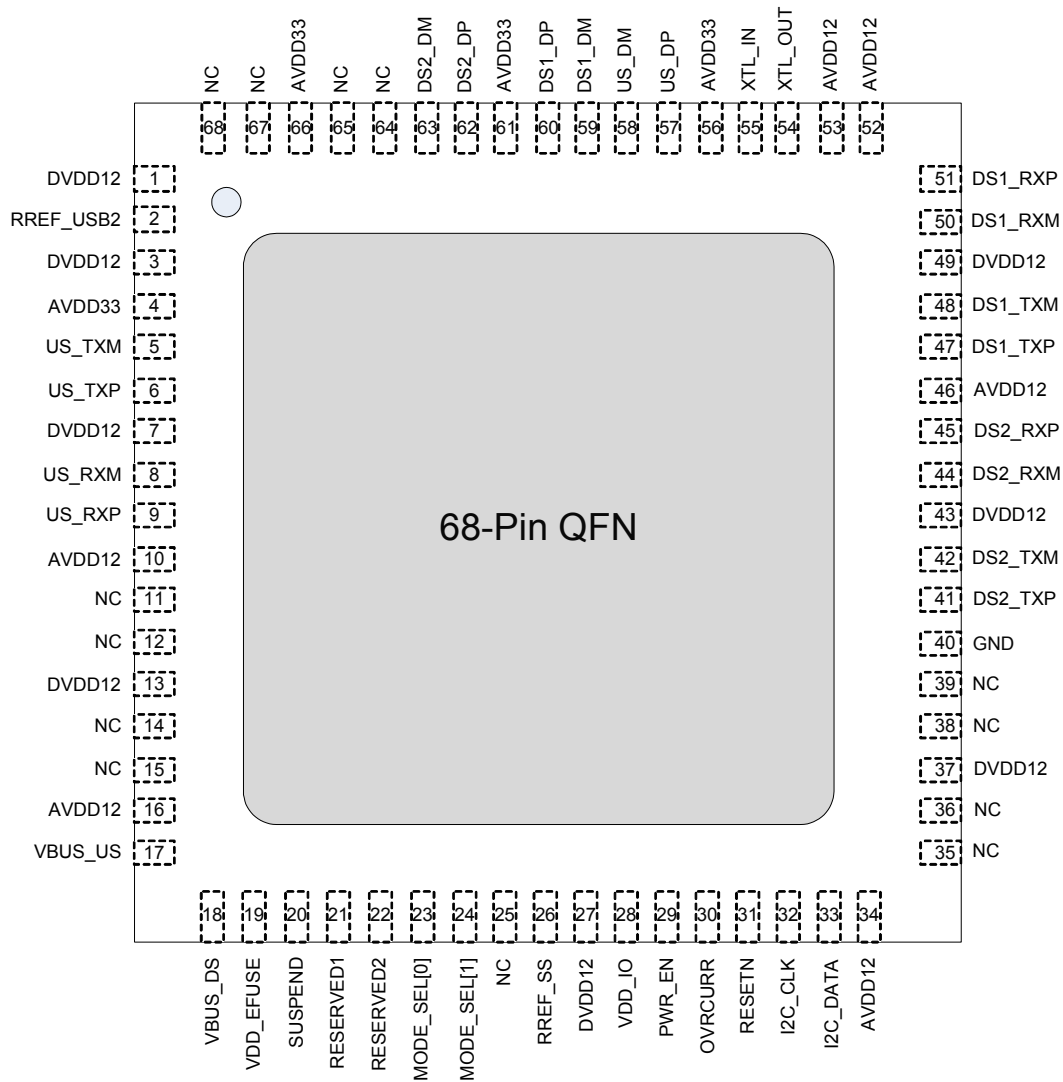


Figure 7. HX3 68-Pin QFN 4-Port Pinout

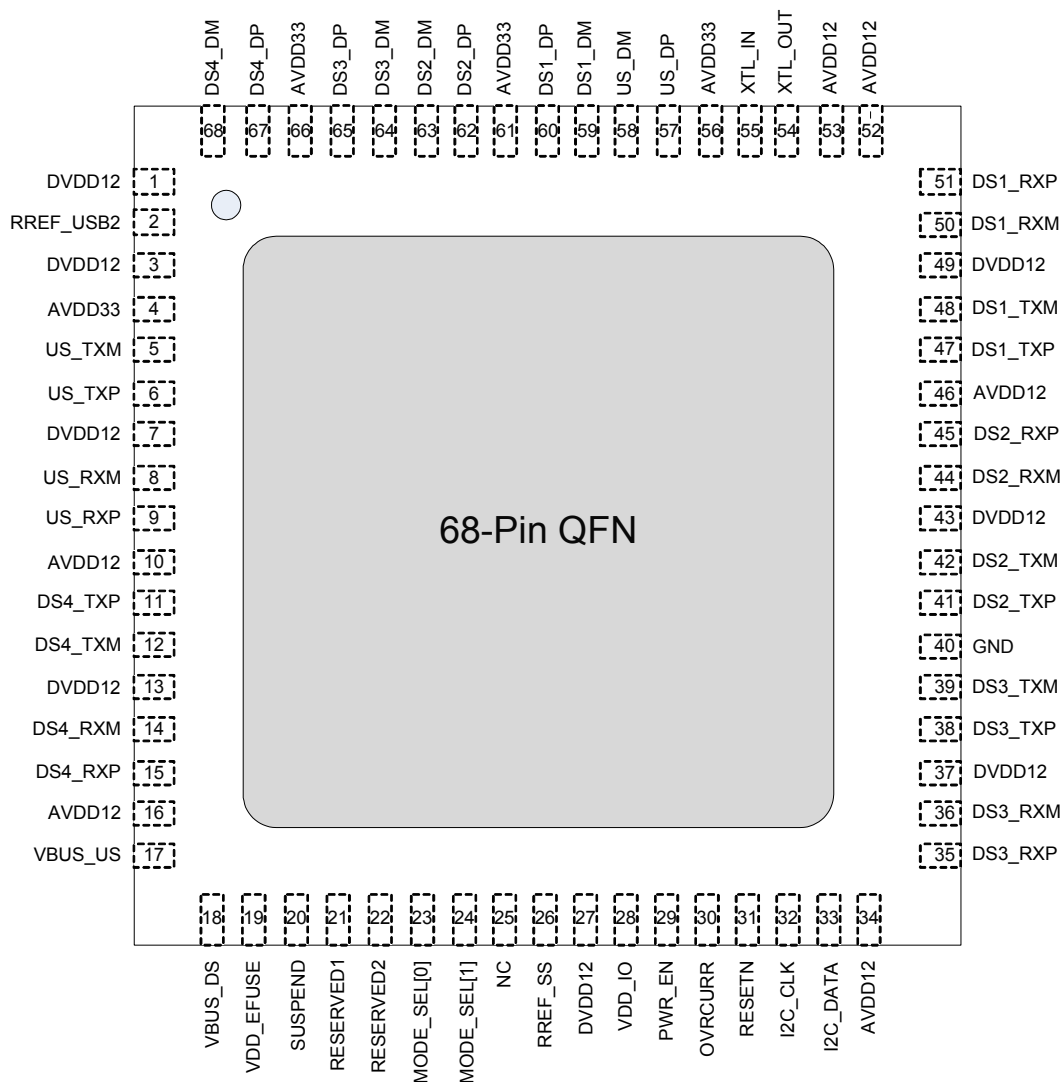


Table 2. 68-Pin QFN Pinout

Pin Name		Type	Pin#	Description
CYUSB3302	CYUSB3304			
US Port				
US_RXP		I	9	SuperSpeed receive plus
US_RXM		I	8	SuperSpeed receive minus
US_TXP		O	6	SuperSpeed transmit plus
US_TXM		O	5	SuperSpeed transmit minus
US_DP		I/O	57	USB 2.0 data plus
US_DM		I/O	58	USB 2.0 data minus
DS1 Port				
DS1_RXP		I	51	SuperSpeed receive plus
DS1_RXM		I	50	SuperSpeed receive minus
DS1_TXP		O	47	SuperSpeed transmit plus
DS1_TXM		O	48	SuperSpeed transmit minus
DS1_DP		I/O	60	USB 2.0 data plus
DS1_DM		I/O	59	USB 2.0 data minus
DS2 Port				
DS2_RXP		I	45	SuperSpeed receive plus
DS2_RXM		I	44	SuperSpeed receive minus
DS2_TXP		O	41	SuperSpeed transmit plus
DS2_TXM		O	42	SuperSpeed transmit minus
DS2_DP		I/O	62	USB 2.0 data plus
DS2_DM		I/O	63	USB 2.0 data minus
DS3 Port				
NC	DS3_RXP	I	35	SuperSpeed receive plus
NC	DS3_RXM	I	36	SuperSpeed receive minus
NC	DS3_TXP	O	38	SuperSpeed transmit plus
NC	DS3_TXM	O	39	SuperSpeed transmit minus
NC	DS3_DP	I/O	65	USB 2.0 data plus
NC	DS3_DM	I/O	64	USB 2.0 data minus
DS4 Port				
NC	DS4_RXP	I	15	SuperSpeed receive plus
NC	DS4_RXM	I	14	SuperSpeed receive minus
NC	DS4_TXP	O	11	SuperSpeed transmit plus
NC	DS4_TXM	O	12	SuperSpeed transmit minus
NC	DS4_DP	I/O	67	USB 2.0 data plus
NC	DS4_DM	I/O	68	USB 2.0 data minus
OVR curr		I	30	Ganged overcurrent input
PWR_EN		I/O	29	Ganged power enable output
NC		I/O	25	NC

Table 2. 68-Pin QFN Pinout (continued)

Pin Name		Type	Pin#	Description
CYUSB3302	CYUSB3304			
RESERVED1		I/O	21	This pin must be pulled HIGH using a 10 k Ω to VDD_IO.
RESERVED2		I	22	This pin must be pulled HIGH using a 10 k Ω to VDD_IO.
Mode Select, Clock, and Reset				
MODE_SEL[0]		I	23	Device operation mode select bit 0; refer to Table 4
MODE_SEL[1]		I	24	Device operation mode select bit 1; refer to Table 4
XTL_OUT		A	54	Crystal out
XTL_IN		A	55	Crystal in
RESETN		I	31	Active LOW reset input
I2C_CLK		I/O	32	I ² C clock
I2C_DATA		I/O	33	I ² C data
SUSPEND		I/O	20	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
Power and Ground				
VDD_EFUSE		PWR	19	1.2 V normal operation, 2.5 V for programming
AVDD12		PWR	10, 16, 34, 46, 52, 53	1.2 V analog supply
GND		PWR	40	GND pin
DVDD12		PWR	1, 3, 7, 13, 27, 37, 43, 49,	1.2 V core supply
VBUS_US		PWR	17	This pin must be connected to VBUS from US port
VBUS_DS		PWR	18	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33		PWR	4, 56, 61, 66	3.3 V analog supply
VDD_IO		PWR	28	3.3 V I/O supply
USB Precision Resistors				
RREF_USB2		A	2	Connect pin to a precision resistor (6.04 k Ω \pm 1%) to generate a current reference for USB 2.0 PHY.
RREF_SS		A	26	Connect pin to a precision resistor (200 Ω \pm 1%) for SS PHY termination impedance calibration.

Figure 8. HX3 88-Pin QFN 2-Port Pinout

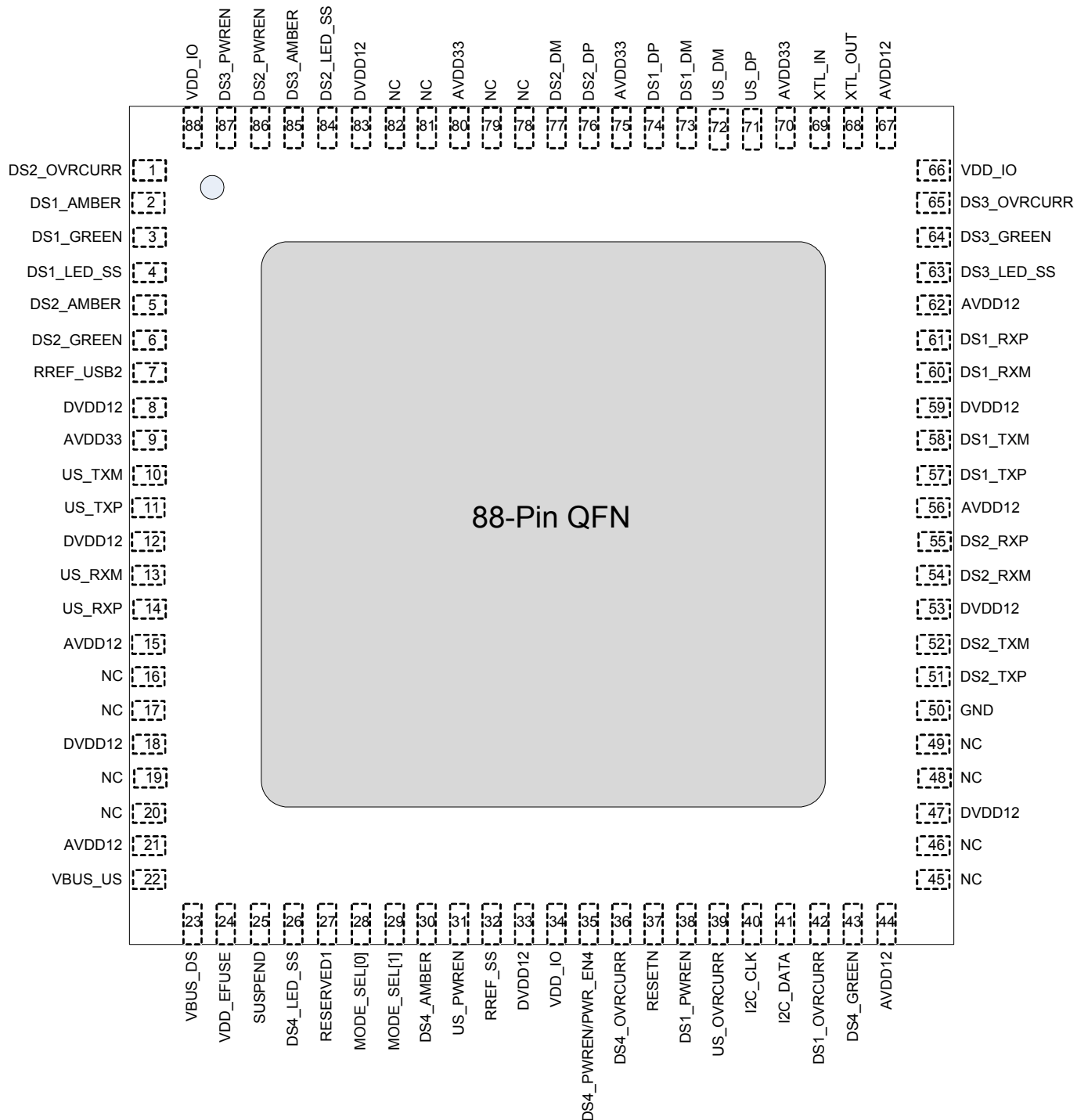


Figure 9. HX3 88-Pin QFN 4-Port Pinout

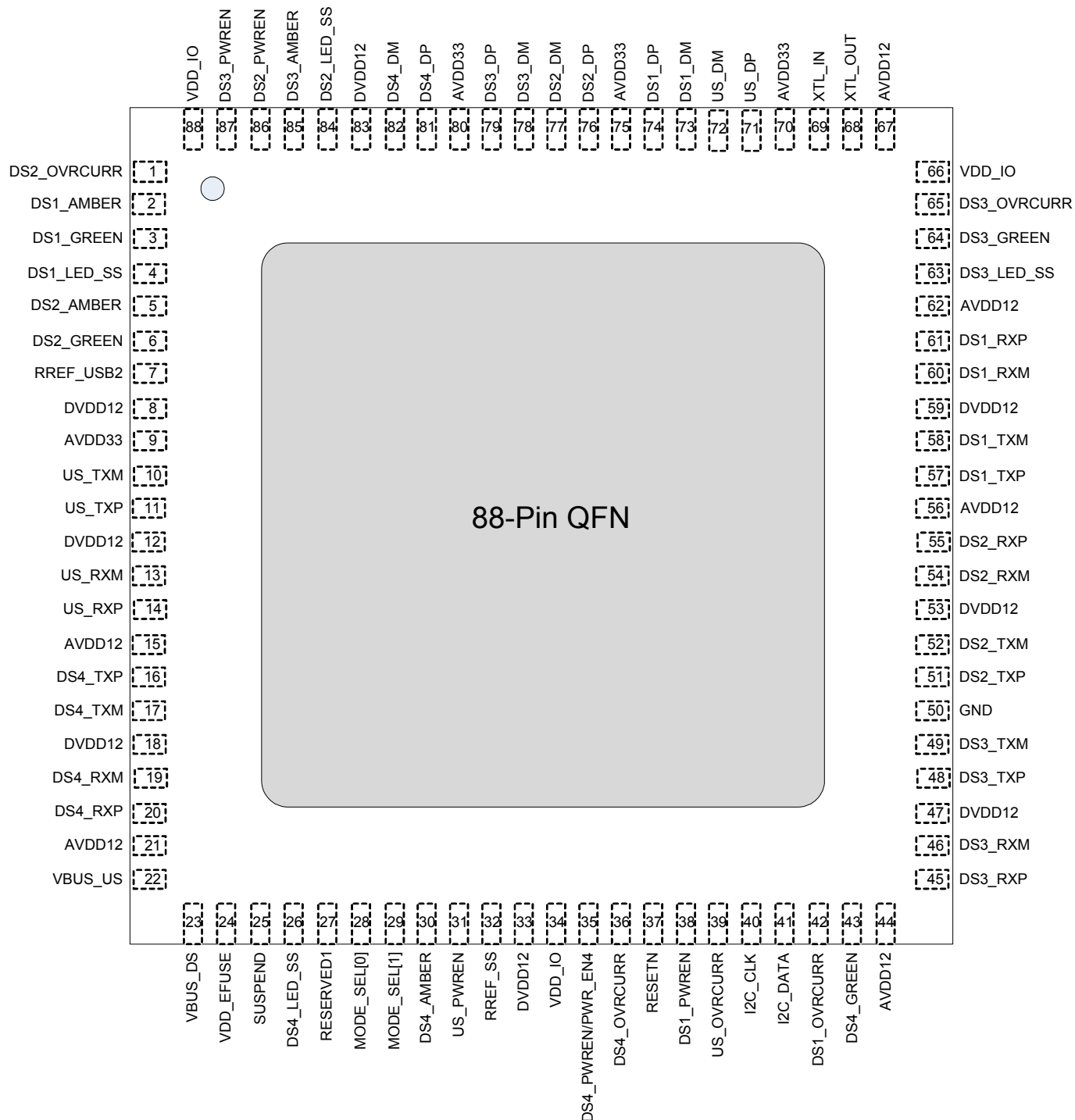


Table 3. 88-Pin QFN Pinout

Pin Name		Type	Pin#	Description
CYUSB3312	CYUSB3314			
	CYUSB3326			
	CYUSB3328			
US Port				
US_RXP	I	14	SuperSpeed receive plus	
US_RXM	I	13	SuperSpeed receive minus	
US_TXP	O	11	SuperSpeed transmit plus	
US_TXM	O	10	SuperSpeed transmit minus	
US_DP	I/O	71	USB 2.0 data plus	
US_DM	I/O	72	USB 2.0 data minus	
US_OVRCURR	I	39	CYUSB3328: Overcurrent detect input for US port in ACA-Dock mode. If ACA-Dock mode is disabled using Configuration Options on page 17 , this pin must be pulled HIGH using a 10 kΩ to VDD_IO. Other part numbers: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.	
US_PWREN ^[1]	I/O	31	CYUSB3328: VBUS power enable output for US port in ACA-Dock mode. If ACA-Dock mode is disabled using Configuration Options on page 17 , this pin can be left floating if Pin-Strap is not enabled. Other part numbers: This pin can be left floating if Pin-Strap (Pin# 63) is not enabled.	
PWR_SW_POL ^[2]			This pin is called PWR_SW_POL in pin-strap configuration mode.	
DS1 Port				
DS1_RXP	I	61	SuperSpeed receive plus	
DS1_RXM	I	60	SuperSpeed receive minus	
DS1_TXP	O	57	SuperSpeed transmit plus	
DS1_TXM	O	58	SuperSpeed transmit minus	
DS1_DP	I/O	74	USB 2.0 data plus	
DS1_DM	I/O	73	USB 2.0 data minus	
DS1_OVRCURR	I	42	Overcurrent detect input for DS1 port	
DS1_PWREN ^[1]	I/O	38	VBUS power enable output for DS1 port. When the port is disabled, this pin is in tristate.	
DS1_CDP_EN ^[2]			This pin is called DS1_CDP_EN in pin-strap configuration mode.	
DS1_AMBER ^[1]	I/O	2	LED_AMBER output for DS1 port	
ACA_DOCK ^[2]			This pin is called ACA-DOCK in pin-strap configuration mode.	
DS1_GREEN ^[1]	I/O	3	CYUSB3312/3314: LED_GREEN output for DS1 port	
DS1_VBUSEN_SL ^[1]			CYUSB3326/3328: VBUS power enable output for SS port 1	
PORT_DISABLE[0] ^[2]			This pin is called PORT_DISABLE[0] in pin-strap configuration mode.	
DS1_LED_SS ^[1]	I/O	4	LED_SS output for DS1 port	
PORT_DISABLE[1] ^[2]			This pin is called PORT_DISABLE[1] in pin-strap configuration mode.	

Notes

1. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
2. For pin-strap configuration details, refer to [Table 5](#).

Table 3. 88-Pin QFN Pinout (continued)

Pin Name		Type	Pin#	Description
CYUSB3312	CYUSB3314			
	CYUSB3326			
	CYUSB3328			
DS2 Port				
DS2_RXP		I	55	SuperSpeed receive plus
DS2_RXM		I	54	SuperSpeed receive minus
DS2_TXP		O	51	SuperSpeed transmit plus
DS2_TXM		O	52	SuperSpeed transmit minus
DS2_DP		I/O	76	USB 2.0 data plus
DS2_DM		I/O	77	USB 2.0 data minus
DS2_OVRCURR		I	1	Overcurrent detect input for DS2 port
DS2_PWREN ^[3]		I/O	86	VBUS power enable output for DS2 port. When the port is disabled, this pin is in tristate.
DS2_CDP_EN ^[4]				This pin is called DS2_CDP_EN in the pin-strap configuration mode.
DS2_AMBER ^[3]		I/O	5	LED_AMBER output for DS2 port
NON_REMOVABLE[0] ^[4]				This pin is called NON_REMOVABLE[0] in the pin-strap configuration mode.
DS2_GREEN ^[3]		I/O	6	CYUSB3312/3314: LED_GREEN output for DS2 port
DS2_VBUSEN_SL ^[3]				CYUSB3326/3328: VBUS power enable output for SS port 2
NON_REMOVABLE[1] ^[4]				This pin is called NON_REMOVABLE[1] in the pin-strap configuration mode.
DS2_LED_SS ^[3]		I/O	84	LED_SS output for DS2 port
PWR_EN_SEL ^[4]				This pin is called PWR_EN_SEL in the pin-strap configuration mode.
DS3 Port				
NC	DS3_RXP	I	45	SuperSpeed receive plus
NC	DS3_RXM	I	46	SuperSpeed receive minus
NC	DS3_TXP	O	48	SuperSpeed transmit plus
NC	DS3_TXM	O	49	SuperSpeed transmit minus
NC	DS3_DP	I/O	79	USB 2.0 data plus
NC	DS3_DM	I/O	78	USB 2.0 data minus
DS3_OVRCURR		I	65	CYUSB3314/3326/3328: Overcurrent detect input for DS3 port CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
DS3_PWREN ^[3]		I/O	87	VBUS power enable output for DS3 port. When the port is disabled, this pin is in tristate.
DS3_CDP_EN ^[4]				This pin is called DS3_CDP_EN in the pin-strap configuration mode.
DS3_AMBER ^[3]		I/O	85	LED_AMBER output for DS3 port
VID_SEL[2] ^[4]				This pin is called VID_SEL[2] in the pin-strap configuration mode.

Notes

 3. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.

 4. For pin-strap configuration details, refer to [Table 5](#).

Table 3. 88-Pin QFN Pinout (continued)

Pin Name		Type	Pin#	Description
CYUSB3312	CYUSB3314			
	CYUSB3326			
	CYUSB3328			
DS3_GREEN ^[5]		I/O	64	CYUSB3312/3314: LED_GREEN output for DS3 port
DS3_VBUSEN_SL ^[5]				CYUSB3326/3328: VBUS power enable output for SS port 3
VID_SEL[1] ^[6]				This pin is called VID_SEL[1] in the pin-strap configuration mode. For pin-strap configuration details, refer to Table 5 .
DS3_LED_SS ^[5]		I/O	63	LED_SS output for DS3 port
PIN_STRAP ^[6]				This pin is called PIN_STRAP in pin-strap configuration mode. When connected to VDD_IO through a 10-kΩ resistor, this pin enables pin-strap configuration mode for HX3.
DS4 Port				
NC	DS4_RXP	I	20	SuperSpeed receive plus
NC	DS4_RXM	I	19	SuperSpeed receive minus
NC	DS4_TXP	O	16	SuperSpeed transmit plus
NC	DS4_TXM	O	17	SuperSpeed transmit minus
NC	DS4_DP	I/O	81	USB 2.0 data plus
NC	DS4_DM	I/O	82	USB 2.0 data minus
DS4_OVRCURR		I	36	CYUSB3314/3326/3328: Overcurrent detect input for DS4 port. CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
DS4_PWREN/PWR_EN4		I/O	35	VBUS power enable output for DS4 port. This pin is also used as power enable output when configured in ganged power mode using the Blaster Plus tool. When the port is disabled, this pin is in tristate.
DS4_CDP_EN ^[6]				This pin is called DS4_CDP_EN in the pin-strap configuration mode.
DS4_AMBER ^[5]		I/O	30	LED_AMBER output for DS4 port
I2C_DEV_ID ^[6]				This pin is called I2C_DEV_ID in the pin-strap configuration mode.
DS4_GREEN ^[5]		I/O	43	CYUSB3312/3314: LED_GREEN output for DS4 port
DS4_VBUSEN_SL				CYUSB3326/3328: VBUS power enable output for SS port 4
VID_SEL[0] ^[6]				This pin is called VID_SEL[0] in the pin-strap configuration mode.
DS4_LED_SS		I/O	26	LED_SS output for DS4 port. The LED must be connected to GND as shown in Figure 12 on page 18 . If LED is not used, this pin must be pulled HIGH using a 10 kΩ to VDD_IO.
RESERVED1		I	27	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
Mode Select, Clock, and Reset				
MODE_SEL[0]		I	28	Device operation mode select bit 0; refer to Table 4
MODE_SEL[1]		I	29	Device operation mode select bit 1; refer to Table 4
XTL_OUT		A	68	Crystal out
XTL_IN		A	69	Crystal in
RESETN		I	37	Active LOW reset input
I2C_CLK		I/O	40	I ² C clock
I2C_DATA		I/O	41	I ² C data

Notes

5. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
 6. For pin-strap configuration details, refer to [Table 5](#).

Table 3. 88-Pin QFN Pinout (continued)

Pin Name		Type	Pin#	Description
CYUSB3312	CYUSB3314			
	CYUSB3326			
	CYUSB3328			
SUSPEND		I/O	25	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
Power and Ground				
VDD_EFUSE		PWR	24	1.2 V normal operation, 2.5 V for programming
AVDD12		PWR	15, 21, 44, 56, 62, 67	1.2 V analog supply
GND		PWR	50	GND pin
DVDD12		PWR	8, 12, 18, 33, 47, 53, 59, 83	1.2 V core supply
VBUS_US		PWR	22	CYUSB3328: Connect the VBUS_US pin to the local 5 V supply. If ACA-Dock mode is disabled using Configuration Options on page 17 , this pin must be connected to VBUS from US port. Other part numbers: This pin must be connected to VBUS from US port.
VBUS_DS		PWR	23	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33		PWR	9, 70, 75, 80	3.3 V analog supply
VDD_IO		PWR	34, 66, 88	3.3 V I/O supply
USB Precision Resistors				
RREF_USB2		A	7	Connect pin to a precision resistor (6.04 k Ω \pm 1%) to generate a current reference for USB 2.0 PHY.
RREF_SS		A	32	Connect pin to a precision resistor (200 Ω \pm 1%) for SS PHY termination impedance calibration.

System Interfaces

Upstream Port (US)

This port is compliant with the USB 3.0 specification and includes an integrated 1.5 k Ω pull-up and termination resistors. It also supports ACA-Dock to enable charging an OTG host connected on the US port.

Downstream Ports (DS1, 2, 3, 4)

DS ports are compliant with the USB 3.0 specification and integrate 15 k Ω pull-down and termination resistors. Ports can be disabled or enabled, and can be set to removable or non-removable options. BC v1.2 charging is enabled by default and can be disabled on each DS port using the configuration options (see [Configuration Options](#)).

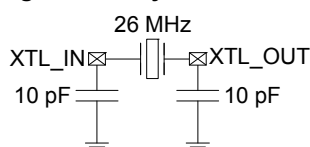
Communication Interfaces (I²C)

The interface follows the Inter-IC Bus specification, version 3.0, with support for the standard mode (100 kHz) and the fast mode (400 kHz) frequencies. HX3 supports I²C in the slave and master modes. The I²C interface supports the multi-master mode of operation. Both the SCL and SDA signals require external pull-up resistors based on the specification. VDD_IO for HX3 is 3.3 V and it is expected that the I²C pull-up resistors will be connected to the same supply.

Oscillator

HX3 requires an external crystal with a frequency of 26 MHz and an accuracy of ± 150 ppm in parallel resonant, fundamental mode. The crystal drive circuit is capable of a low-power drive level (<200 μ W). The crystal connection to the XTL_OUT and XTL_IN pins is shown in [Figure 10](#).

Figure 10. Crystal Connection



GPIOs

HX3 GPIOs are used for overcurrent sensing, controlling external power switches, and driving LEDs. These pins can sink up to 4 mA current each. GPIOs also enable pin-straps for input configuration. Refer to [Table 5](#) for more details.

Power Control

The PWR_EN[1-4] and OV_CURR[1-4] pins interface HX3 to external power switches. These pins are used to control power switches for DS port power and monitor overcurrent conditions. The power switch polarity and the power control mode (individual and ganged) can be changed using the configuration options.

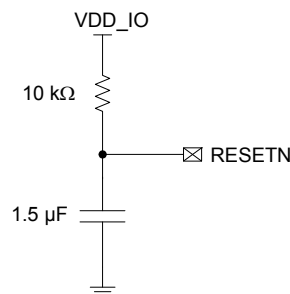
Reset

HX3 operates with two external power supplies, 3.3 V and 1.2 V. There is no power sequencing requirement between these two supplies. However, the RESETN pin should be held LOW until both these supplies become stable.

The RESETN pin can be tied to VDD_IO through an external resistor and to ground (GND) through an external capacitor (minimum 5 ms time constant), as shown in [Figure 11](#). This creates a clean reset signal for power-on reset (POR).

HX3 does not support internal brown-out detection. If the system requires this feature, an external reset should be provided on the RESETN pin when supplies are below their valid operating ranges.

Figure 11. Reset Connection



Configuration Mode Select

Configuration options are selected through the MODE_SEL pins and the pin-strap enable pin (PIN_STRAP). After power-up, these pins are sampled by an on-chip bootloader to determine the configuration options (see [Table 4](#)).

Table 4. HX3 Boot Sequence

MODE SEL[1]	MODE SEL[0]	HX3 Configuration Modes
0	0	Reserved. Do not use this mode.
1	1	Internal ROM configuration (See Errata on page 30)
0	1	I ² C Master, read configuration from I ² C EEPROM ¹
1	0	I ² C Slave, configure from an external I ² C Master

¹ Download Cypress-provided firmware from www.cypress.com/hx3.

Configuration Options

HX3 can be configured by using one of the following:

- eFuse (one-time programmable memory)
- Pin-Strap (read configuration from dedicated pins at power on)
- External I²C slave such as an EEPROM
- External I²C master

The I²C master/slave configuration overrides the pin-strap configuration. Pin-straps override the eFuse configuration, and the eFuse configuration overrides the internal ROM configuration.

eFuse Configuration

HX3 contains eFuses, which are OTP elements on the chip that can be electrically blown. The eFuses are read by the bootloader to determine the customer-specific configurations. eFuse programming is supported only at factory and distributor locations where programming conditions can be controlled.

eFuse programming is supported under the following conditions:
 Temperature range of 25 °C–70 °C and programming voltage of 2.5 V–2.7 V.

Pin-Strap Configuration

Pin-straps are supported for select product options (see [Table 1](#)) to provide reconfigurability without an additional EEPROM. The pin-strap configuration is enabled by pulling the Pin #63 of 88-pin QFN HIGH. [Table 5](#) shows the configuration options supported through pin-straps and the GPIOs used for this purpose. [Figure 12](#) and [Figure 13](#) show how the GPIOs need to be connected if pin-strap and LED connection are required or only pin-strap is required.

HX3 samples pin-strap GPIOs at power-up. Floating straps are considered as invalid and the default configuration is used. If PIN_STRAP (Pin #63 of 88-pin QFN) is floating, all strap inputs are considered invalid. A GPIO is considered strapped “1” or “0” when connected with a weak pull-up (10 kΩ) or pull-down (10 kΩ) respectively. After the initial sampling at power-up and reset, the GPIOs are used in their normal functions.

Figure 12. Pin-Strap With LED or LED-Only Connection

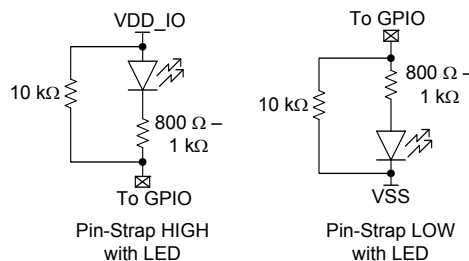


Figure 13. Pin-Strap Connection

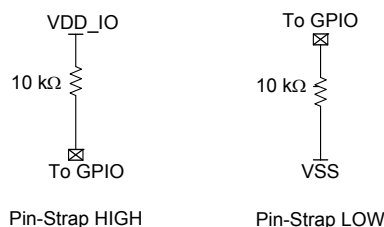


Table 5. Pin-Strap Configuration

88-QFN Pin #	Pin-Strap Name	Strapped '0' ^[7]		Strapped '1' ^[7]	
31	PWR_SW_POL	Power enable and overcurrent will be active LOW		Power enable and overcurrent will be active HIGH	
		strapped '0'	strapped '1'	strapped '0'	strapped '1'
38	DS1_CDP_EN ^[8]	DS1 CDP enabled	DS1 CDP disabled	DS1 CDP disabled	DS1 CDP enabled
86	DS2_CDP_EN ^[8]	DS2 CDP enabled	DS2 CDP disabled	DS2 CDP disabled	DS2 CDP enabled
87	DS3_CDP_EN ^[8]	DS3 CDP enabled	DS3 CDP disabled	DS3 CDP disabled	DS3 CDP enabled
35	DS4_CDP_EN ^[8]	DS4 CDP enabled	DS4 CDP disabled	DS4 CDP disabled	DS4 CDP enabled
2	ACA_DOCK	Disabled		Enabled	
4	PORT_DISABLE[1]	PORT_DISABLE[1:0] = b'00: DS1, DS2, DS3, DS4 active b'01: DS1, DS2, DS3 active b'10: DS1, DS2 active b'11: DS1 active Pin-straps cannot enable ports disabled by factory setting.			
3	PORT_DISABLE[0]				
6	NON_REMOVABLE[1] ^[9]	NON_REMOVABLE[1:0] = b'00: DS1, DS2, DS3, DS4 removable b'01: DS1, DS2, DS3 removable b'10: DS1, DS2 removable b'11: DS1 removable			
5	NON_REMOVABLE[0] ^[9]				
84	PWR_EN_SEL	Individual		Gang	
85	VID[2]	Reserved. If PIN_STRAP is enabled and CY VID is required, strap VID[2:0] to '1'.			
64	VID[1]				
43	VID[0]				
63	PIN_STRAP ^[10]	No pin-strapping		Pin-strapping configuration enabled	
30	I2C_DEV_ID ^[11]	ID 0: HX3 I ² C slave address (7 bits) is 0x60. This is also the default I ² C slave address for the 68-pin QFN package.		ID 1: HX3 I ² C slave address (7 bits) is 0x58	

Notes

- See [Figure 12](#) and [Figure 13](#).
- DS_x_CDP_EN will be active LOW input when PWR_SW_POL is set to active LOW; similarly DS_x_CDP_EN will be active HIGH input when PWR_SW_POL is set to active HIGH.
- These DS ports are exposed ports and the connected devices can be removed.
- VID, PORT_DISABLE, NON_REMOVABLE are group straps. If one of the pins in a group strap is floating (INVALID), that group input will be INVALID and the default will not be overwritten.
- I2C_DEV_ID is valid only when HX3 is in I²C slave mode.

I²C Configuration

When enabled for I²C configuration through the MODE_SEL pins (See Table 4), HX3 can be configured as an I²C master or as an I²C slave. HX3's configuration data is a maximum of 197 bytes and HX3's firmware is 10 KB. Note that HX3's firmware also includes configuration settings.

HX3 as I²C Master

HX3 reads configurations from an external I²C EEPROM with sizes ranging from 16 to 64 KB. An example of a supported EEPROM is 24LC128. Based on the contents of the bSignature and bImageType fields in Table 6, HX3 performs one of the following actions:

- Loads custom configuration settings from the EEPROM when bSignature is "CY" and bImageType is 0xD4.
- Loads the Cypress-provided firmware from the EEPROM when bSignature is "CY" and bImageType is 0xB0. This firmware also includes configuration settings.
- If bSignature ≠ "CY", HX3 enumerates in the vendor-specific mode.

The contents of the EEPROM can be updated with the easy-to-use [Cypress Blaster Plus](#) tool. Blaster Plus is a

GUI-based tool to configure HX3. This tool allows to do the following:

- Download the Cypress-provided firmware from a PC via HX3's US port and store it on an EEPROM connected to HX3's I²C port.
- Read the configuration settings from the EEPROM. These settings are displayed in the Blaster Plus GUI. Modify settings as required.
- Write back the updated settings on to the EEPROM. In addition, an image file can be created for external use.

The Blaster Plus tool, user guide, and the Cypress-provided firmware are available at www.cypress.com/hx3.

HX3 as I²C Slave

An external I²C master can program the configuration settings into HX3 according to the EEPROM map in Table 6. Alternatively, the HX3 firmware (<10 KB), which includes configuration settings, can also be programmed. It is recommended to use the Blaster Plus tool to create the HX3 firmware or configuration image file. HX3's I²C slave address needs to be provided while creating the image file. Refer to Table 5 for HX3's I²C slave address.

Table 6. EEPROM Map

I ² C Offset	Bits	Name	Default	Description
0	7:0	bSignature LSB ("C")	0x43	Two-byte signature initialized with "CY" ASCII text When the signature is not valid, the hub enumerates as a vendor-specific device.
1	7:0	bSignature MSB ("Y")	0x59	Two-byte signature initialized with "CY" ASCII text When the signature is not valid, the hub enumerates as a vendor-specific device.
2	7:6	bImageCTL	b'00	Reserved
	5:4	I ² C Speed	b'11	b'01: 400 kHz b'11: 100 kHz
	3:1	bImageCTL	b'000	Reserved
	0	bImageCTL	0	0: Execution binary file 1: Data file
3	7:0	bImageType	0xD4	0xD4: Load only configuration 0xB0: Load firmware boot image All other bImageType will return an error code.
4	7:0	bD4Length	40	bD4Length is defined in bytes as the length from offset 5. I ² C offset bytes 0–4 are the header bytes. bD4Length = 6: Only update VID, PID, and DID bD4Length = 18: Configuration options (no PHY trim) bD4Length = 40: Configuration options with PHY trim options bD4Length > 40: User must provide valid string descriptors bD4Length > 192: Error
5	7:0	VID [7:0]	0xB4	Custom Vendor ID - LSB
6	7:0	VID [15:8]	0x04	Custom Vendor ID - MSB
7	7:0	PID [7:0]	0x04	Custom Product ID (PID)
8	7:0	PID [15:8]	0x65	Default: 0x6504 If separate PID is used for USB 2.0, the USB 2.0 PID will be read from offset 35 and 36. Else, USB 2.0 PID = 0x6506

Table 6. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
9	7:0	DID [7:0]	0x00 - 88-pin QFN, 0x10 - 68-pin QFN	Custom Device ID - revision
10	7:0	DID [15:8]	0x50	Custom Device ID - revision
11	7:0	Reserved	0	Reserved
12	7:4	SHARED_LINK_EN	b'0000	Enable Shared Link bit[7:4]=DS4, DS3, DS2, DS1 0: Not active 1: Active
	3:0	SHC_ACTIVE_PORTS [3:0]	b'1111	Indicates if a SuperSpeed port is active. bit[3:0] = DS4, DS3, DS2, DS1 0: Not active 1: Active
13	7:0	POWER_ON_TIME	0x32	Time (in 2-ms intervals) from the time the power-on sequence begins on a port until power is good on that port (bPwron2PwrGood)
14	7:4	REMOVABLE_PORTS [3:0]	b'1111	Indicates if the port is removable. bit[7:4]=DS4, DS3, DS2, DS1 0: Non-removable 1: Removable
	3:0	UHC_ACTIVE_PORTS [3:0]	b'1111	Indicates if a USB 2.0 port is active. bit[3:0]=DS4, DS3, DS2, DS1 0: Not active 1: Active
15	7	SS_LED_PIN_CONTROL	0	Port 1–4: SS LED disable 0: DS[1:4]_LED_SS are LEDs. The LED glows when the SS port is active and not in disabled state. 1: DS[1:4]_LED_SS are not LEDs
	6	GREEN_LED_PIN_CONTROL	0	Port 1–4: USB 2.0 Green LED disable 0: DS[1:4]_GREEN are LEDs 1: DS[1:4]_GREEN are not LEDs
	5	AMBER_LED_PIN_CONTROL	0	Port 1–4: USB 2.0 Amber LED disable 0: DS[1:4]_AMBER are LEDs 1: DS[1:4]_AMBER are not LEDs
	4	PORT_INDICATORS	1	Port indicators supported 0: Port indicators are not supported on its DS-facing ports and the USB 2.0 PORT_INDICATOR request has no effect. 1: Port indicators are supported on its DS-facing ports and the USB 2.0 PORT_INDICATOR request controls the indicators.
	3	COMPOUND_HUB	0	Identifies a compound device. 0: Hub is not part of a compound device. 1: Hub is part of a compound device.
	2:1	Reserved	0	Reserved
	0	GANG	0	1: Ganged power switch enable for all DS ports 0: Individual port power switch enable for each DS port

Table 6. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
16	7	SUSPEND_INDICATOR_DISABLE	0	0: Suspend indicator enabled 1: Suspend indicator disabled
	6	SS_US_DISABLE	0	Hub mode of operation (USB 3.0 or USB 2.0) 0: USB 3.0 hub and USB 2.0 hub enabled 1: USB 3.0 hub disabled and USB 2.0 hub enabled
	5	PWR_EN_POLARITY	0	Power control output polarity 0: Active LOW 1: Active HIGH
	4:0	PORT_POLARITY	b'00000	USB 2.0 DP and DM swapped bit[4:0]=DS4, DS3, DS2, DS1, US 1: Port polarity swapped 0: Port polarity not swapped
17	7:5	Reserved	0	Reserved
	4	BC_ENABLE	1	0: BC v1.2 disabled 1: BC v1.2 enabled
	3	ACA_DOCK	0	If this bit is set, enable ACA-Dock on the US port
	2	APPLE_XA	0	0: Max limit for Apple charging 2.1 A 1: Max limit for Apple charging 1 A
	1	Reserved	0	Reserved
	0	GHOST_CHARGE_EN	1	0: Ghost Charging disabled 1: Ghost Charging enabled
18	7:4	CDP_EN[3:0]	b'1111	Per-port charging setting bit[7:4]=DS4, DS3, DS2, DS1 0: CDP disabled 1: CDP enabled
	3:0	DCP_EN[3:0]	b'0000	Per-port charging setting bit[3:0]=DS4, DS3, DS2, DS1 0: DCP disabled 1: DCP enabled
19	7	EMBEDDED_HUB	0	If this bit is set, the US is as an embedded port and VBUS connected to VBUS_US pin is ignored.
	6	ILLEGAL_DESCRIPTOR	1	If this bit is set, the USB 2.0 hub controller will accept both 0x00 and 0x29 as valid descriptor types. If '0', only 0x29 will be accepted as a valid descriptor type.
	5	MODULATE_INDICATOR	1	If this bit is set, the LED outputs will be modulated by a 200 Hz square wave for power saving. If '0', the outputs will be static.
	4	OC_POLARITY	0	Overcurrent input polarity 0: Active LOW 1: Active HIGH
	3:0	OC_TIMER	b'1000	Time in milliseconds for which the overcurrent inputs will be filtered
20	7:0	Reserved	0	Reserved
21	7:4	Reserved	0	Reserved
	3	STRING_DESCRIPTOR_ENABLE	0	0: String descriptor support is disabled 1: String descriptor support is enabled When string descriptors are not supported, the hub controller returns a non-zero index (compile-time programmable) for each string which is supported, and 0x00 for each string not supported, as indicated by this field.
	2:0	Reserved	0	Reserved
22	7:0	Reserved	0	Reserved

Table 6. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
23	7:6	HS_AMPLITUDE_DS4	b'00	HS driver amplitude control; HS driver current: +0% to +7.5% b'00: Default b'01: +2.5% b'10: +5% b'11: +7.5%
	5:4	HS_AMPLITUDE_DS3	b'00	
	3:2	HS_AMPLITUDE_DS2	b'00	
	1:0	HS_AMPLITUDE_DS2	b'00	
24	7:6	HS_AMPLITUDE_US	b'00	HS driver slope control for all ports b'0000: +15% b'0001: +5% b'0100: Default b'0101: -5% b'1111: -7.5%
	5:2	HS_SLOPE	b'0100	
	1:0	HS_TX_VREF	b'10	
25	7:3	HS_PREEMP_EN[4:0]	b'00000	HS driver pre-emphasis enable – for ports DS4, DS3, DS2, DS1, and US 0: pre-emphasis is disabled 1: pre-emphasis is enabled
	2	HS_PREEMP_DEPTH_DS4 ^[12]	0	
	1	HS_PREEMP_DEPTH_DS3 ^[12]	0	
	0	HS_PREEMP_DEPTH_DS2 ^[12]	0	
	7	HS_PREEMP_DEPTH_DS1 ^[12]	0	
	6	HS_PREEMP_DEPTH_US ^[12]	0	
26	5	Reserved	1	Reserved
	4:1	PCS_TX_DEEMPH_DS4	0x6	USB 3.0 Tx driver de-emphasis value 0x3: -2.75 dB 0x6: -3.4 dB (Default) 0x9: -4.0 dB
	0	Reserved	0	
	7:4	PCS_TX_DEEMPH_DS3	0x6	
	3:0	PCS_TX_DEEMPH_DS2	0x6	
27	7:4	PCS_TX_DEEMPH_DS1	0x6	0x3: -2.75 dB 0x6: -3.4 dB (Default) 0x9: -4.0 dB
	3:0	PCS_TX_DEEMPH_US	0x6	
28	7	Reserved	0	Reserved
	6	Reserved	1	
	5:0	PCS_TX_SWING_FULL_DS4	0x29	
29	7:6	Reserved	0	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
	5:0	PCS_TX_SWING_FULL_DS3	0x29	

Note

12. HS_PREEMP_DEPTH is valid only when corresponding HS_PREEMP_EN is set for that port.

Table 6. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
31	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_DS2	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
32	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_DS1	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
33	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_US	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
34	7:0	Reserved	0	Reserved
35	7:0	UHC_PID [7:0]_LSB	0x06	USB 2.0 PID. If bD4Length ≥ 40, USB 2.0 PID will be read from this location.
36	7:0	UHC_PID [15:8]_MSB	0x65	
37–44	7:0	Reserved	0	Eight bytes reserved for future expansion
45	7:0	bLength: LangID	4	Size of LangID (defined by spec as N+2)
46	7:0	DescType	3	String descriptor type (constant value)
47	7:0	LangID - MSB	9	String language ID - MSB of wLangID
48	7:0	LangID - LSB	4	String language ID - MSB of wLangID
49	7:0	bLength: Manufacturer (X)	54	Manufacturer string length ("bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number" should be less than or equal to 152 bytes). X ≤ 66.
50	7:0	DescType	3	String descriptor type (constant value)
51	7:0	bString: Manufacturer	'2', 0, '0', 0, '1', 0, '4', 0, ' ', 0, 'C', 0, 'y', 0, 'p', 0, 'r', 0, 'e', 0, 's', 0, 's', 0, ' ', 0, 'S', 0, 'e', 0, 'm', 0, 'i', 0, 'c', 0, 'o', 0, 'n', 0, 'd', 0, 'u', 0, 'c', 0, 't', 0, 'o', 0, 'r', 0	Manufacturer string: UNICODE UTF-16LE per USB 2.0 specification: "2014 Cypress Semiconductor"
49 + X	7:0	bLength: Product (Y)	22	Product string length ("bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number" should be less than or equal to 152 bytes). Y ≤ 66.
50 + X	7:0	DescType	3	String descriptor type (constant value)

Table 6. EEPROM Map *(continued)*

I ² C Offset	Bits	Name	Default	Description
51 + X	7:0	bString: Product	'C', 0, 'Y', 0, '-', 0, 'H', 0, 'X', 0, '3', 0, ' ', 0, 'H', 0, 'U', 0, 'B', 0	Product string: UNICODE UTF-16LE per USB 2.0 specification: "CY-HX3 HUB"
49 + X + Y	7:0	bLength: Serial Number (Z)	22	Serial number string length ("bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number" should be less than or equal to 152 bytes). Z ≤ 66.
50 + X + Y	7:0	DescType	3	String descriptor type (constant value)
51 + X + Y	7:0	bString: Serial Number	'1', 0, '2', 0, '3', 0, '4', 0, '5', 0, '6', 0, '7', 0, '8', 0, '9', 0, 'A', 0	Serial number string: UNICODE UTF-16LE per USB 2.0 specification: "123456789A"

EMI

HX3 meets the EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. HX3 tolerates EMI conducted by aggressors outlined by the above specifications and continues to function as expected.

ESD

HX3 has a built-in ESD protection on all pins. The ESD protection level provided on these ports is 2.2 kV Human Body Model (HBM) based on the JESD22-A114 specification.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature..... –65 °C to +150 °C

Operating temperature –40 °C to +85 °C

Electrostatic discharge voltage 2200 V

Oscillator or crystal frequency 26 MHz ±150 ppm

I/O voltage supply 3 V to 3.6 V

Maximum input sink current per I/O 4 mA

Electrical Specifications

HX3 meets all USB-IF Electrical Compliance specifications.

DC Electrical Characteristics

Table 7. DC Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
DVDD12	1.2 V core supply		1.14	1.2	1.26	V
VDD_EFUSE	eFuse supply	Normal operation	1.14	1.2	1.26	V
		Programming	2.5	2.6	2.7	
AVDD12	1.2 V analog supply		1.14	1.2	1.26	V
VDD_IO	3.3 V I/O supply		3	3.3	3.6	V
AVDD33	3.3 V analog supply		3	3.3	3.6	V
V _{IH}	Input HIGH voltage		0.7 × VDD_IO	–	VDD_IO	V
V _{IL}	Input LOW voltage		0	–	0.3 × VDD_IO	V
V _{OH}	Output HIGH voltage	Output HIGH voltage at I _{OH} ≤ +4 mA	2.4	–	–	V
V _{OL}	Output LOW voltage	Output LOW voltage at I _{OL} ≥ –4 mA	–	–	0.4	V
I _{OS}	Input sink current	LED GPIO usage	–	–	4	mA
I _{IX}	Input leakage current	All I/O signals held at VDD_IO or GND	–1	–	1	μA
I _{OZ}	Output HI-Z leakage current		–	–	10	μA
I _{CC}	1.2 V supplies combined operating current		–	410	526	mA
I _{CC}	3.3 V supplies combined operating current		–	260	286	mA
I _{SB1}	Total 1.2-V supply current during HX3 suspend	US port is not connected	–	12	20	mA
I _{SB2}	Total 3.3-V supply current during HX3 suspend	US port is not connected	–	4	6	mA
V _{RAMP}	Voltage ramp rate on core and I/O supplies	Voltage ramp must be monotonic	0.2	–	50	V/ms
V _N	Noise level permitted on core and I/O supplies	Max p-p noise level permitted on all supplies except AVDD	–	–	100	mV
V _{N_USB}	Noise level permitted on AVDD12 and AVDD33 supply	Max p-p noise level permitted USB supply	–	–	20	mV

Power Consumption

Table 8 provides the power consumption estimates for HX3 under different conditions. Table 9 summarizes the power consumption for various combinations of devices connected to DS ports.

For example, to calculate the HX3 power consumption for three SS devices connected to DS ports (and no device connected to one DS port), and a US port connected to a USB 3.0 host:

$$\text{Power consumption} = [a] + 2*[g] = 492.5 + 2*76 = 644 \text{ mW}$$

[a] is the active power consumption for the US port connected to a USB 3.0 host and the SS device connected to the DS port.

[g] is the incremental power consumption for an additional SS device connected to the DS port.

Table 8. Power Consumption Estimates for Various Usage Scenarios

Device Condition	Number and Speed of DS Ports Connected	Typical Consumption			Comments
		Supply Current (mA)		Power (mW)	
		1.2 V	3.3 V		
Host not attached	–	18.0	6.0	41.4	–
Suspend with host attached ^[13]	No devices connected	42.0	12.0	90.0	–
Active power with USB 3.0 host ^[14]	1 SS	204.1	75.0	492.5	[a]
	1 HS	51.2	45.2	210.7	[b]
	1 FS	51.2	34.0	173.7	[c]
	1 SS + 1 HS	218.0	103.4	602.9	[d]
Active power with USB 2.0 host ^[14, 15]	1 HS	51.2	45.2	210.7	[e]
	1 FS	51.2	34.0	173.7	[f]
Incremental active power for additional DS port	SS	39.4	8.7	76.0	[g]
	HS	7.0	19.8	73.7	[h]
	FS	7.0	14.2	55.2	[i]
Active power saving per disabled DS port ^[16]	–	10.6	9.6	44.4	[j]

Table 9. Power Consumption Under Various Configurations

Configuration	Number of DS Devices Connected With Data Transfer	Typical Consumption			Comments
		Supply Current (mA)		Power (mW)	
		1.2 V	3.3 V		
USB 3.0 4-Port Hub (USB 3.0 host)	4 SS devices	322	101	720	[a] + 3*[g]
	3 SS + 1 HS devices	297	121	755	[d] + 2*[g]
	3 SS devices	283	92	644	[a] + 2*[g]
USB 3.0 4-Port Hub with one port disabled (USB 3.0 host)	3 SS devices	272	83	600	[a] + 2*[g] - [j]
	2 SS + 1 HS devices	247	103	634	[d] + [g] - [j]
Shared Link with eight DS ports	4 SS + 4 HS devices	357	189	1052	[d] + 3*([g] + [h])
USB 2.0 4-Port Hub (USB 2.0 host)	4 HS devices	72	105	432	[e] + 3*[h]
	3 HS + 1 FS devices	72	99	413	[e] + 2*[h] + [i]

Notes

13. US port in low-power state (SS in U3 and USB 2.0 in L2).

14. All four DS ports are enabled.

15. US SS disabled using configuration options. Refer to Table 6 for I²C configuration options.

16. Power saving applicable only with a USB 3.0 host. DS ports can be disabled through configuration options. Refer to Table 5 for pin-strapping and Table 6 for I²C configuration options.

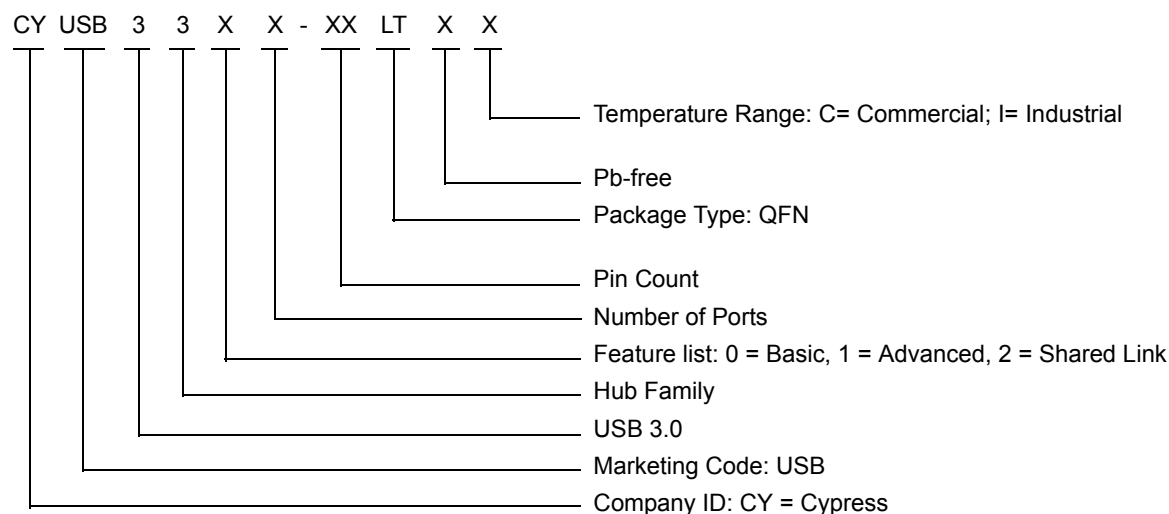
Ordering Information

Table 10 lists HX3's ordering information. The table contains only the part numbers that are currently available for order. Additional part numbers for industrial temperature range can be made available on request. For more information, visit the Cypress [website](#) or contact the local sales representative.

Table 10. Ordering Information

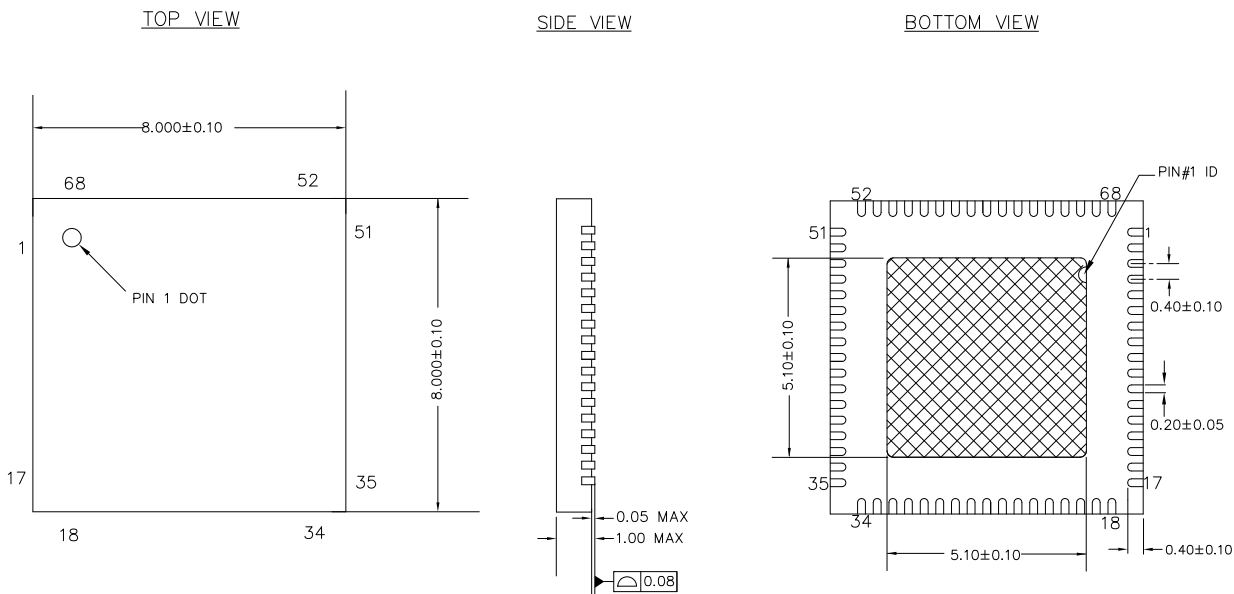
Ordering Part Number	Number of DS Ports	Number of Shared Link Ports	Ghost Charge	ACA- Dock	Temperature	Package
CYUSB3302-68LTXC	2 (USB 3.0)	0	Yes	No	0-70 °C	68-QFN
CYUSB3304-68LTXC	4 (USB 3.0)	0	Yes	No	0-70 °C	68-QFN
CYUSB3304-68LTXI	4 (USB 3.0)	0	Yes	No	-40-85 °C	68-QFN
CYUSB3312-88LTXC	2 (USB 3.0)	0	Yes	No	0-70 °C	88-QFN
CYUSB3314-88LTXC	4 (USB 3.0)	0	Yes	No	0-70 °C	88-QFN
CYUSB3314-88LTXI	4 (USB 3.0)	0	Yes	No	-40-85 °C	88-QFN
CYUSB3326-88LTXC	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2	Yes	No	0-70 °C	88-QFN
CYUSB3326-88LTXI	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2	Yes	No	-40-85 °C	88-QFN
CYUSB3328-88LTXC	8 (4 SS, 4 USB 2.0)	4	Yes	Yes	0-70 °C	88-QFN

Ordering Code Definitions



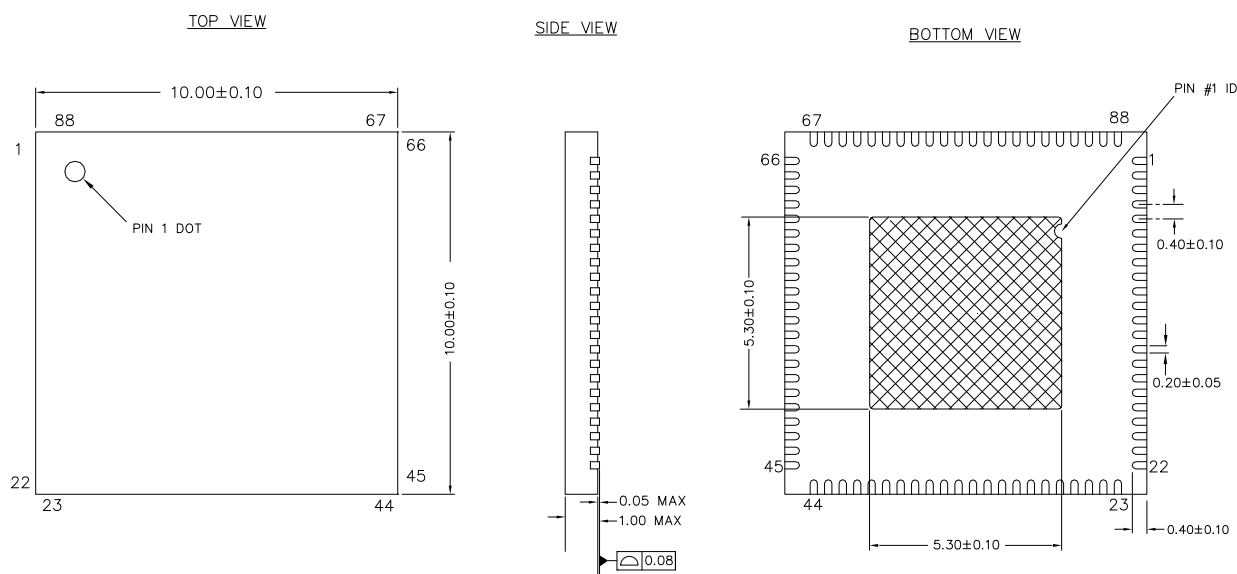
Package Diagrams

Figure 14. 68-pin QFN (8 × 8 × 1.0 mm) LT68B 5.1 × 5.1 mm EPAD (Sawn) Package Outline



001-78925 *B

Figure 15. 88-pin QFN (10 × 10 × 1.0 mm) LT88B 5.3 × 5.3 EPAD (Sawn) Package Outline



001-76569 *A

Acronyms

Table 11. Acronyms Used in this Document

Acronym	Description
ACA	Accessory Charging Adapter
ASSP	Application-Specific Standard Product
BC	Battery Charging
CDP	Charging Downstream Port
DS	DownStream
DCP	Dedicated Charging Port
DWG	Device Working Group
EEPROM	Electrically Erasable Programmable Read-Only Memory
FS	Full-Speed
FW	FirmWare
GND	GrouND
GPIO	General-Purpose Input/Output
HS	Hi-Speed
ISP	In-System Programming
I/O	Input/Output
LS	Low-Speed
NC	No Connect
OTG	On-The-Go
PID	Product ID
POR	Power-On Reset
ROM	Read-Only Memory
SCL	Serial CLock
SDA	Serial DATA
SS	SuperSpeed
TT	Transaction Translator
US	UpStream
VID	Vendor ID

Reference Documents

[USB 2.0 Specification](#)

[USB 3.0 Specification](#)

[Battery Charging Specification](#)

Document Conventions

Units of Measure

Table 12. Units of Measure

Symbol	Unit of Measure
°C	degree celsius
Ω	ohm
Gbps	gigabit per second
KB	kilobyte
kHz	kilohertz
kΩ	kiloohm
Mbps	megabit per second
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
ppm	parts per million
V	volt

Errata

This section describes the errata for the HX3 USB 3.0 Hub. This errata is applicable to all part numbers.

HX3 USB 3.0 Hub Qualification Status

Product Status: Production with Rev. *A silicon

HX3 USB 3.0 Hub Errata Summary

This table defines the errata applicable to the available HX3 USB 3.0 hub devices.

No.	Items	Part Number	Fix Status
1	HX3 with internal ROM firmware does not pass USB-IF compliance certification with Rev. *A silicon.	All	To be fixed in Rev. *B silicon
2	The HX3 US port should not be connected to an FS-only hub or host.	All	To be fixed in Rev. *B silicon

1. HX3 with internal ROM firmware does not pass USB-IF compliance certification with Rev. *A silicon.

■ Problem Definition

HX3 does not pass USB-IF certification with internal ROM firmware.

■ Parameters Affected

N/A

■ Trigger Condition(s)

N/A

■ Scope of Impact

Customer must use Cypress-provided firmware available from www.cypress.com/hx3 to pass USB-IF certification.

■ Workaround

To pass USB-IF certification, it requires Cypress-provided firmware be downloaded to HX3 using (a) I²C EEPROM or (b) external I²C master.

a. When using I²C EEPROM

- Connect EEPROM to HX3 using the I²C interface.
- Connect pins MODE_SEL[0] to HIGH and MODE_SEL[1] to LOW respectively. Refer to [Table 2](#), [Table 3](#), and [Table 4](#) for details on the HX3 pinout and mode selection.
- Use Cypress-provided Blaster Plus software tool to program the firmware into EEPROM. The Blaster Plus tool, user guide, and Cypress-provided firmware are available at www.cypress.com/hx3.
- Reset or power cycle to boot HX3 with the new firmware.

b. When using external I²C master

- Connect I²C master to HX3 using the I²C interface.
- Connect pins MODE_SEL[0] to LOW and MODE_SEL[1] to HIGH respectively. Refer to [Table 2](#), [Table 3](#), and [Table 4](#) for details on the HX3 pinout and mode selection.
- Download firmware for HX3 using the external I²C master.
- Reset or power cycle to boot HX3 with the new firmware.

The Rev. *B silicon will have new internal ROM firmware to pass USB-IF compliance. This silicon will be drop-in compatible for all part numbers. Customers could switch to the Rev. *B silicon and save BOM by eliminating the EEPROM. To move from Rev. *A to Rev. *B silicon, the following changes on the PCB are recommended:

- Connect pins MODE_SEL[0] and MODE_SEL[1] to HIGH.
- EEPROM need not be populated unless required for custom configurations.
- During PCB design, make provision for MODE_SEL[1:0] pins to be configured as HIGH or LOW.

■ Fix Status

To be fixed in the Rev. *B silicon and will be available by July 1, 2014.

2. The HX3 US port should not be connected to an FS-only hub or host.

■ **Problem Definition**

If an HX3 US port is connected to a FS hub or host, FS devices connected to the DS ports may not enumerate. The HX3 US port connected to an HS/SS host or hub will not have this problem.

■ **Parameters Affected**

N/A

■ **Trigger Condition(s)**

N/A

■ **Scope of Impact**

The HX3 US port should not be connected to an FS-only hub or host.

■ **Workaround**

N/A

■ **Fix Status**

To be fixed in the Rev. *B silicon and will be available by July 1, 2014.

Document History Page

Document Title: CYUSB330x, CYUSB331x, CYUSB332x, HX3 USB 3.0 Hub Document Number: 001-73643				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*E	4271496	MURT	02/21/2014	Updated all sections of the datasheet Updated datasheet for new part numbers
*F	4291210	MURT	02/25/2014	Post to web.
*G	4308926	MURT	03/14/2014	Updated Table 6 .

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