NT2L1001_NT2H1001

NTAG 210µ, NFC Forum Type 2 Tag compliant IC with 48 bytes user memory

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Product data sheet
COMPANY PUBLIC

1. Introduction

NXP Semiconductors developed the NTAG 210µ as a standard NFC tag IC to be used in mass market applications such as retail, gaming and publishing. It is used in combination with NFC devices or NFC-compliant Proximity Coupling Devices. NTAG 210µ is designed to comply fully with NFC Forum Type 2 Tag (Ref. 2) and ISO/IEC14443 Type A (Ref. 1) specifications.

Target applications include Out-of-Home and print media smart advertisement, SoLoMo applications, product authentication, NFC shelf labels, mobile companion tags and gaming.

The mechanical and electrical specifications of NTAG 210µ are tailored to meet the requirements of inlay and tag manufacturers.

2. General description

2.1 Contactless energy and data transfer

Communication to NTAG 210µ can be established only when the IC is connected to an antenna. Form and specification of the coil is out of scope of this document.

When NTAG 210µ is positioned in the RF field, the high-speed RF communication interface allows the transmission of the data with a baud rate of 106 kbit/s.

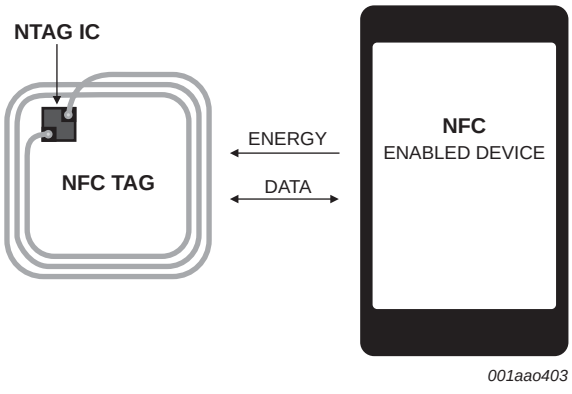


Fig 1. Contactless system

2.2 Simple deployment and user convenience

NTAG 210µ offers specific features designed to improve integration and user convenience:

- NTAG 210µ is available as 17 pF and 50 pF version
- The excellent RF performance allows for more flexibility in the choice of shape, dimension and materials
- The option for 75 µm IC thickness enables the manufacturing of ultrathin tags, for a more convenient integration in e.g. magazines or gaming cards.

2.3 Security

- Manufacturer programmed 7-byte UID for each device
- Pre-programmed Capability container with one time programmable bits
- Field programmable read-only locking function per page
- Pre-programmed ECC-based originality signature, offering the possibility for customizing and permanently locking

2.4 NFC Forum Tag 2 Type compliance

NTAG 210µ IC provides full compliance to the NFC Forum Tag 2 Type technical specification (see Ref. 2) and enables NDEF data structure configurations (see Ref. 3).

2.5 Anticollision

An intelligent anticollision function allows more than one tag to operate in the field simultaneously. The anticollision algorithm selects each tag individually. It ensures that the execution of a transaction with a selected tag is performed correctly without interference from another tag in the field.

3. Features and benefits

- Contactless transmission of data and supply energy
- Operating frequency of 13.56 MHz
- Data transfer of 106 kbit/s
- Data integrity of 16-bit CRC, parity, bit coding, bit counting
- Operating distance up to 100 mm (depending on various parameters as e.g. field strength and antenna geometry)
- 7 bytes serial number (cascade level 2 according to ISO/IEC 14443-3)
- Originality signature
- True anticollision

3.1 EEPROM

- 64 bytes organized in 16 pages with 4 bytes per page
- 48 bytes freely available user Read/Write area (12 pages)
- 4 bytes initialized capability container with one time programmable access bits
- Field programmable read-only locking function per page
- Anti-tearing support for capability container (CC) and lock bits
- Pre-programmed ECC-based originality signature, offering the possibility for customizing and permanently locking
- Data retention time of 10 years
- Write endurance 100,000 cycles

4. Applications

- Smart advertisement
- Goods and device authentication
- Call request
- Gaming
- Call to action
- Voucher and coupons
- Bluetooth simple pairing
- Connection handover

5. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance	NT2L1001	-	17.0	-	pF
		NT2H1001	-	50.0	-	pF
f_i	input frequency		-	13.56	-	MHz
EEPROM characteristics						
t_{ret}	retention time	T_{amb} = 22 °C	10	-	-	years
$N_{endu(W)}$	write endurance	T_{amb} = 22 °C	100000	-	-	cycles

6. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
NT2L1001G0DUF	FFC Bump	8 inch wafer, 75 µm thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 48 bytes user memory, 17 pF input capacitance	-
NT2L1001G0DUD	FFC Bump	8 inch wafer, 120 µm thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 48 bytes user memory, 17 pF input capacitance	-
NT2H1001G0DUF	FFC Bump	8 inch wafer, 75 µm thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 48 bytes user memory, 50 pF input capacitance	-
NT2H1001G0DUD	FFC Bump	8 inch wafer, 120 µm thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 48 bytes user memory, 50 pF input capacitance	-

7. Block diagram

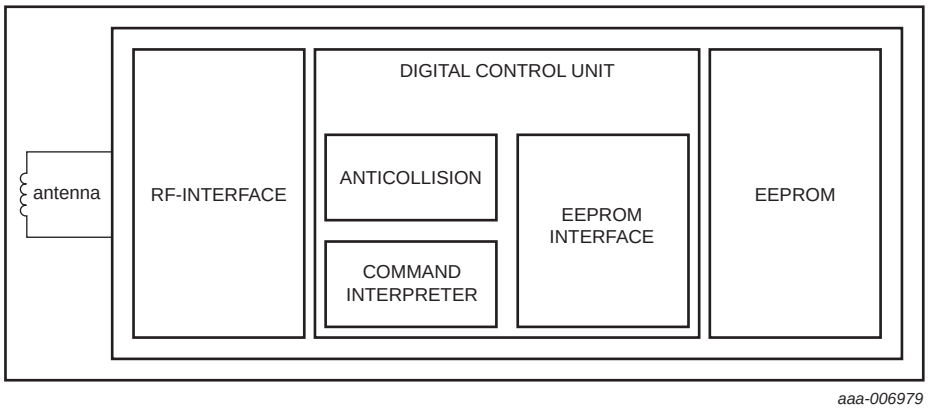


Fig 2. Block diagram of NT2L1001_NT2H1001

8. Pinning information

8.1 Pinning

The pinning of the NT2L1001_NT2H1001 wafer delivery is shown in section “Bare die outline” (see Section 15).

Table 3. Pin allocation table

Pin	Symbol	
LA	LA	Antenna connection LA
LB	LB	Antenna connection LB

9. Functional description

9.1 Block description

NTAG 210µ ICs consist of a 64 bytes of EEPROM, RF interface and Digital Control Unit (DCU). Energy and data are transferred via an antenna consisting of a coil with a few turns which is directly connected to NTAG 210µ. No further external components are necessary. Refer to Ref. 4 for details on antenna design.

- RF interface:
  - modulator/demodulator
  - rectifier
  - clock regenerator
  - Power-On Reset (POR)
  - voltage regulator
- Anticollision: multiple cards may be selected and managed in sequence
- Command interpreter: processes memory access commands supported by the NTAG 210µ
- EEPROM interface
- NTAG 210µ EEPROM: 64 bytes, organized in 16 pages of 4 bytes per page.
  - 10 bytes reserved for manufacturer and configuration data
  - 16 bits used for the read-only locking mechanism
  - 4 bytes available as capability container
  - 48 bytes user programmable read/write memory

9.2 RF interface

The RF-interface is based on the ISO/IEC 14443 Type A standard.

During operation, the NFC device generates an RF field. The RF field must always be present with short pauses for data communication. It is because it is used for both communication and as power supply for the tag.

For both directions of data communication, there is one start bit at the beginning of each frame. Each byte is transmitted with an odd parity bit at the end. The LSB of the byte with the lowest address of the selected block is transmitted first. The maximum length of an NFC device to tag frame is 163 bits. It comprises 16 data bytes + 2 CRC bytes which equal $16 \times 9 + 2 \times 9 + 1$ start bit. The maximum length of a frame from a tag to an NFC device is 307 bits. It comprises 32 data bytes + 2 CRC bytes which equal $32 \times 9 + 2 \times 9 + 1$ start bit.

For a multi-byte response, the least significant byte is always transmitted first. As an example, when reading from the memory using the READ command, byte 0 from the addressed block is transmitted first. It is then followed by byte 1 to byte 3 from this block. The same sequence continues for the next block and all subsequent blocks.

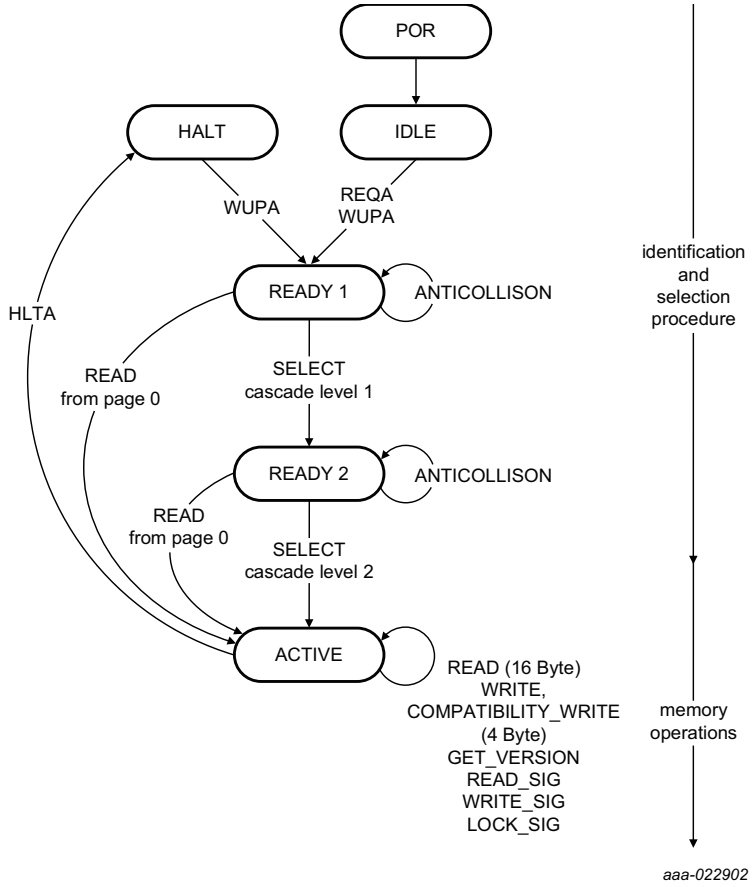
9.3 Data integrity

Following mechanisms are implemented in the contactless communication link between NFC device and NTAG to ensure very reliable data transmission:

- 16 bits CRC per block
- parity bits for each byte
- bit count checking
- bit coding to distinguish between “1”, “0” and “no information”
- channel monitoring (protocol sequence and bit stream analysis)

9.4 Communication principle

The NFC device initiates the commands and the Digital Control Unit of the NTAG 210µ, controls them. The command response is depending on the state of the IC and for memory operations also on the access conditions valid for the corresponding page.



Remark: In all states, the command interpreter returns to the idle state on receipt of an unexpected command. If the IC was previously in the HALT state, it returns to that state.

Fig 3. State diagram

9.4.1 IDLE state

After a power-on reset (POR), NTAG 210µ switches to the IDLE state. It only exits this state when a REQA or a WUPA command is received from the NFC device. Any other data received while in this state is interpreted as an error and NTAG 210µ remains in the IDLE state.

After a correctly executed HLTA command out of the ACTIVE state, the default waiting state changes from the IDLE state to the HALT state. This state can then be exited with a WUPA command or power-on reset only.

9.4.2 READY1 state

In this state, the NFC device resolves the first part of the UID (3 bytes) using the ANTICOLLISION or SELECT commands in cascade level 1. This state is correctly exited after execution of either of the following commands:

- SELECT command from cascade level 1: the NFC device switches NTAG 210µ into READY2 state where the second part of the UID is resolved.
- READ command (from address 0): all anticollision mechanisms are bypassed and the NTAG 210µ switches directly to the ACTIVE state.

Remark: If more than one NTAG 210µ is in the NFC device field, a READ command from address 0 selects all NTAG 210µ devices.
Any other data received in the READY1 state is interpreted as an error and depending on its previous state NTAG 210µ returns to the IDLE or HALT state.

9.4.3 READY2 state

In this state, NTAG 210µ supports the NFC device in resolving the second part of its UID (4 bytes) with the cascade level 2 ANTICOLLISION command. This state is usually exited using the cascade level 2 SELECT command.

Alternatively, READY2 state can be skipped using a READ command (from address 0) as described for the READY1 state.

Remark: The response of NTAG 210µ to the cascade level 2 SELECT command is the select acknowledge (SAK) byte. In accordance with ISO/IEC 14443, this byte indicates if the anticollision cascade procedure has finished. NTAG 210µ is now uniquely selected and only this device communicates with the NFC device even when other contactless devices are present in the NFC device field. If more than one NTAG 210µ is in the NFC device field, a READ command from address 0 selects all NTAG 210µ devices. In this case, a collision occurs.
Any other data received when the device is in this state is interpreted as an error. Depending on its previous state, the NTAG 210µ returns to either the IDLE state or HALT state.

9.4.4 ACTIVE state

All memory operations and other functions like the originality check are operated in the ACTIVE state.

The ACTIVE state is exited with the HLTA command and upon reception NTAG 210µ transits to the HALT state.

Any other data received when the device is in this state is interpreted as an error. Depending on its previous state NTAG 210µ returns to either the IDLE state or HALT state.

9.4.5 HALT state

HALT and IDLE states constitute the two wait states implemented in NTAG 210µ. An already processed NTAG 210µ can be set into the HALT state using the HLTA command. In the anticollision phase, this state helps the NFC device to distinguish between processed tags and tags yet to be selected. NTAG 210µ can only exit this state on execution of the WUPA command. Any other data received when the device is in this state is interpreted as an error and NTAG 210µ state remains unchanged.

9.5 Memory organization

The EEPROM memory is organized in pages with 4 bytes per page. NTAG 210µ has 16 pages in total. The memory organization can be seen in Figure 4, the functionality of the different memory sections is described in the following sections.

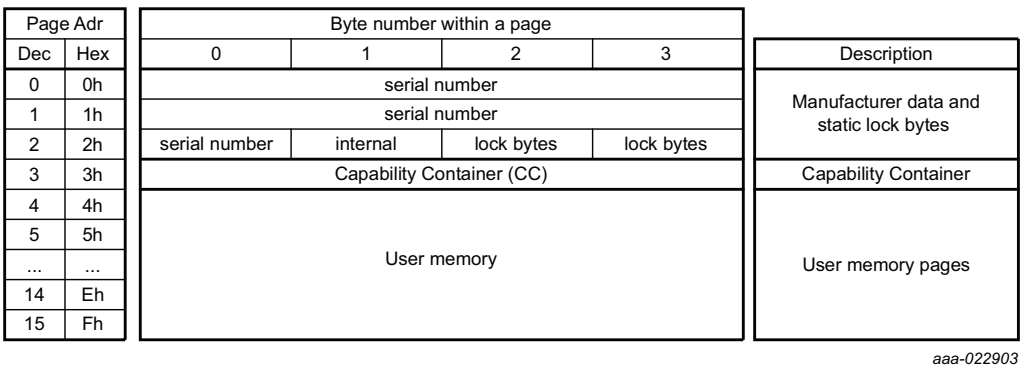


Fig 4. Memory organization NTAG 210µ

The structure of manufacturing data, static lock bytes, capability container and user memory pages are compatible to NTAG 210.

9.5.1 UID/serial number

The unique 7-byte serial number (UID) and its two check bytes are programmed into the first 9 bytes of memory. It covers page addresses 00h, 01h and the first byte of page 02h. The second byte of page address 02h is reserved for internal data. These bytes are programmed and write protected in the production test.

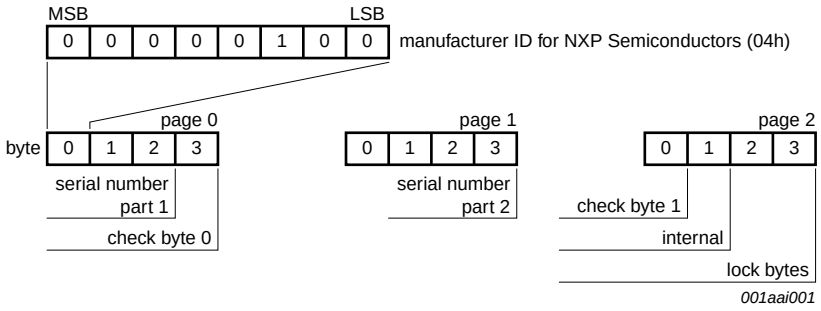


Fig 5. UID/serial number

In accordance with ISO/IEC 14443-3, check byte 0 (BCC0) is defined as CT ⊕ SN0 ⊕ SN1 ⊕ SN2. Check byte 1 (BCC1) is defined as SN3 ⊕ SN4 ⊕ SN5 ⊕ SN6.

SN0 holds the Manufacturer ID for NXP Semiconductors (04h) in accordance with ISO/IEC 14443-3.

9.5.2 Static lock bytes

The bits of byte 2 and byte 3 of page 02h represent the field programmable read-only locking mechanism. Each page from 03h (CC) to 0Fh can be individually locked by setting the corresponding locking bit Lx to logic 1. This locking prevents further write access and the corresponding block becomes read-only memory.

The three least significant bits of lock byte 0 are the block-locking bits. Bit 2 deals with blocks 0Ah to 0Fh, bit 1 deals with blocks 04h to 09h and bit 0 deals with block 03h (CC). Once the block-locking bits are set, the locking configuration for the corresponding memory area is frozen.

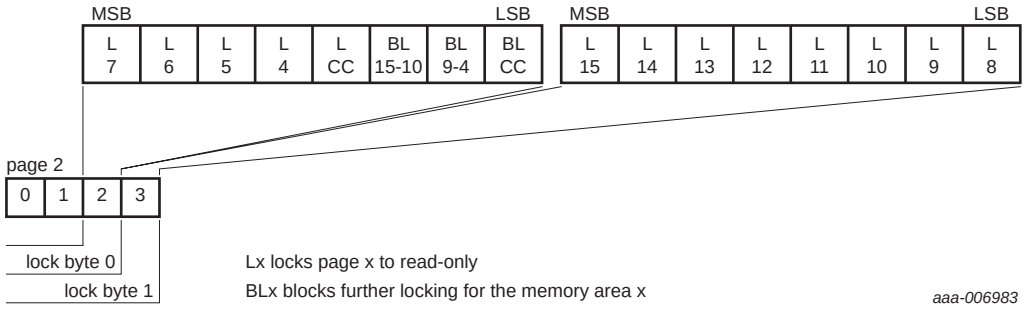


Fig 6. Static lock bytes 0 and 1

For example if BL15-10 is set to logic 1, then bits L15 to L10 (lock byte 1, bit[7:2]) can no longer be changed. A WRITE or COMPATIBILITY_WRITE command to block 02h, sets the static locking and block-locking bits. Data bytes 2 and 3 of the WRITE or COMPATIBILITY_WRITE command, and the contents of the lock bytes, are a bit-wise OR. The result becomes the new content of the lock bytes. This process is irreversible. If a bit is set to logic 1, it cannot be changed back to logic 0.

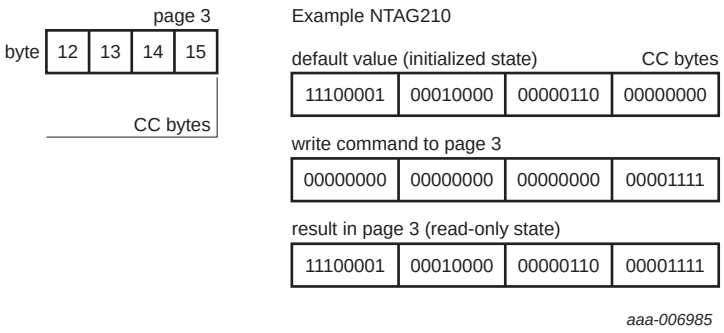
The contents of bytes 0 and 1 of block 02h are unaffected by the corresponding data bytes of the WRITE or COMPATIBILITY_WRITE command.

The default value of the static lock bytes is 00 00h.

Any write operation to the static lock bytes is tearing-proof.

9.5.3 Capability Container (CC bytes)

The Capability Container CC (block 3) is programmed during the IC production according to the NFC Forum Type 2 Tag specification (see Ref. 2). These bytes may be bit-wise modified by a WRITE or COMPATIBILITY_WRITE command.



This memory area can be used as a 32 tick one-time counter.

Fig 7. CC bytes

The parameter bytes of the WRITE command and the current contents of the CC bytes are bit-wise OR'ed. The result is the new CC byte contents. This process is irreversible and once a bit is set to logic 1, it cannot be changed back to logic 0.

Any write operation to the CC bytes is tearing-proof.

The default values of the CC bytes at delivery are defined in Section 9.5.5.

9.5.4 Data blocks

Blocks 04h to 0Fh for NTAG 210µ are the user memory read/write area.

The default values of the data blocks at delivery are defined in Section 9.5.5.

9.5.5 Memory content at delivery

The capability container in block 03h, and the data blocks 04h and 05h of NTAG 210µ, are pre-programmed to the initialized state. It is in accordance with the NFC Forum Type 2 Tag specification (see Ref. 2) as defined in Table 4.

Table 4. Memory content at delivery NTAG 210µ

Block Address	Byte number within block			
	0	1	2	3
03h	E1h	10h	06h	00h
04h	03h	00h	FEh	00h
05h	00h	00h	00h	00h

Remark: The default content of the data blocks from block 05h onwards is not defined at delivery.

9.6 Originality signature

The NTAG 210µ offers a feature to verify the origin of a tag confidently, using the UID toward an originality signature stored in a hidden part of memory. The originality signature can be read with the READ_SIG command.

The NTAG 210µ provides the possibility to customize the originality signature to personalize the IC individually for specific application.

At delivery, the NTAG 210µ is pre-programmed with the NXP originality signature described below. This signature is locked in the dedicated memory. If needed, the signature can be unlocked with the LOCK_SIG command. It is reprogrammed with a custom-specific signature using the WRITE_SIG command during the personalization process by the customer. The signature can be permanently locked afterwards with the LOCK_SIG command to avoid further modifications.

Remark: If no customized originality signature is required, it is recommended to lock the NXP signature permanently during the initialization process with the LOCK_SIG command.

9.6.1 Originality Signature at delivery

At the delivery, the NTAG 210µ is programmed with an NXP digital signature based on standard Elliptic Curve Cryptography (curve name secp128r1), according to the ECDSA algorithm. The use of a standard algorithm and curve ensures easy software integration of the originality check procedure in NFC devices without specific hardware requirements.

Each NTAG 210µ UID is signed with an NXP private key and the resulting 32-byte signature is stored in a hidden part of the NTAG 210µ memory during IC production.

This signature can be retrieved using the READ_SIG command and verified in the NFC device by using the corresponding ECC public key provided by NXP. In case the NXP public key is stored in the NFC device, the complete signature verification procedure can be performed offline.

To verify the signature, for example with the use of the public domain crypto-library OpenSSL, the tool domain parameters are set to secp128r1. It is defined within the standards for elliptic curve cryptography SEC (Ref. 7).

Details on how to check that the NXP signature value is provided in following application note (Ref. 5). It is foreseen to offer an online and offline way to verify originality of NTAG 210µ.

10. Command overview

NTAG 210µ activation follows the ISO/IEC 14443 Type A. After NTAG 210µ has been selected, it can either be deactivated using the ISO/IEC 14443 HLTA command, or the NTAG 210µ commands (e.g. READ or WRITE) can be performed. For more details about the card activation, refer to Ref. 1.

10.1 NTAG 210µ command overview

All available commands for NTAG 210µ are shown in Table 5.

Table 5. Command overview

Command[1]	ISO/IEC 14443	NFC FORUM	Command code (hexadecimal)
Request	REQA	SENS_REQ	26h (7 bit)
Wake-up	WUPA	ALL_REQ	52h (7 bit)
Anticollision CL1	Anticollision CL1	SDD_REQ CL1	93h 20h
Select CL1	Select CL1	SEL_REQ CL1	93h 70h
Anticollision CL2	Anticollision CL2	SDD_REQ CL2	95h 20h
Select CL2	Select CL2	SEL_REQ CL2	95h 70h
Halt	HLTA	SLP_REQ	50h 00h
GET_VERSION	-	-	60h
READ	-	READ	30h
WRITE	-	WRITE	A2h
COMP_WRITE	-	-	A0h
READ_SIG	-	-	3Ch
WRITE_SIG[2]	-	-	A9h
LOCK_SIG[2]			ACh

[1] Unless otherwise specified, all commands use the coding and framing as described in Ref. 1.

[2] This command is new in NTAG 210µ compared to NTAG 210.

10.2 Timings

The command and response timings shown in this document are not to scale and values are rounded to 1 µs.

All given command and response transmission times refer to the data frames including start of communication and end of communication. An NFC device data frame contains the start of communication start-bit and the end of communication logic 0 + 1-bit length of unmodulated carrier. An NFC tag data frame contains the start of communication (1 “start bit”) and the end of communication (1-bit length of no subcarrier).

The minimum command response time is specified according to Ref. 1 as an integer n which specifies the NFC device to NFC tag frame delay time. The frame delay time from NFC tag to NFC device is at least 87 µs. The maximum command response time is specified as a timeout value. Depending on the command, the T_{ACK} value specified for command responses defines the NFC device to NFC tag frame delay time. It does it for either the 4-bit ACK/NAK value specified in Section 10.3 or for a data frame.

All command timings are according to ISO/IEC 14443-3 frame specification as shown for the Frame Delay Time in Figure 8. For more details, refer to Ref. 1.

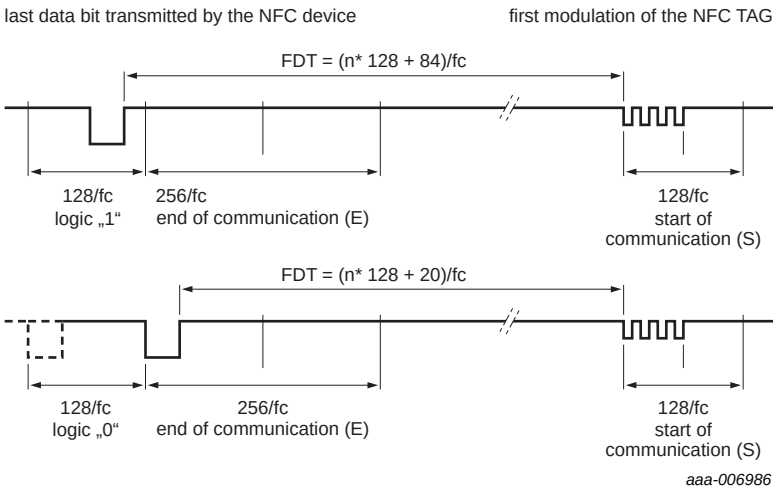


Fig 8. Frame Delay Time (from NFC device to NFC tag)

Remark: Due to the coding of commands, the measured timings usually exclude (a part of) the end of communication. Considered this factor when comparing the specified with the measured times.

10.3 NTAG 210µ ACK and NAK

NTAG 210µ uses a 4-bit ACK / NAK as shown in Table 6.

Table 6. ACK and NAK values

Code (4 bit)	ACK/NAK
Ah	Acknowledge (ACK)
0h	NAK for invalid argument (i.e. invalid block address)
1h	NAK for parity or CRC error
5h or 7h	NAK for EEPROM write error

10.4 ATQA and SAK responses

NTAG 210µ replies to a REQA or WUPA command with the ATQA value shown in Table 7. It replies to a Select CL2 command with the SAK value shown in Table 8. The 2-byte ATQA value is transmitted with the least significant byte first (44h).

Table 7. ATQA response of the NTAG 210µ

		Bit number															
Sales type	Hex value	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
NTAG 210µ	00 44h	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0

Table 8. SAK response of the NTAG 210µ

		Bit number							
Sales type	**Hex value**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
NTAG 210µ	00h	0	0	0	0	0	0	0	0

Remark: The ATQA coding in bits 7 and 8 indicate the UID size according to ISO/IEC 14443.

Remark: The bit numbering in the ISO/IEC 14443 starts with LSB = bit 1 and not with LSB = bit 0. So 1 byte counts bit 1 to bit 8 instead of bit 0 to 7.

11. NTAG 210µ commands

11.1 GET_VERSION

The GET_VERSION command is used to retrieve NTAG21x family information, the product version, storage size and other product data required to identify the specific NTAG21x.

This command is also available on all other NTAG21x products to have a common way of identifying products across platforms and evolution steps.

The GET_VERSION command has no arguments and replies the version information for the specific NTAG21x type. The command structure is shown in Figure 9 and Table 9.

Table 10 shows the required timing.

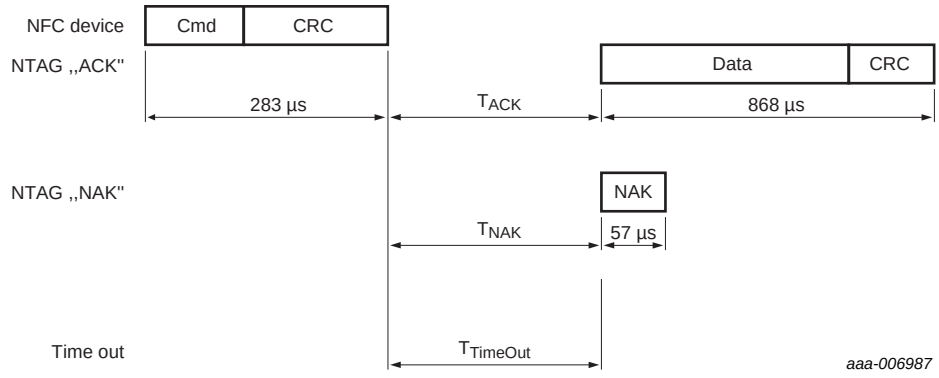


Fig 9. GET_VERSION command

Table 9. GET_VERSION command

Name	Code	Description	Length
Cmd	60h	Get product version	1 byte
CRC	-	CRC according to Ref. 1	2 bytes
Data	-	Product version information	8 bytes
NAK	see Table 6	see Section 10.3	4 bit

Table 10. GET_VERSION timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
GET_VERSION	n = 9[1]	$T_{TimeOut}$	5 ms

[1] Refer to Section 10.2 “Timings”.

Table 11. GET_VERSION response for NTAG 210µ

Byte no.	Description	NT2L1001	NT2H1001	Interpretation
0	fixed Header	00h	00h	
1	vendor ID	04h	04h	NXP Semiconductors
2	product type	04h	04h	NTAG
3	product subtype	01h	02h	17 pF / 50 pF
4	major product version	02h	02h	2
5	minor product version	00h	00h	V0
6	storage size	0Bh	0Bh	see following information
7	protocol type	03h	03h	ISO/IEC 14443-3 compliant

The most significant 7 bits of the storage size byte are interpreted as an unsigned integer value n. As a result, it codes the total available user memory size as 2^n. If the least significant bit is 0b, the user memory size is exactly 2^n. If the least significant bit is 1b, the user memory size is between 2^n and 2^{n+1}.

The user memory for NTAG 210µ is 48 bytes. This memory size is between 32 bytes and 64 bytes. Therefore, the most significant 7 bits of the value 0Bh, are interpreted as 5d and the least significant bit is 1b.

11.2 READ

The READ command requires a start block address, and returns the 16 bytes of four NTAG 210µ blocks. For example, if address (Addr) is 03h then blocks 03h, 04h, 05h, 06h are returned. Special conditions apply if the READ command address is near the end of the accessible memory area. For details on those cases and the command structure, refer to Figure 10 and Table 12.

Table 13 shows the required timing.

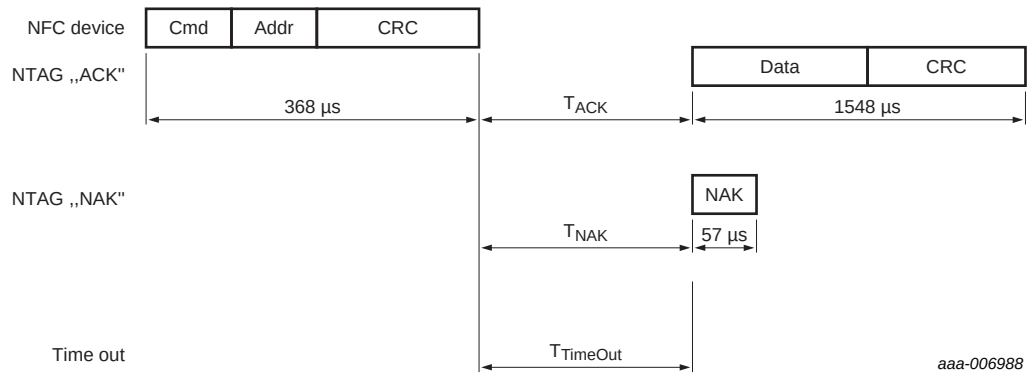


Fig 10. READ command

Table 12. READ command

Name	Code	Description	Length
Cmd	30h	read four blocks	1 byte
Addr	-	start block address	1 byte
CRC	-	CRC according to Ref. 1	2 bytes
Data	-	Data content of the addressed blocks	16 bytes
NAK	see Table 6	see Section 10.3	4 bit

Table 13. READ timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
READ	n = 9[1]	$T_{TimeOut}$	5 ms

[1] Refer to Section 10.2 “Timings”.

Valid memory blocks as Addr parameter to the READ command are

- block address 00h to 0Fh

Addressing a memory block beyond the limits above results in a NAK response from NTAG 210µ.

A roll-over mechanism is implemented to continue reading from block 00h once the end of the accessible memory is reached. Reading from address 0Dh on a NTAG 210µ results in blocks 0Dh, 0Eh, 0Fh and 00h being returned.

11.3 WRITE

The WRITE command requires a block address, and writes 4 bytes of data into the addressed NTAG 210µ block. The WRITE command is shown in Figure 11 and Table 14.

Table 15 shows the required timing.

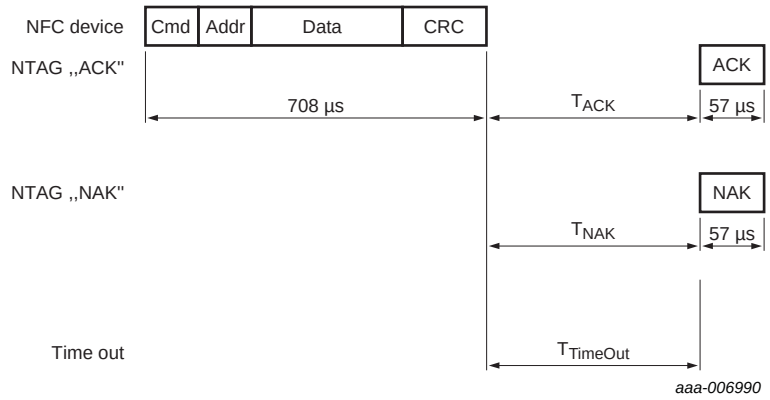


Fig 11. WRITE command

Table 14. WRITE command

Name	Code	Description	Length
Cmd	A2h	write one block	1 byte
Addr	-	block address	1 byte
CRC	-	CRC according to Ref. 1	2 bytes
Data	-	data	4 bytes
NAK	see Table 6	see Section 10.3	4 bit

Table 15. WRITE timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
WRITE	n = 9[1]	$T_{TimeOut}$	10 ms

[1] Refer to Section 10.2 “Timings”.

In the initial state of NTAG 210µ, the following memory blocks are valid Addr parameters to the WRITE command.

- block address 02h to 0Fh for NTAG 210µ

Addressing a memory block beyond the limits above results in a NAK response from NTAG 210µ. Blocks which are locked against writing cannot be reprogrammed using any write command. The locking mechanisms also include the static lock bits.

NTAG 210µ features tearing protected write operations to specific memory content. The following blocks are protected against tearing events during a WRITE operation:

- block 02h containing static lock bits
- block 03h containing CC bits

11.4 COMPATIBILITY_WRITE

The COMPATIBILITY_WRITE command is implemented to guarantee interoperability with the established MIFARE Classic PCD infrastructure, in case of coexistence of ticketing and NFC applications. Even though 16 bytes are transferred to NTAG 210µ, only the least significant 4 bytes (bytes 0 to 3) are written to the specified address. Set all the remaining bytes, 04h to 0Fh, to logic 00h. The COMPATIBILITY_WRITE command is shown in Figure 12, Figure 13 and Table 14.

Table 17 shows the required timing.

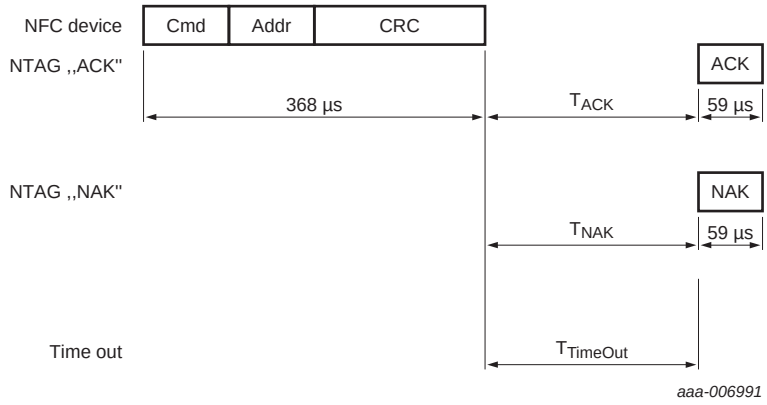


Fig 12. COMPATIBILITY_WRITE command part 1

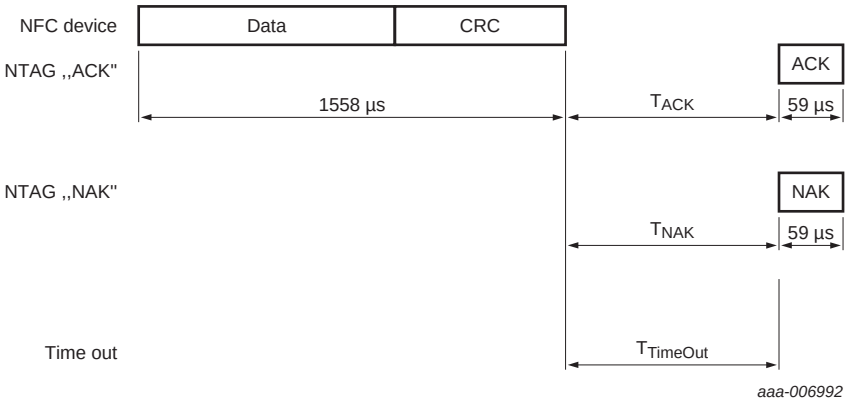


Fig 13. COMPATIBILITY_WRITE command part 2

Table 16. COMPATIBILITY_WRITE command

Name	Code	Description	Length
Cmd	A0h	compatibility write	1 byte
Addr	-	block address	1 byte
CRC	-	CRC according to Ref. 1	2 bytes
Data	-	16-byte Data, only least significant 4 bytes are written	16 bytes
NAK	see Table 6	see Section 10.3	4 bit

Table 17. COMPATIBILITY_WRITE timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
COMPATIBILITY_WRITE part 1	n = 9[1]	$T_{TimeOut}$	5 ms
COMPATIBILITY_WRITE part 2	n = 9[1]	$T_{TimeOut}$	10 ms

[1] Refer to Section 10.2 “Timings”.

In the initial state of NTAG 210µ, the following memory blocks are valid Addr parameters to the COMPATIBILITY_WRITE command.

- block address 02h to 0Fh for NTAG 210µ

Addressing a memory block beyond the limits above results in a NAK response from NTAG 210µ.

Blocks which are locked against writing cannot be reprogrammed using any write command. The locking mechanisms include the static bits as well.

NTAG 210µ features tearing protected write operations to specific memory content. The following blocks are protected against tearing events during a COMPATIBILITY_WRITE operation:

- block 02h containing static lock bits
- block 03h containing CC bits

11.5 READ_SIG

The READ_SIG command returns an IC specific, 32-byte ECC signature. The command structure is shown in Figure 14 and Table 18.

Table 19 shows the required timing.

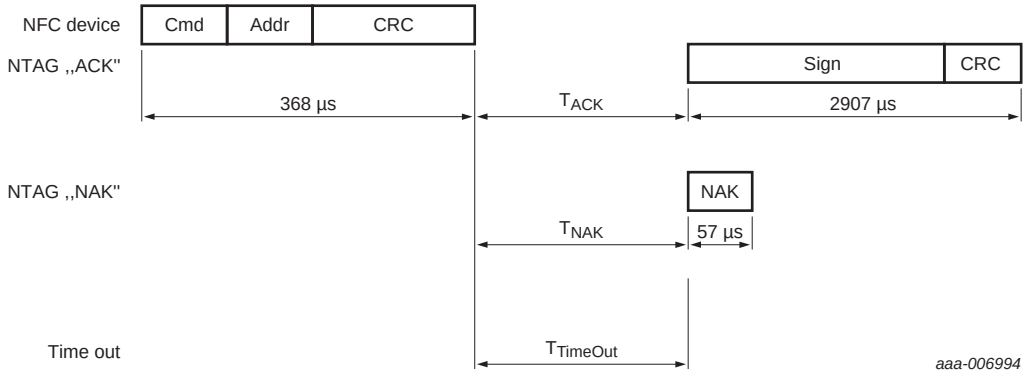


Fig 14. READ_SIG command

Table 18. READ_SIG command

Name	Code	Description	Length
Cmd	3Ch	read ECC signature	1 byte
Addr	00h	RFU, is set to 00h	1 byte
CRC	-	CRC according to Ref. 1	2 bytes
Signature	-	ECC signature	32 bytes
NAK	see Table 6	see Section 10.3	4 bit

Table 19. READ_SIG timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
READ_SIG	n = 9[1]	$T_{TimeOut}$	5 ms

[1] Refer to Section 10.2 “Timings”.

Details on how to check that the signature value is provided in the application note (Ref. 5). It is foreseen to offer an online and offline way to verify originality of NTAG 210µ.

11.6 WRITE_SIG

The WRITE_SIG command allows the writing of a customized originality signature into the dedicated originality signature memory.

The WRITE_SIG command requires an originality signature block address, and writes 4 bytes of data into the addressed originality signature block. The WRITE_SIG command is shown in Figure 15 and Table 20.

Table 21 shows the required timing.

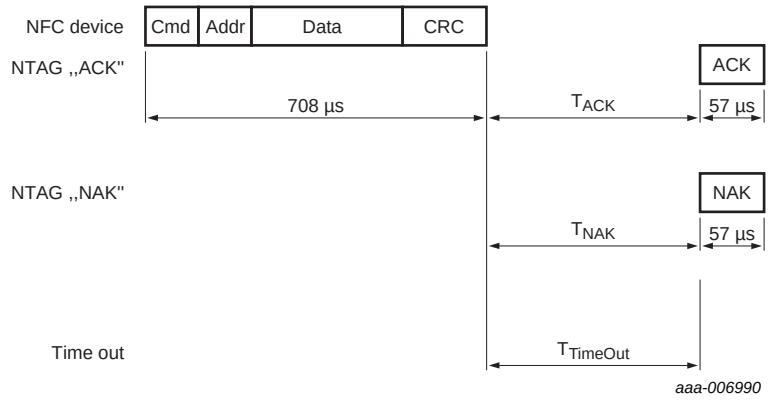


Fig 15. WRITE_SIG command

Table 20. WRITE_SIG command

Name	Code	Description	Length
Cmd	A9h	write one originality signature block	1 byte
Addr	-	block address	1 byte

Table 20. WRITE_SIG command

Name	Code	Description	Length
CRC	-	CRC according to Ref. 1	2 bytes
Data	-	signature bytes to be written	4 bytes
NAK	see Table 6	see Section 10.3	4 bit

Table 21. WRITE_SIG timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
WRITE_SIG	n = 9[1]	$T_{TimeOut}$	10 ms

[1] Refer to Section 10.2 “Timings”.

In the initial state of NTAG 210µ, the following originality signature blocks are valid Addr parameters to the WRITE_SIG command.

- originality signature block address 00h to 07h for NTAG 210µ

Addressing a memory block beyond the limits above results in a NAK response from NTAG 210µ.

Table 22. Blocks for the WRITE_SIG command

Originality signature block	byte 0	byte 1	byte 2	byte 3
00h				MSByte
01h				
...				
06h				
07h	LSByte			

11.7 LOCK_SIG

The LOCK_SIG command allows the user to unlock, lock or permanently lock the dedicated originality signature memory.

The originality signature memory can only be unlocked if the originality signature memory is not permanently locked.

Permanently locking of the originality signature with the LOCK-SIG command is irreversible and the originality signature memory can never be unlocked and reprogrammed again.

The LOCK_SIG command is shown in Figure 16 and Table 23.

Table 24 shows the required timing.

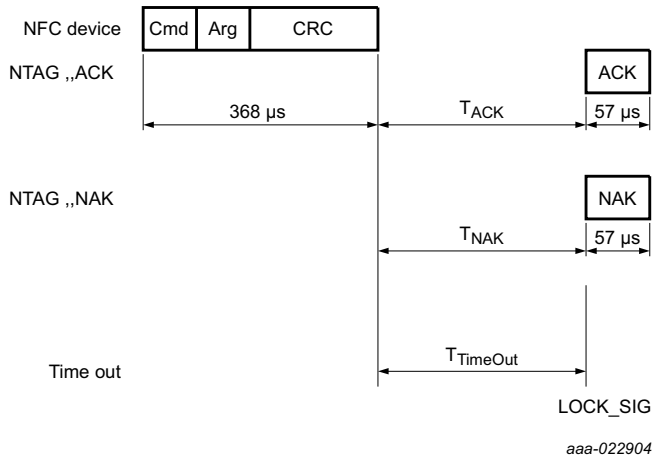


Fig 16. LOCK_SIG command

Table 23. LOCK_SIG command

Name	Code	Description	Length
Cmd	A9h	lock signature	1 byte
Arg	-	locking action	1 byte
		00h - unlock	1 byte
		01h - lock	1 byte
		02h - permanently lock	1 byte
CRC	-	CRC according to Ref. 1	2 bytes
NAK	see Table 6	see Section 10.3	4 bit

Table 24. LOCK_SIG timing

These times exclude the end of communication of the NFC device.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
LOCK_SIG	n = 9[1]	$T_{TimeOut}$	10 ms

[1] Refer to Section 10.2 “Timings”.

12. Limiting values

Stresses exceeding one or more of the limiting values can permanently damage the device. Exposure to limiting values for extended periods can affect device reliability.

Table 25. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
I_I	input current		-	40	mA
P_{tot}	total power dissipation		-	120	mW
T_{stg}	storage temperature		–55	125	°C
T_{amb}	ambient temperature		–25	70	°C
V_{ESD}	electrostatic discharge voltage	on pin LA/LB [1]	2	-	kV

[1] ANSI/ESDA/JEDEC JS-001; Human body model: C = 100 pF, R = 1.5 kΩ

13. Characteristics

Table 26. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance	NT2L1001	-	17.0	-	pF
		NT2H1001	-	50.0	-	pF
f_i	input frequency		-	13.56	-	MHz
EEPROM characteristics						
t_{ret}	retention time	T_{amb} = 22 °C	10	-	-	year
$N_{endu(W)}$	write endurance	T_{amb} = 22 °C	100,000	-	-	cycle

14. Wafer specification

For more details on the wafer delivery forms, see Ref. 5.

Table 27. Wafer specifications NTAG 210

Wafer	
diameter	200 mm typical (8 inches)
maximum diameter after foil expansion	210 mm
thickness	
NT2L1001G0DUD	120 µm ± 15 µm
NT2L1001G0DUF	75 µm ± 10 µm
flatness	not applicable
Potential Good Dies per Wafer (PGDW)	112373
Wafer backside	
material	Si
treatment	ground and stress relieve
roughness	R_a max = 0.5 µm
	R_t max = 5 µm
Chip dimensions	
step size[1]	x = 528 µm
	y = 524 µm
gap between chips[1]	typical = 20 µm
	minimum = 5 µm
Passivation	
type	sandwich structure
material	PSG / nitride
thickness	500 nm / 600 nm
Gold bump (substrate connected to VSS)	
material	> 99.9 % pure gold
hardness	35 to 80 HV 0.005
shear strength	> 70 MPa
height	18 µm
height uniformity	within a die = ±2 µm
	within a wafer = ±3 µm
	wafer to wafer = ±4 µm
flatness	minimum = ±1.5 µm
size	LA, LB, GND, TP[2] = 60 µm × 60 µm
size variation	±5 µm
under bump metallization	sputtered TiW

[1] The step size and the gap between chips may vary due to changing foil expansion

[2] Pads GND and TP are disconnected when wafer is sawn

14.1 Failed die identification

Electronic wafer mapping covers the electrical test results and additionally the results of mechanical/visual inspection. No ink dots are applied.

15. Bare die outline

For more details on the wafer delivery forms, see Ref. 6.

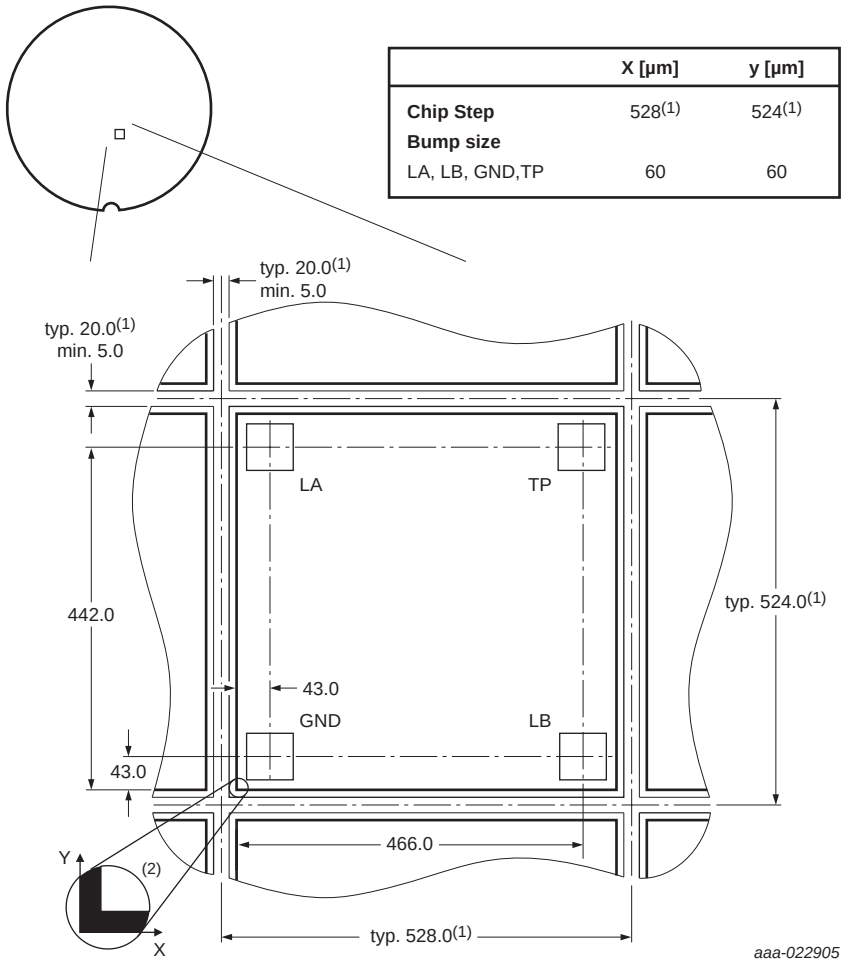


Fig 17. Bare die outline NT2L1001_NT2H1001

16. Abbreviations

Table 28. Abbreviations and symbols

Acronym	Description
ACK	Acknowledge
ATQA	Answer to request, type A
CRC	Cyclic Redundancy Check
CC	Capability Container
CT	Cascade Tag (value 88h) as defined in ISO/IEC 14443-3 type A
ECC	Elliptic Curve Cryptography
EEPROM	Electrically Erasable Programmable Read-Only Memory
FDT	Frame Delay Time
FFC	Film Frame Carrier
IC	Integrated Circuit
LSB	Least Significant Bit
NAK	Not acknowledge
NFC device	NFC Forum device
NFC tag	NFC Forum tag
NV	Non-Volatile memory
REQA	Request command, type A
RF	Radio Frequency
RFUI	Reserved for Future Use - Implemented
RMS	Root Mean Square
SAK	Select acknowledge, type A
SECS-II	SEMI Equipment Communications Standard part 2
TiW	Titanium Tungsten
UID	Unique IDentifier
WUPA	Wake-up Protocol type A

17. References

[1] **ISO/IEC 14443 —** International Organization for Standardization

[2] **NFC Forum Tag 2 Type Operation, Technical Specification —** NFC Forum, 31.05.2011, Version 1.1

[3] **NFC Data Exchange Format (NDEF), Technical Specification —** NFC Forum, 24.07.2006, Version 1.0

[4] **AN11276 NTAG Antenna Design Guide —** Application note, BU-ID Document number 2421**[1]

[5] **AN11350 NTAG21x Originality Signature Validation —** Application note, BU-ID Document number 2604**

[6] **General specification for 8" wafer on UV-tape; delivery types —** Delivery Type Description, BU-ID Document number 1005**

[7] **Certicom Research. SEC 2 —** Recommended Elliptic Curve Domain Parameters, version 2.0, January 2010

1. ** ... BU ID document version number

18. Revision history

Table 29. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NT2L1001_NT2H1001 v.3.0	20160907	Product data sheet	-	NT2L1001_NT2H1001 v.2.0
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Corrections and editorial changes made.			
NT2L1001_NT2H1001 v.2.0	20160414	Preliminary data sheet	-	NT2L1001_NT2H1001 v.1.0
NT2L1001_NT2H1001 v.1.0	20150903	Objective data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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21. Contents

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