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FAIRCHILD SEMICONDUCTOR®

April 2010

FAN6206
Highly Integrated Dual-Channel Synchronous Rectification Controller for Dual-Forward Converter

Features

- Highly Integrated Dual-Channel SR Controller
- Receives Synchronized Driving Signal from the Primary Side
- Internal Linear-Predict Timing Control for DCM Operation
- Ultra-Low V_{DD} Operating Voltage for Different Output Voltage of PC Power
- V_{DD} Over-Voltage Protection
- 14V Gate Driver Clamp

Applications

- PC Power
- Server Power
- Open-Frame SMPS

Description

The highly integrated FAN6206 is a dual-channel synchronous rectification (SR) controller. FAN6206 allows design of a cost-effective power supply with fewer external components, especially suited for dual-forward topology used to obtain higher efficiency for ATX power supplies.

The primary-side control method provides synchronous rectification control for dual-forward converters that operate in continuous conduction mode (CCM). FAN6206 includes a proprietary linear-predict timing control mechanism for dual-forward converters that operate in discontinuous conduction mode (DCM) at fixed or variable frequency. PWM frequency tracking with secondary-side winding detection is provided by adding dividing resistors. The primary-side signals are generated from Fairchild's FAN6210 (Primary-Side Synchronous Rectifier Signal Trigger for Dual-Forward Converter). The primary-side signals are transferred through a pulse transformer to the secondary-side. The benefits of this technique include simple control method and improved power system reliability.

FAN6206 is available in 8-pin SOP package.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6206MY	-40°C to +105°C	8-Pin Small Outline Package (SOP)	Tape & Reel

Application Diagram

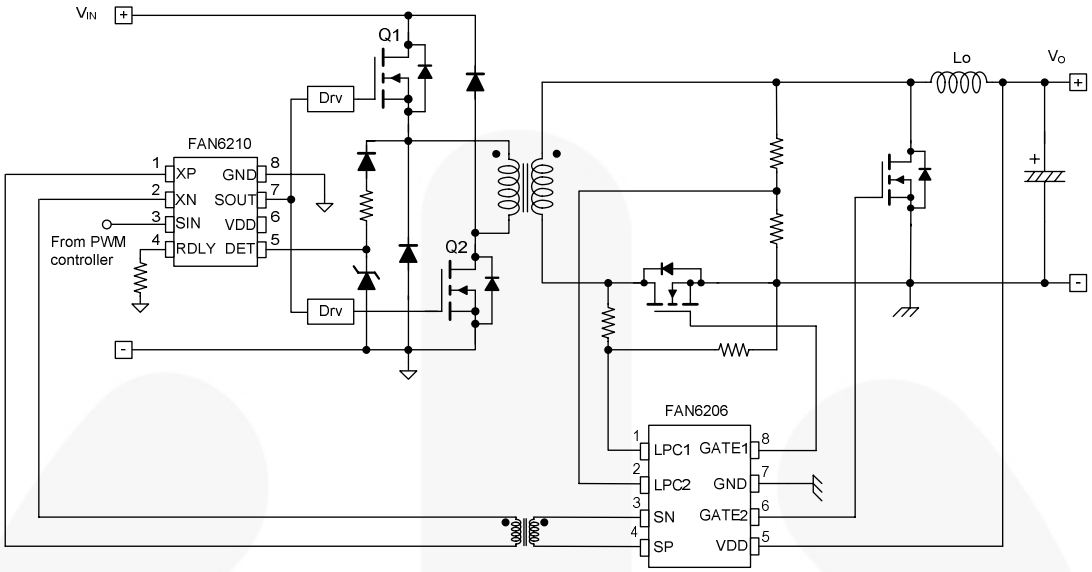


Figure 1. Typical Application

Internal Block Diagram

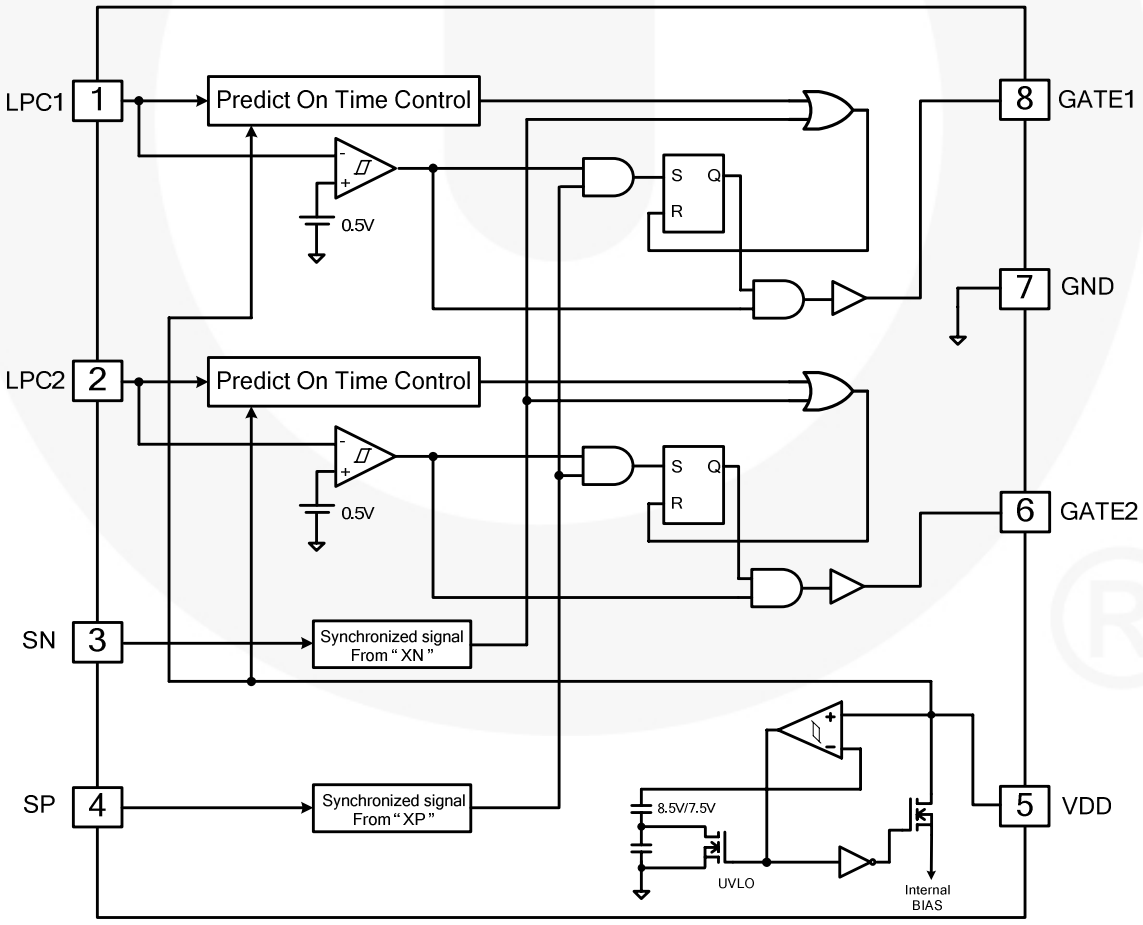
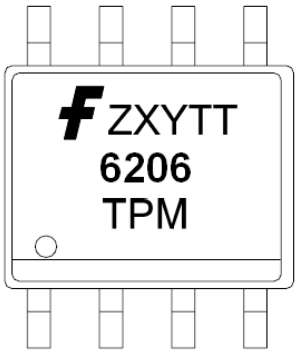


Figure 2. Functional Block Diagram

Marking Information



F: Fairchild Logo
Z: Plant Code
X: Year Code
Y: Week Code
TT: Package Type
T: M=SOP
P: Y: Green Package
M: Manufacture Flow Code

Figure 3. Top Mark

Pin Configuration

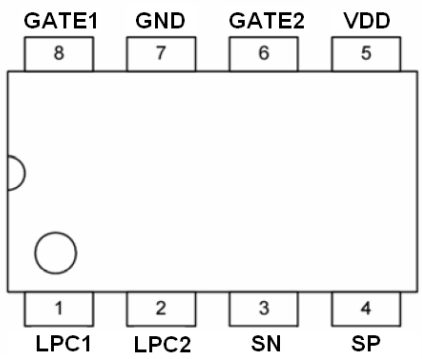


Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1,2	LPC1, LPC2	Winding detection. This pin is used to detect the voltage on the winding during the on-time period of the primary GATE. An internal current source, I_{CHG}, is determined according to the voltage on the DET pin.
3	SN	Synchronized signal to turn on SR. This pin is used to receive the “XN” signal from the primary side to turn off the SR gate.
4	SP	Synchronized signal to turn on SR. This pin is used to receive the “XP” signal from the primary-side to turn-on the SR gate.
5	VDD	Power supply pin. The threshold voltages for startup and turn-off are 8.5V and 7.5V, respectively.
6	GATE2	Driver output for freewheeling synchronous rectifier MOSFET.
7	GND	Ground
8	GATE1	Driver output for rectifying synchronous rectifier MOSFET.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage		30	V
V_{HV}	SP, SN		30	V
V_L	LPC	-0.3	7.0	V
P_D	Power Dissipation at T_A < 50°C		400	mW
Θ_{JA}	Junction to Ambient Thermal Resistance		130	°C/W
Ψ_{jt}	Junction to Top Thermal Characteristics		46	°C/W
T_J	Operating Junction Temperature	-40	+125	°C
T_{STG}	Storage Temperature Range	-55	+150	°C
T_L	Lead Temperature, (Soldering 10 Seconds)		+260	°C
ESD	Human Body Model, JESD22-A114		4.00	kV
	Charged Device Model, JESD22-C101		1.25	

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to GND pin.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

V_{DD}=20V, T_A=25℃, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} Section						
V_{OP}	Continuously Operating Voltage				25	V
V_{TH-ON1}	Turn-On Threshold Voltage		8.0	8.5	9.0	V
V_{TH-ON2}	Turn-On Threshold Voltage		8.0	8.5	9.0	V
$V_{TH-OFF1}$	Turn-Off Threshold Voltage		7.0	7.5	8.0	V
$V_{TH-OFF2}$	Turn-Off Threshold Voltage		7.0	7.5	8.0	V
I_{DD-OP}	Operating Current	V_{DD}=15V, DET=50KHz		3	5	mA
I_{DD-ST}	Startup Current	V_{DD} = 7.5V		340	500	μA
$V_{DD-OVP1}$	V_{DD} Over-Voltage Protection 1		20	21	22	V
$V_{DD-OVP2}$	V_{DD} Over-Voltage Protection 2		20	21	22	V
$V_{DD-OVP-HYS1}$	Hysteresis Voltage for V_{DD} OVP 1		1.2	1.7	2.2	V
$V_{DD-OVP-HYS2}$	Hysteresis Voltage for V_{DD} OVP 2		1.2	1.7	2.2	V
t_{OVP1}	V_{DD} OVP Debounce Time 1		40	60	100	μs
t_{OVP2}	V_{DD} OVP Debounce Time 2		40	60	100	μs
Output Drive for SR MOSFET Section						
V_{Z1}	Output Voltage Maximum (Clamp) 1	V_{DD} = 20V		12	14	V
V_{Z2}	Output Voltage Maximum (Clamp) 2	V_{DD} = 20V		12	14	V
V_{OL1}	Output Voltage LOW 1	V_{DD}=12V, I_O=50mA			0.5	V
V_{OL2}	Output Voltage LOW 2	V_{DD}=12V, I_O=50mA			0.5	V
V_{OH1}	Output Voltage HIGH 1	V_{DD}=12V, I_O=50mA	9			V
V_{OH2}	Output Voltage HIGH 2	V_{DD}=12V, I_O=50mA	9			V
t_{R1}	Rising Time 1	V_{DD}=12V, C_L=7nF, OUT=2V~9V	30	70	120	ns
t_{R2}	Rising Time 2	V_{DD}=12V, C_L=7nF, OUT=2V~9V	30	70	120	ns
t_{F1}	Falling Time1	V_{DD}=12V, C_L=7nF, OUT=9V~2V	20	50	100	ns
t_{F2}	Falling Time 2	V_{DD}=12V, C_L=7nF, OUT=9V~2V	20	50	100	ns
V_{Z1}	Output Voltage Maximum (Clamp)	V_{DD} = 20V		12	14	V
$t_{PD-HIGH-SP1}$	Propagation Delay to OUT HIGH	t_R+t_{PD}, (Trigger by SP), |SP-SN|=5V	280	350	450	ns
$t_{PD-HIGH-SP2}$			280	350	450	
$t_{PD-LOW-SN1}$	Propagation Delay to OUT LOW	t_R+t_{PD}, (Trigger by SN), |SP-SN|=5V	180	250	350	ns
$t_{PD-LOW-SN2}$			180	250	350	
$t_{PD-LOW-LPC1}$	Propagation Delay to OUT LOW	t_R+t_{PD}, (Trigger by LPC)	100	150	200	ns
$t_{PD-LOW-LPC2}$			100	150	200	
$t_{ON-MAX1}$	Maximum On Time		12	13	14	μs
$t_{ON-MAX2}$			12	13	14	μs

Continued on the following page…

Electrical Characteristics

V_{DD}=20V, T_A=25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
SP/SN Section						
$V_{N\text{-}P(turn\ off)\ 1}$	Threshold Voltage of V_N-V_P to Turn-Off SR MOS 1	Sweep $V_{N\text{-}P\text{-}}$ from LOW to HIGH	3	4	5	V
$V_{N\text{-}P(turn\ off)\ 2}$	Threshold Voltage of V_N-V_P to Turn-Off SR MOS 2		3	4	5	V
$V_{P\text{-}N(turn\ on)\ 1}$	Threshold Voltage of V_P-V_N to Turn-On SR MOS 1	Sweep $V_{P\text{-}N\text{-}}$ from LOW to HIGH	3	4	5	V
$V_{P\text{-}N(turn\ on)\ 2}$	Threshold Voltage of V_P-V_N to Turn-On SR MOS 2	Sweep $V_{P\text{-}N\text{-}}$ from LOW to HIGH	3	4	5	V
$Ratio\_{SP\text{-}SN}$	Voltage Difference between SP and SN	$\lvert V_{SP}\text{-}V_{SN}\rvert$ / $MIN(V_{SP},V_{SN})$			5	%
LPC Section						
$Ratio\_{LPC\text{-}RES}$	Charge Divide Discharge Current Transfer Ratio vs. Input Voltage	Connect a Diode 1N4148 and Divider (Ratio 12) to LPC, V_{DET} = 3V, V_{LPC} = 3V	2.79	3.00	3.21	
$V_{LPC\text{-}EN1}$	LPC Enable Threshold Voltage 1		1.8	2.0	2.2	V
$V_{LPC\text{-}EN2}$	LPC Enable Threshold Voltage 2		1.8	2.0	2.2	V
$V_{LPC\text{-}CLAMP1}$	Lower Clamp Voltage 1	I_{LPC} = -5μA	0.10	0.25	0.40	V
$V_{LPC\text{-}CLAMP2}$	Lower Clamp Voltage 2	I_{LPC} = -5μA	0.10	0.25	0.40	V
$I_{LPC\text{-}SOURCE1}$	Maximum Source Current 1	V_{LPC} = -0.3V		250	300	μA
$I_{LPC\text{-}SOURCE2}$	Maximum Source Current 2	V_{LPC} = -0.3V		250	300	μA
$V_{LPC\text{-}LOW1}$	Threshold Voltage for Disable LPC Function		1.3	1.5	1.7	V
$V_{LPC\text{-}LOW2}$	Threshold Voltage for Disable LPC Function		1.3	1.5	1.7	V
$t_{LPC\text{-}LOW1}$	Debounce Time for Disable LPC Function	$V_{LPC} < V_{LPC\text{-}LOW}$	70	100	130	μs
$t_{LPC\text{-}LOW2}$	Debounce Time for Disable LPC Function	$V_{LPC} < V_{LPC\text{-}LOW}$	70	100	130	μs

Typical Performance Characteristics

These characteristic graphs are normalized at T_A = 25°C.

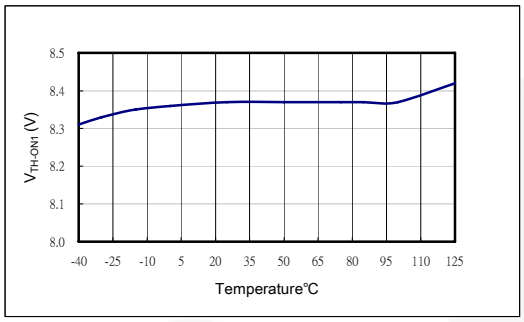


Figure 5. Turn-On Threshold Voltage 1

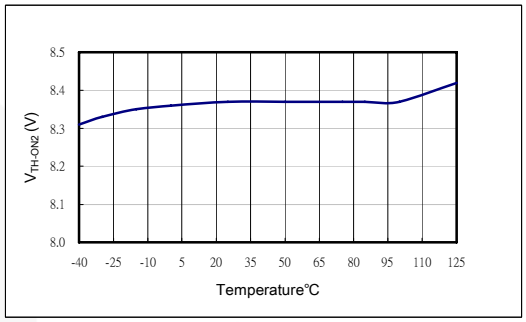


Figure 6. Turn-On Threshold Voltage 2

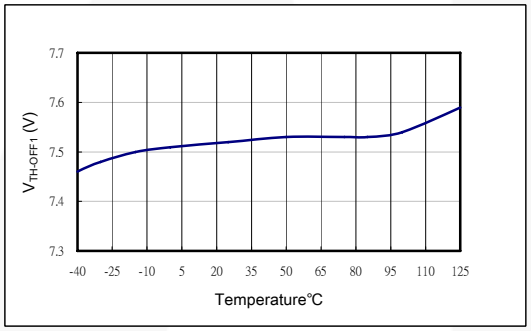


Figure 7. Turn-Off Threshold Voltage 1

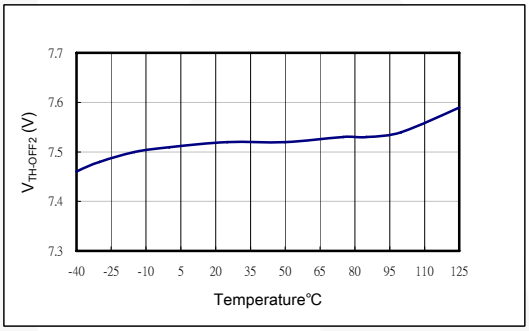


Figure 8. Turn-Off Threshold Voltage 2

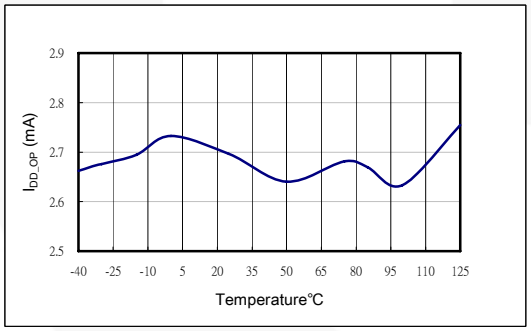


Figure 9. Operating Current

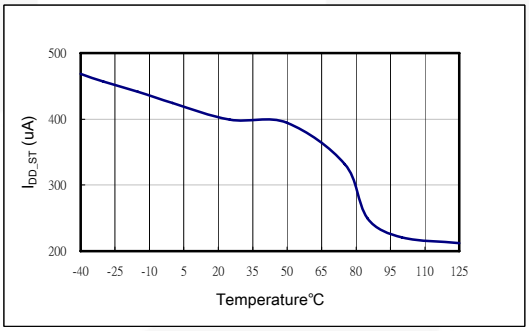


Figure 10. Startup Current

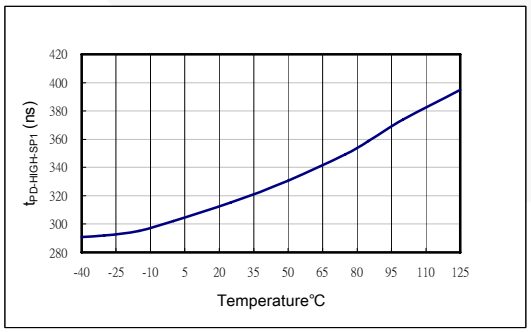


Figure 11. Propagation Delay to OUT HIGH 1 (Trigger by SP)

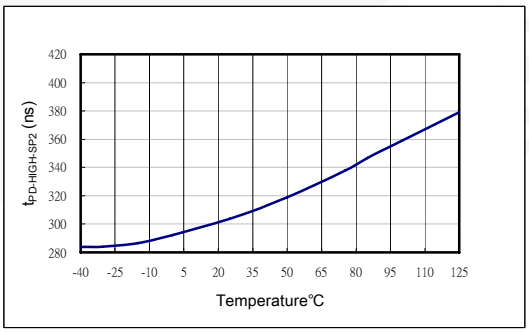


Figure 12. Propagation Delay to OUT HIGH 2 (Trigger by SP)

Typical Performance Characteristics

These characteristic graphs are normalized at T_A = 25°C.

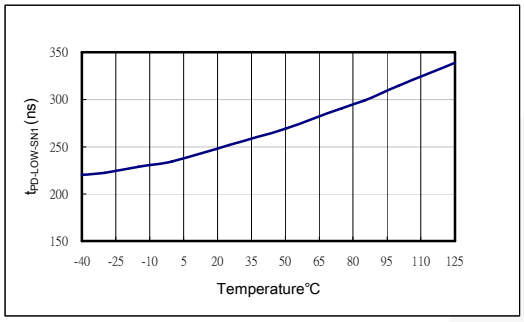


Figure 13. Propagation Delay to OUT LOW 1 (Trigger by SN)

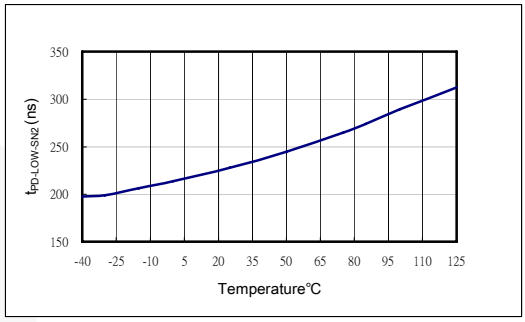


Figure 14. Propagation Delay to OUT LOW 2 (Trigger by SN)

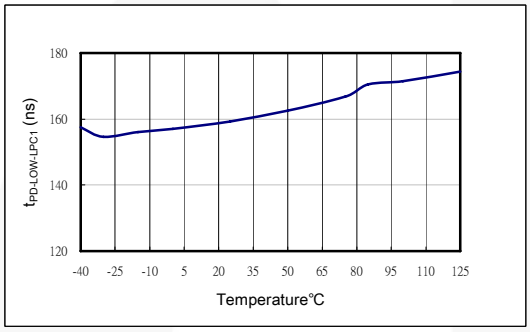


Figure 15. Propagation Delay to OUT LOW 1 (Trigger by LPC)

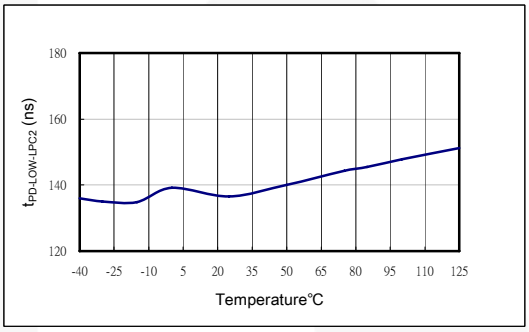


Figure 16. Propagation Delay to OUT LOW 2 (Trigger by LPC)

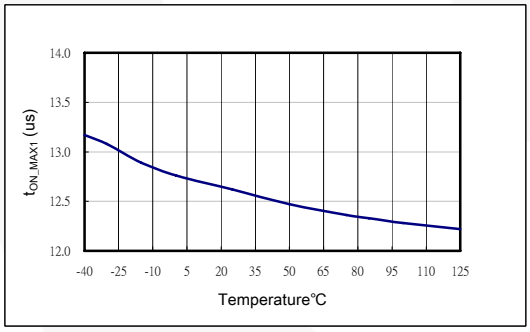


Figure 17. Maximum On Time 1

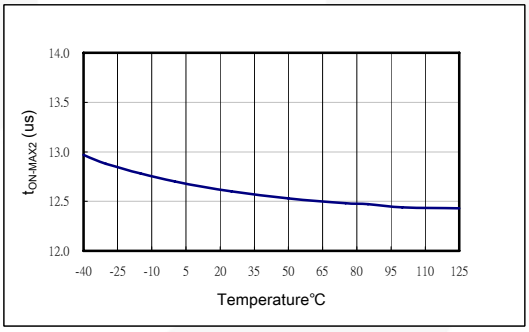


Figure 18. Maximum On Time 2

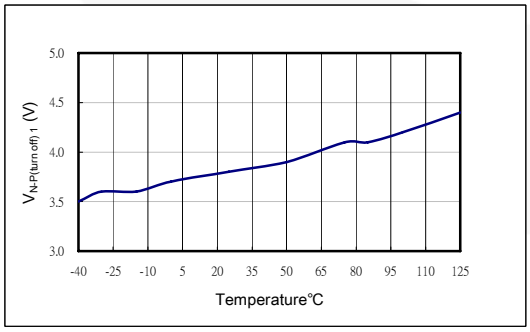


Figure 19. Threshold Voltage of V_N-V_P to Turn Off SR MOS 1

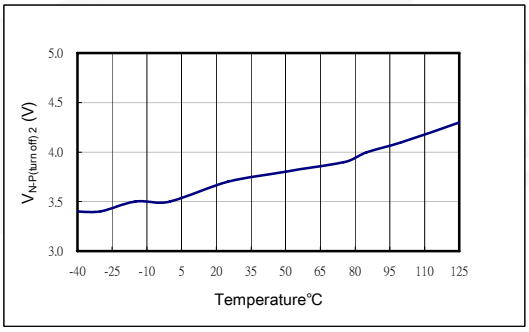


Figure 20. Threshold Voltage of V_N-V_P to Turn Off SR MOS 2

Typical Performance Characteristics

These characteristic graphs are normalized at T_A = 25°C.

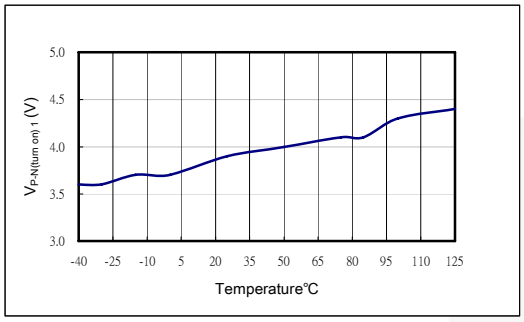


Figure 21. Threshold Voltage of VP-VN to Turn On SR MOS 1

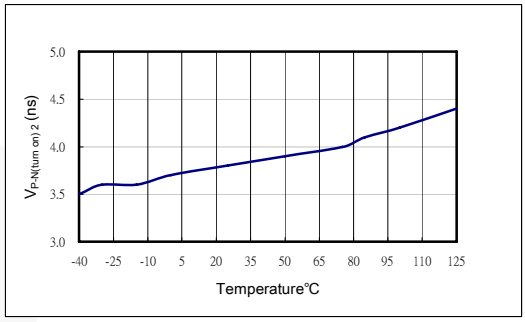


Figure 22. Threshold Voltage of V_P-V_N to Turn On SR MOS 2

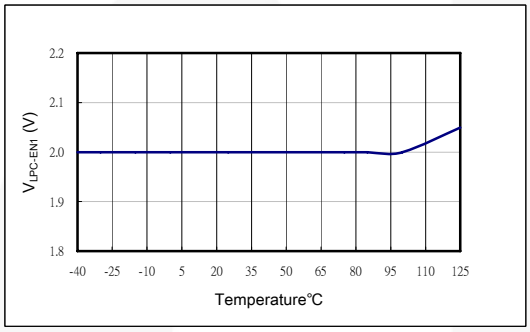


Figure 23. LPC Enable Threshold Voltage 1

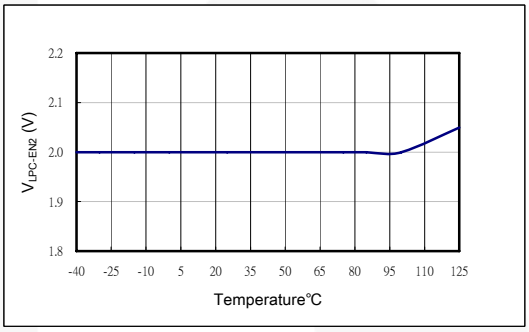


Figure 24. LPC Enable Threshold Voltage 2

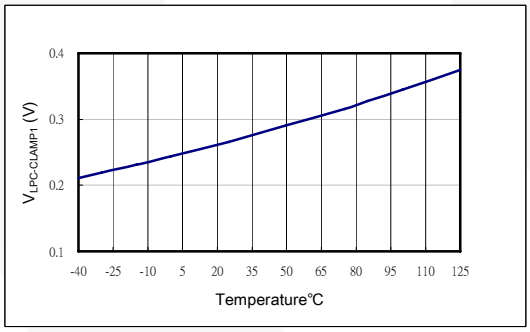


Figure 25. Lower Clamp Voltage 1

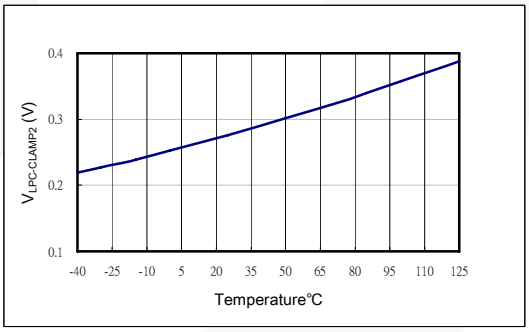


Figure 26. Lower Clamp Voltage 2

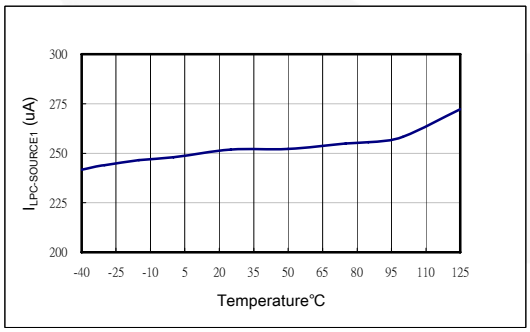


Figure 27. Maximum Source Current 1

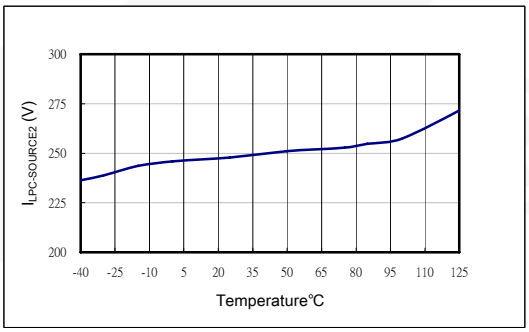


Figure 28. Maximum Source Current 2

Function Description

Figure 29 and Figure 30 show the simplified circuit diagram of a dual-forward converter and its key waveforms. Switches Q_1 and Q_2 are turned on and off together. Once Q_1 and Q_2 are turned on, input voltage is applied across the transformer primary side and power is delivered to the secondary side through the transformer, powering D_1. During this time, the magnetizing current linearly increases. When Q_1 and Q_2 are turned off, the magnetizing current of the transformer forces the reset diodes (D_{R1} and D_{R2}) and negative input voltage is applied across the transformer primary side. During this time, magnetizing current linearly decreases to zero and the secondary-side inductor current freewheels through diode D_2. When synchronous rectifier SR_1 and SR_2 are used instead of diodes D_1 and D_2, it is important to have proper timing between drive signals for SR_1 and SR_2.

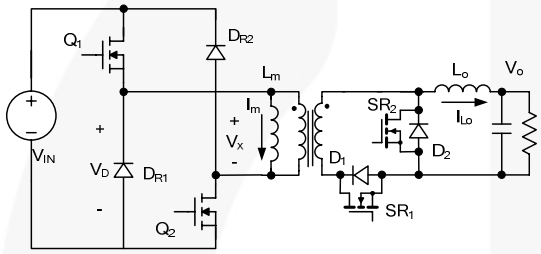


Figure 29. Simplified Circuit Diagram of Dual-Forward Converter

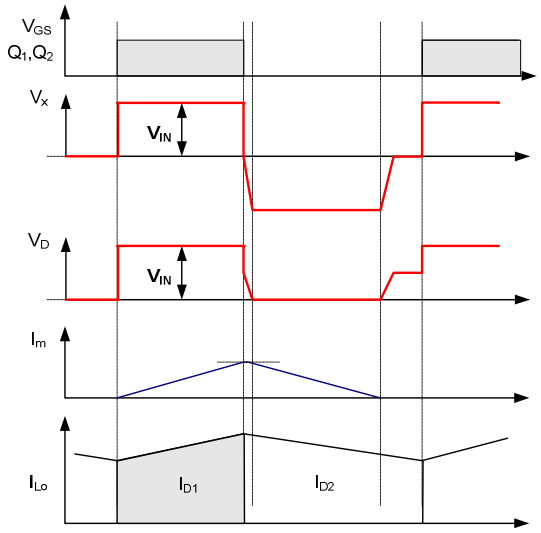


Figure 30. Key Waveforms of Dual-Forward Converter

Figure 31 shows a typical application circuit. When a dual-forward converter operates in continuous conduction mode, the SR gate signals (GATE1 and GATE2) are mainly controlled by SP and SN signals. SP and SN signals are transferred through a pulse transformer from XP and XN signals, which are generated by FAN6210 (Primary-Side Synchronous Rectifier Signal Trigger for Dual Forward Converter).

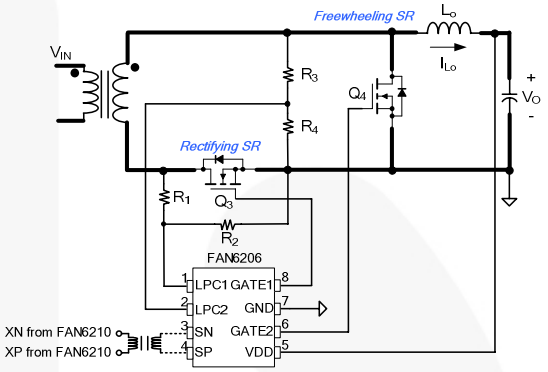


Figure 31. Typical Application Circuit

Figure 32 shows the timing diagram for continuous conduction mode (CCM). Figure 33 shows the timing diagram for discontinuous conduction mode (DCM).

The switching operation of SR MOSFETs Q_3 and Q_4 is determined by the SN and SP signals. FAN6206 turns on SR MOSFETs at the rising edge of the SP signal, while it turns off the SR MOSFETs at the rising edge of the SN signal. Within one switching cycle, SP and SN are obtained two times.

With a voltage divider R_1 and R_2 connected from LPC1 to secondary winding, R_3 and R_4 connected from LPC2 to secondary winding, the PWM timing sequences and frequency can be tracked precisely. The SR MOSFET is turned on by SP signal only when the voltage level on LPC1 or LPC2 pin is pulled LOW to GND.

During PWM-on period, the rectifying SR Q_3 is turned on by the rising edge of the SP signal after a propagation delay ($t_{PD\text{-}HIGH\text{-}SP1}$) and Q_3 is turned off by the rising edge of the SN signal after a propagation delay ($t_{PD\text{-}LOW\text{-}SN1}$). During PWM-off period, the freewheeling SR Q_4 is turned on by the rising edge of the SP signal after a propagation delay ($t_{PD\text{-}HIGH\text{-}SP2}$) and Q_4 is turned off by the rising edge of the SN signal after a propagation delay ($t_{PD\text{-}LOW\text{-}SN2}$) in CCM operation.

In DCM operation, the proprietary Linear-Predict Timing Control (LPC) technique can provide synchronous rectification control mechanism for freewheeling SR MOSFET. Since SN signal is sent following with PWM signal, the freewheeling SR MOSFET cannot be turned off in time by SN signal before I_{Lo} linearly decreases to zero. Therefore, the LPC mechanism is applied to turn off Q_3 in DCM mode.

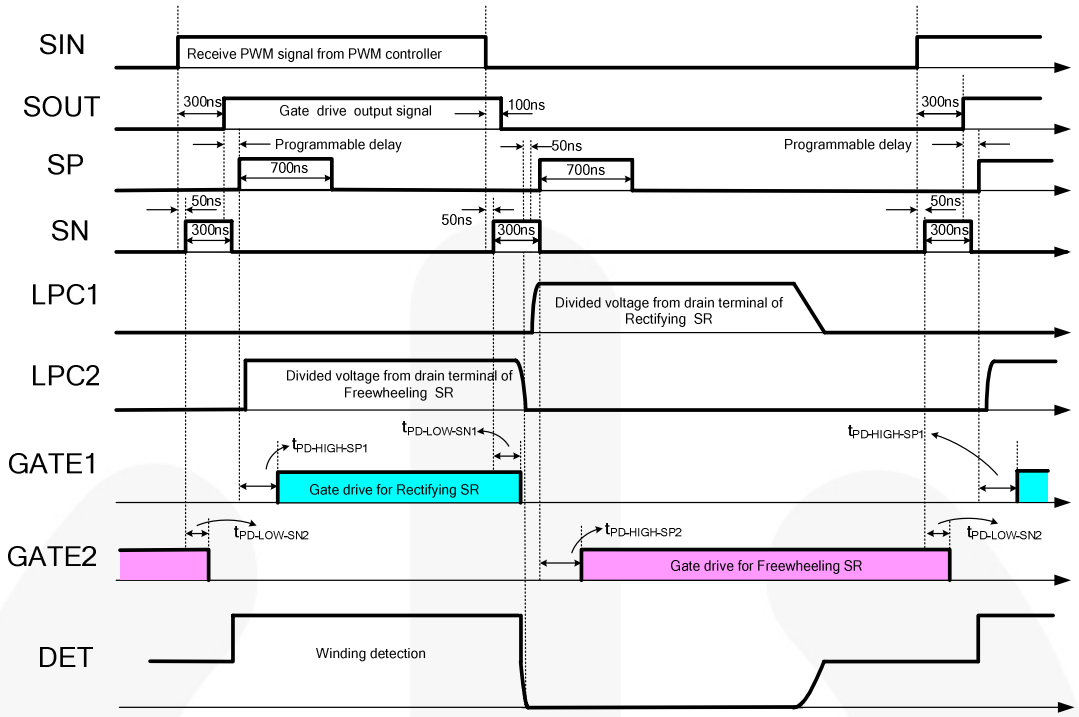


Figure 32. SR Gate is Driven by SP & SN Signal in CCM Mode

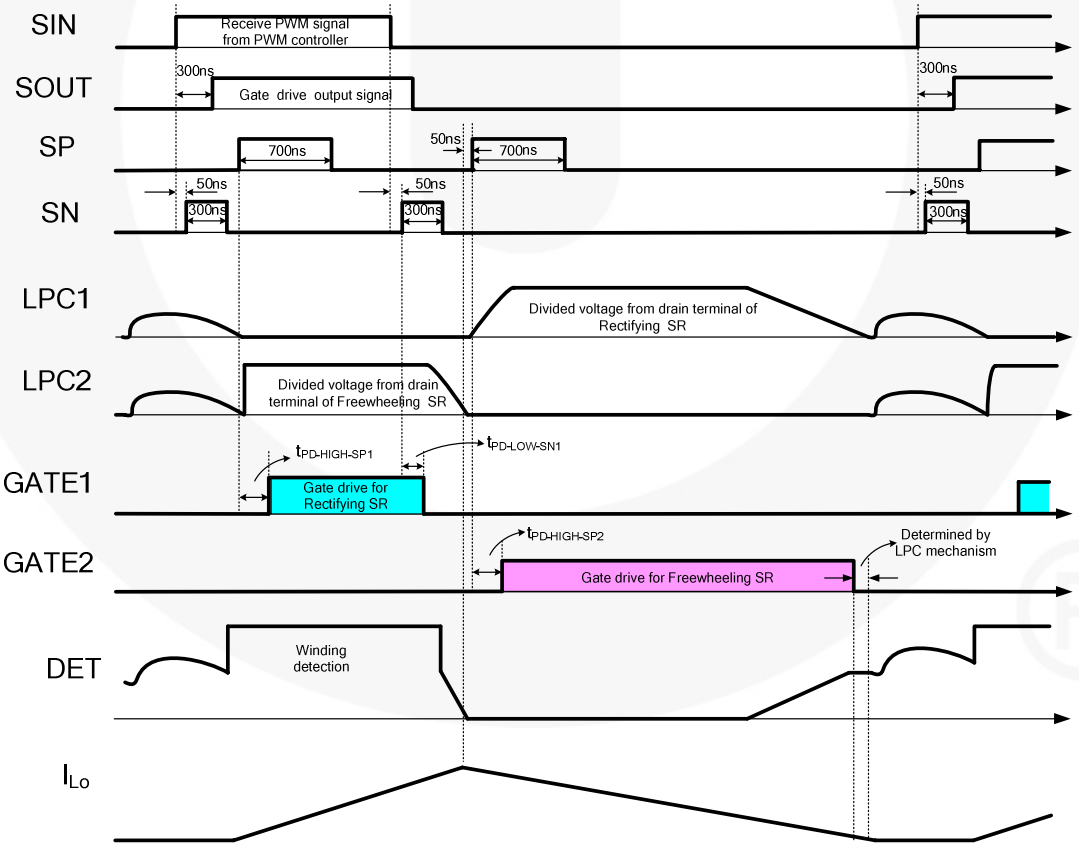


Figure 33.Freewheeling SR Turned Off by LPC Mechanism in DCM Mode

Linear-Predict Timing Control

When a dual-forward converter operates in CCM or DCM; in PWM t_{ON} period, the V_{IN} voltage is applied to the primary winding and the secondary inductor starts to rise linearly and store energy. The across voltage on secondary winding is coupled from primary winding and proportional to V_{IN}. The SR controller can detect this winding voltage through a voltage divider and acquire the V_{IN} level. According to this detected V_{IN} level during PWM turn-on period, SR controller produces a charge current I_{CHG} to charge internal capacitor, CT, of the SR controller. On the other hand, at PWM turn-off period, the energy stored in the secondary inductor is discharged. The SR controller also detects the output voltage level to modulate discharge current I_{DISCHG} of internal capacitor, CT. Once the internal capacitor voltage reaches zero, SR controller turns off SR MOS immediately.

R_4 is connected between the LPC2 pin and the drain terminal of Q_4. During PWM turn-on period, voltage on the LPC2 pin is pulled HIGH due to the secondary winding coupled from primary winding. At this moment, SR MOS is turned off and the internal body diode of SR MOS is reverse-biased. During PWM turn-off period, the potential on the primary winding reverses and the internal body diode starts to conduct output current. The voltage on the LPC2 pin is also pulled LOW to GND. R_2 is recommended as 10kΩ and the divided voltage level on the LPC1 pin is suggested between 3V~5V. If the voltage level of V_O is 12V, the resistor values are recommended as 105kΩ for R_3 and 10kΩ for R_4. The turn-off timing of Q_4 is determined by the ratio $\frac{R_4}{R_3+R_4}$ as Figure 34 shows. If $\frac{R_4}{R_3+R_4}$ decreases, Q_4 is turned off earlier.

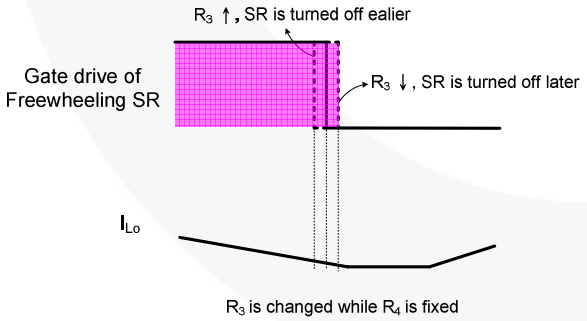


Figure 34. Turn-Off Timing of Freewheeling SR

Under-Voltage Lockout (UVLO)

The power-on and off thresholds are fixed at 8.5V and 7.5V. The VDD pin is connected to a 12V output voltage terminal.

VDD Pin Over-Voltage Protection

The over-voltage conditions are usually caused by open feedback loops. V_{DD} over-voltage protection is built in to prevent damage if over voltage occurs. When the voltage on the VDD pin exceeds 21V, the SR controller turns off all of SR MOS operations.

Typical Application Circuit (Dual-Forward Converter with SR)

Application	Fairchild Devices	Input Voltage Range	Output
PC Power	FAN4801 FAN6210 FAN6206	90~264V_{AC}	12V/25A

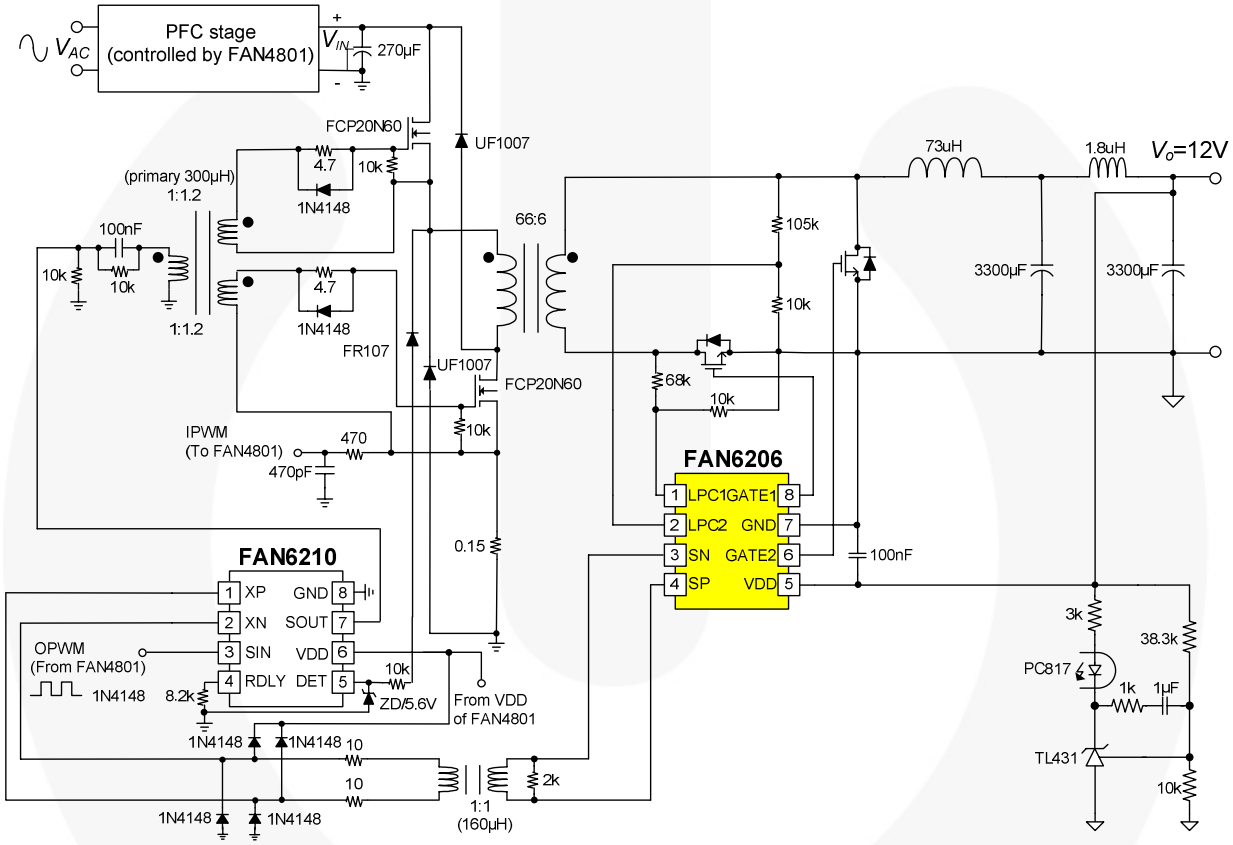


Figure 35. Application Circuit

Physical Dimensions

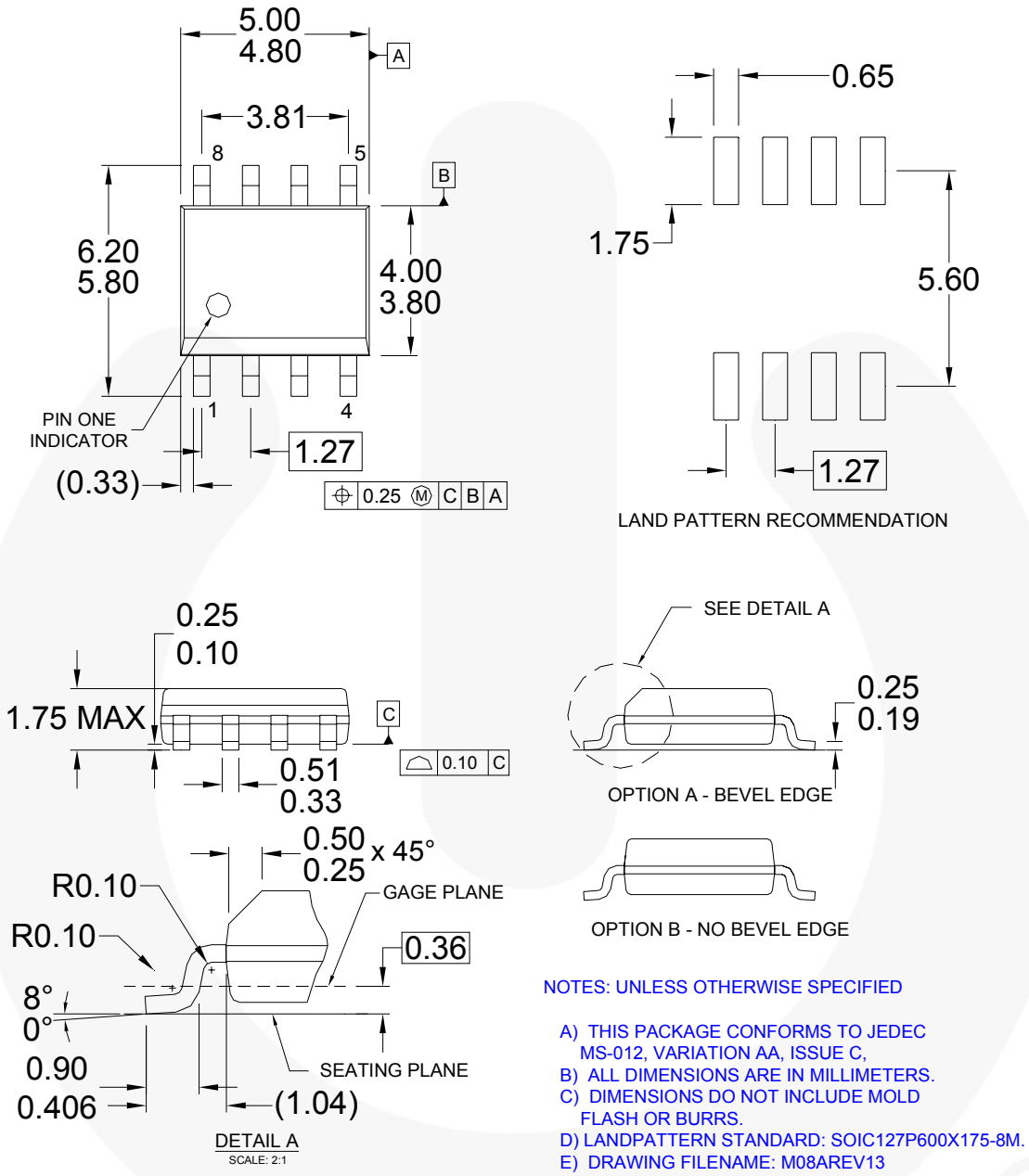


Figure 36. 8-Pin Small Outline Package (SOP)

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