Audio Accessory ICs for Mobile Devices

Mixer & Selector ICs with 16bit D/A Converter

BU7858KN,BU7893GU

No.10087EAT03

●Description

This LSI is mounted with stereo 16bit D/A Converter and suitable for higher sound quality and miniaturization of cellular phone with music play. BU7893GU has a 3D surround enhancement function and hence can play the wide-spreading stereo sound from stereo speakers that are arranged nearby.

●Features

1) Mounted with Stereo 16bit audio D/A converter
2) Compatible with Stereo analogue interface
3) Stereo headphone amplifier (16Ω)
4) Low-band corrective circuit in headphone amplifier
5) Volume that can adjust the gain
6) Flexible mixing function

●Applications

Portable information & communication equipments such as cellular phone and PDA (Personal Digital Assistant) etc.
Cellular phone with music play

●Line up matrix

Function	BU7858KN	BU7893GU
Stereo audio D/A converter	16bit	16bit
Stereo audio interface format	16bit Right justified 18bit Right justified IIS	16bit Left justified 16bit Right justified IIS
3D surround enhancement function	No	Yes
3 band equalizer	No	Yes
Stereo headphone amplifier	16Ω driver	16Ω driver
Line output (600Ω driver)	Yes	No
Headphone amplifier low-band correction function	Built-in	Built-in
Click noise reduction function	Yes (headphone only)	Yes
Package	VQFN28	VCSP85H3

●Absolute maximum ratings

Parameter		Symbol	Ratings	Unit
Power-Supply Voltage	BU7858KN	VDD	-0.3 ～ 4.5	V
	BU7893GU	DVDDIO AVDD	-0.3 ～ 4.5	V
		DVDDCO	-0.3 ～ 2.5	
Power Dissipation	BU7858KN	Pd	580 *1	mW
	BU7893GU		700 *2	
Operating Temperature	BU7858KN	T_{OPR}	-20 ～ +85	℃
	BU7893GU		-30 ～ +85	
Storage Temperature	BU7858KN	T_{STG}	-55 ～ +125	℃
	BU7893GU		-50 ～ +125	

*1 : 5.8mW is decreased every 1℃ when using it over 25℃. (Mounted on the ROHM standard PCB)
*2: 7.0mW is decreased every 1℃ when using it over 25℃.

●Operating conditions

【BU7858KN】

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Power-Supply Voltage	VDD	2.7	3.0	3.3	V

【BU7893GU】

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Analog Power-Supply Voltage	AVDD	2.6	2.8	3.3	V
Digital I/O Power-Supply Voltage	DVDDIO	DVDDCO	1.8	3.3	V
Digital Core Power-Supply Voltage	DVDDCO	1.62	1.8	1.98	V

●Electrical characteristics

【BU7858KN】

Unless otherwise specified, Ta=25℃, AVDD=DVDD=3.0V

・Analog

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Current Consumption	Idd3	-	2.3	3.7	mA	16Ω driver part and no signal
DAC S/(N+D)	SN+D	-	85	-	dB	fs=44.1kHz, fin=1kHz, 20kHz LPF, Vin=-0.5dBFS
DAC S/N	SNR	-	92	-	dB	fs=44.1kHz, fin=1kHz , A-weighted, Vin=0dBFS
Headphone Amplifier Total Harmonic Distortion	THDhp	-	0.05	0.5	%	fin=1kHz, 20kHz LPF, Vin=-10dBV
Headphone Amplifier Maximum Output	PO	-	10	-	mW	fin=1kHz, THD=10%, RL=16Ω
Headphone Amplifier Output Noise Voltage	VNO	-	-94	-80	dBV	A-weighted
SPO Maximum Output Level	VOMAX1	2.0	-	-	V_{P-P}	fin=1kHz, THD≦1%, 10kΩLoad
EXTO Maximum Output Level	VOMAX2	2.0	-	-	V_{P-P}	fin=1kHz, THD≦1%, 600ΩLoad

・Digital (DC)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Digital Input Voltage “L”	VIL	-	-	0.2 x DVDD	V	
Digital Input Voltage “H”	VIH	0.8 x DVDD	-	-	V	
Digital Output Voltage “L”	VOL	-	-	0.5	V	Iol=-500μA
Digital Output Voltage “H”	VOH	DVDD -0.5	-	-	V	Ioh=500μA
Input Leakage Current 1	IIN1	-	-	±2	μA	at 0V, 3V

・Audio Interface

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
MCLKI Frequency	fMCLK	4.096	-	18.432	MHz	
MCLKI Duty Ratio	dMCLK	45	-	55	%	
LRCLK Frequency	fs	16	-	48	kHz	
LRCLK Duty Ratio	dLR	45	-	55	%	
BCLK Frequency	fBCK	0.512	-	3.072	MHz	
BCLK Duty Ratio	dBCK	45	-	55	%	
LRCLK edge to BCLK↑ Time	tLRS	50	-	-	ns	
BCLK↑ to LRCLK Edge Time	tSLR	50	-	-	ns	
Data Hold Time	tSDH	50	-	-	ns	
Data Set-up Time	tSDS	50	-	-	ns	

【BU7893GU】

・Whole Block

Unless otherwise specified, Ta=25℃, DVDD_CORE=1.8V, DVDD_IO=1.8V, AVDD=2.8V, Digital input terminal is fixed with DVDD_IO “L” or “H” level, The gain settings of the audio paths are all 0dB, and no signal

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
DVDD_CORE Stand-by Current (Core logic block)	ISTCO	-	-	10	μA	standby,CLKI = DVSS
DVDD_IO Stand-by Current	ISTIO	-	-	5	μA	standby,CLKI = DVSS
AVDD Stand-by Current	ISTA	-	-	5	μA	standby
DVDD_CORE Operation Current	IDDCO	-	5	10	mA	
DVDD_IO Operation Current	IDDIO	-	0.1	1	mA	BCLK,LRCLK = Input mode MCLK = L output
AVDD Operation Current 1 (Analog melody)	IDDA1	-	1.6	2.8	mA	ANAINL→MIX1→SPOL ANAINR→MIX2→SPOR
AVDD Operation Current 2 (Digital melody)	IDDA2	-	6.0	10.0	mA	SDI→MIX1→SPOL SDI→MIX2→SPOR TCXOI = 19.8MHz,fs = 44.1kHz

・DC Characteristic

Parameter	Symbol	Terminal	Limits		Unit	Conditions
			Min.	Max.		
L Output Voltage	All output terminal※1	Vold	0	0.30	V	Iol=+0.8mA
H Output Voltage	All output terminal※1	Vohd	DVDD_IO -0.30	DVDD_IO	V	Ioh=-0.8mA
L Level Input Voltage1	All input terminal※2	Vild1	-0.3	DVSS+0.5	V	
L Level Input Voltage 2	CLKI※3	Vild2	-0.3	※3	V	
H Level Input Voltage 1	All input terminal※2	Vihd1	DVDD_IO -0.5	DVDD_IO +0.3	V	
H Level Input Voltage 2	CLKI※3	Vihd2	※3	DVDD_CORE +0.3	V	
L Level Input Current	All input terminal※2	Iild	-1	1	μA	Input terminal voltage is DVSS
H Level Input Current 1	All input terminal※2	Iihd1	-1	1	μA	Input terminal voltage is DVDD_IO
H Level Input Current 2	CLKI※3	Iihd2	-1	1	μA	Input terminal voltage is DVDD_CORE
Output OFF Current	Hi-Z terminal※4	Iozd	-10	10	μA	

※1 : They also contain interactive terminals that are set output state.
※2 : They also contain interactive terminals that are set input state.
※3 : Please connect 100pF coupling capacitor and input $0.5V_{P-P}$ or more when you input through coupling capacitor.
(In address 15h CLKSEL1=0, CLKSEL0=1)
※4 : At interactive terminals of input state or three-state terminals of output-disable state

・Audio Path(MIX)

Unless otherwise specified, Ta=25℃, AVDD=2.8V, reference input level=-6dBV, f=1kHz, A-weighted, path gain =0dB

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
ANAL_V Volume Setting	G_{DACL}	-11	-	+3	dB	1dB step
ANAR_V Volume Setting	G_{DACR}	-11	-	+3	dB	1dB step

・Audio Path (SP PREamp)
Unless otherwise specified,Ta=25℃,AVDD=2.8V, Reference input level =-6dBV, f=1kHz,
A-weighted, path gain =0dB, RL=33kΩ

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
THD+N	THD_{SP}	-	-70	-60	dB	20kHz LPF
Output Noise Voltage	V_{NOSP}	-	-90	-80	dBV	At no a signal
Mute Level	ML_{SP}	-	-90	-80	dB	1kHz BPF

・Audio Path (HP amp)
Unless otherwise specified, Ta=25℃, AVDD=2.8V, reference input level =-6dBV, f=1kHz,
A-weighted, path gain =0dB, RL=16Ω

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
THD+N	THD_{HP}	-	-65	-55	dB	20kHz LPF
Output Noise Voltage	V_{NOHP}	-	-90	-80	dBV	At no signal
The Maximum Output Power	P_{OHP}	10	-	-	mW	THD=10%,16Ω load
Channel Separation	CS_{HP}	-	-80	-70	dB	Vo=-14dBV,1kHz BPF
Mute Level	ML_{HP}	-	-90	-80	dB	1kHz BPF
HPL_V Volume Setting 1	$GA1_{HPL}$	-48	-	0	dB	2dB step
HPL_V Volume Setting 2	$GA2_{HPL}$	-42	-	+6	dB	2dB step
HPR_V Volume Setting 1	$GA1_{HPR}$	-48	-	0	dB	2dB step
HPR_V Volume Setting 2	$GA2_{HPR}$	-42	-	+6	dB	2dB step

・3D Surround, Equalizer, and Audio DAC
Unless otherwise specified, Ta=25℃, AVDD=2.8V, BCLK=64fs, LRCLK=256fs, f=1kHz, path gain=0dB,
SPOL/SPOR output, SPOL/SPOR= no load, output=0dBFS

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Full-scale Amplitude	VMAX	1.40	1.68	2.00	V_{P-P}	0.6×AVDD
S/N1 (A-Weighted)	DAC_{sn1}	70	75	-	dB	
THD+N1 (20kHz LPF)	DACthd1	-	-70	-60	dB	fs=8,11.025kHz
THD+N2 (20kHz LPF)	DACthd2	-	-75	-65	dB	fs=16,22.05,32,44.1,48kHz

・Audio I/F Format
Unless otherwise specified, Ta=25℃, DVDD_IO=1.62～3.3V, DVDD_CORE=1.62～1.98V

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
BCLK Output Frequency	FBCKO	0.512	-	3.072	MHz	64fs
LRCLK Output Frequency	FLRCKO	8	-	48	kHz	
SDI Set-up Time	tSDSU	100	-	-	nsec	
SDI Hold Time	tSDH	100	-	-	nsec	

・PLL
Unless otherwise specified, Ta=25℃, AVDD=2.8V, BCLK = no load

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
PLL Lock-up Time	Tlock1	-	-	10	msec	
PLL Jitter	Tjitter1	-	200	-	psec	BCLK terminal,f_{VCO}=65.536MHz

●Reference Data

【BU7858KN】

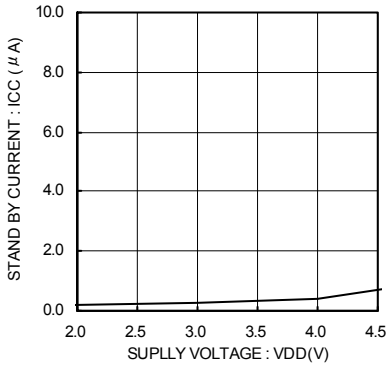


Fig.1 Stand-by Current

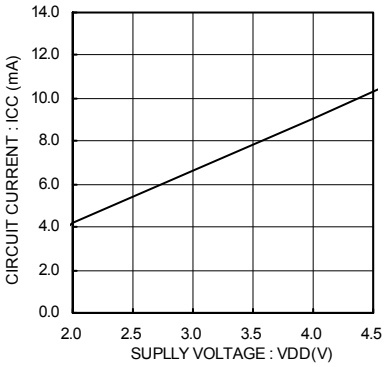


Fig.2 16bit D/A Converter Operation Current

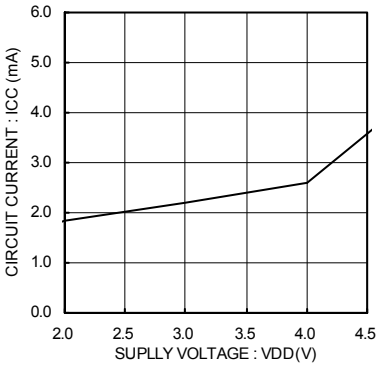


Fig.3 Headphone Amplifier Operation Current

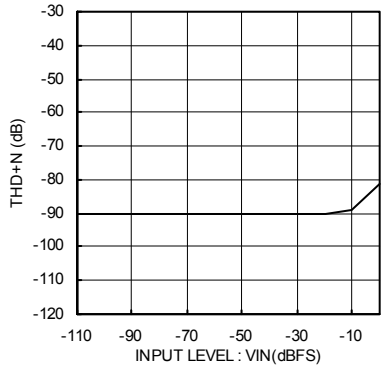


Fig.4 16bit D/A Converter Total Harmonic Distortion (Lch)

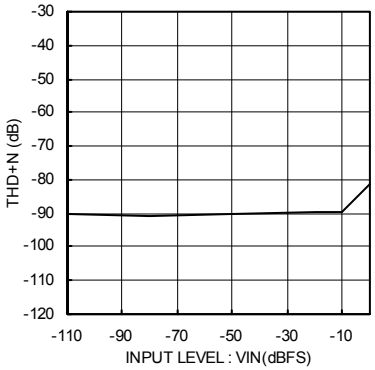


Fig.5 16bit D/A Converter Total Harmonic Distortion (Rch)

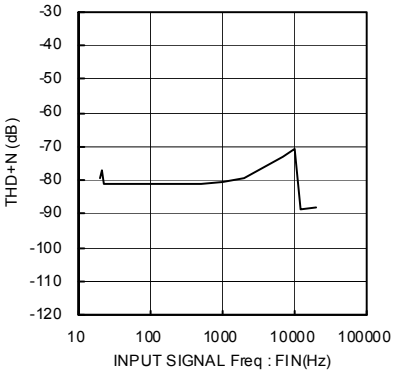


Fig.6 16bit D/A Converter Total Harmonic Distortion (Lch)

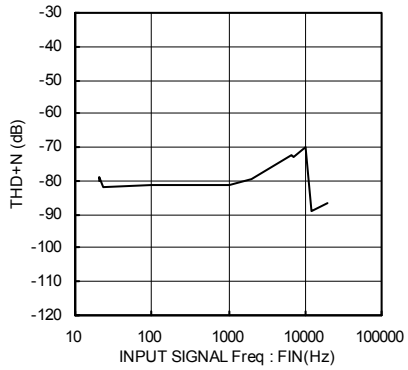


Fig.7 16bit D/A Converter Total Harmonic Distortion (Rch)

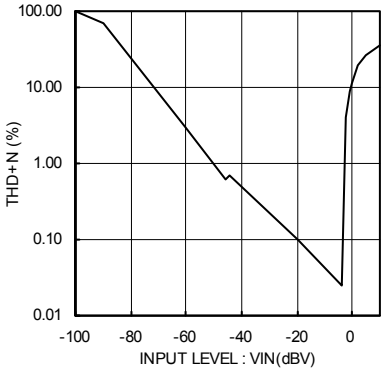


Fig.8 Headphone Amplifier Total Harmonic Distortion (HP_L)

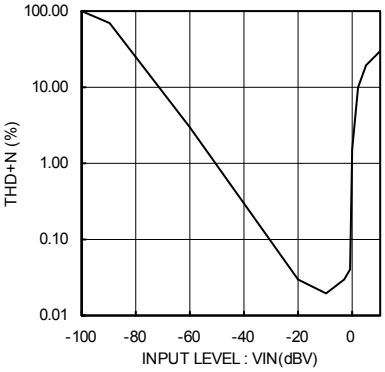


Fig.9 Headphone Amplifier Total Harmonic Distortion (HP_R)

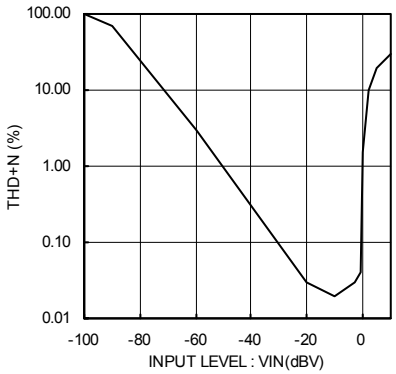


Fig.10 SPO Total Harmonic Distortion

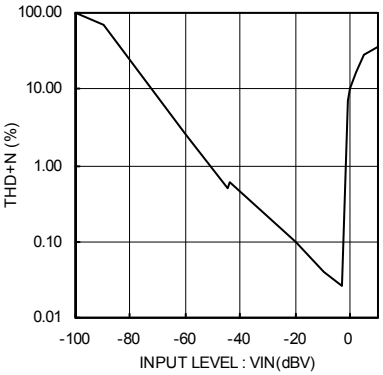


Fig.11 EXTO Total Harmonic Distortion

【BU7893GU】

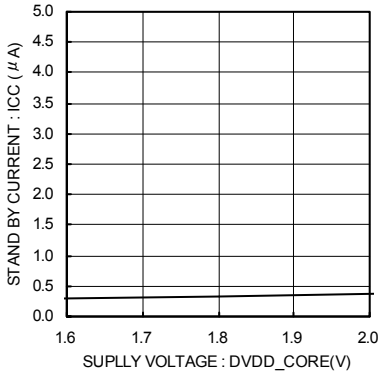


Fig.12 DVDD_CORE
Standby Current

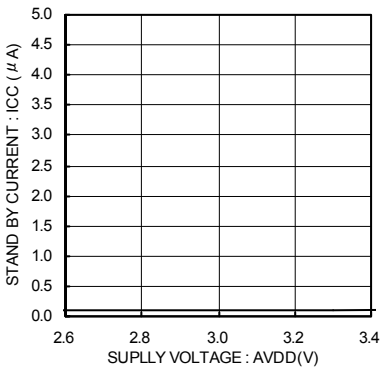


Fig.13 AVDD
Standby Current

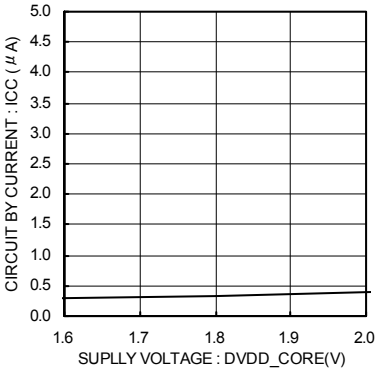


Fig.14 DVDD_CORE
Operation Current (Analog melody)

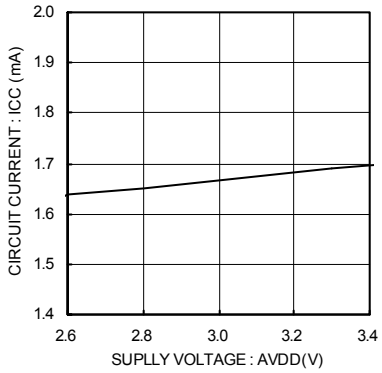


Fig.15 AVDD
Operation Current (Analog melody)

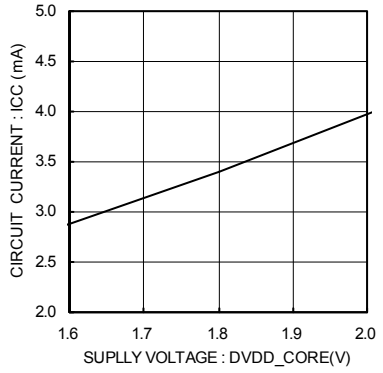


Fig.16 DVDD_CORE
Operation Current (digital melody)

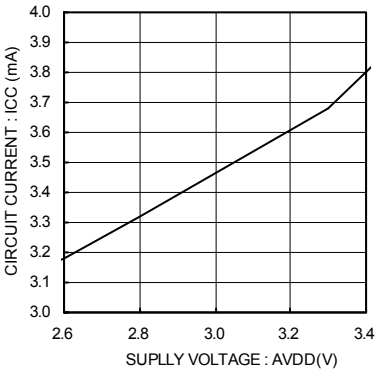


Fig.17 AVDD
Operation Current (digital melody)

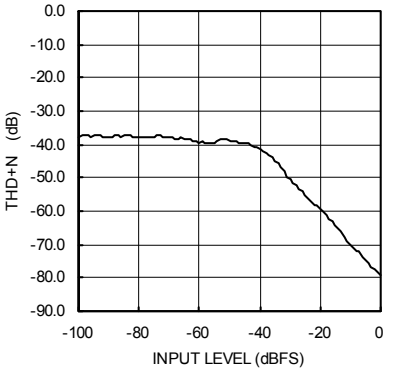


Fig.18 16bit D/A Converter
Total Harmonic Distortion 1kHz (SPOL)

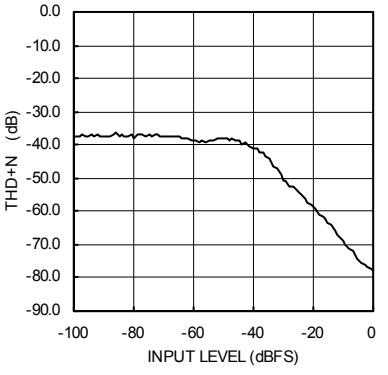


Fig.19 16bit D/A Converter
Total Harmonic Distortion 1kHz (SPOR)

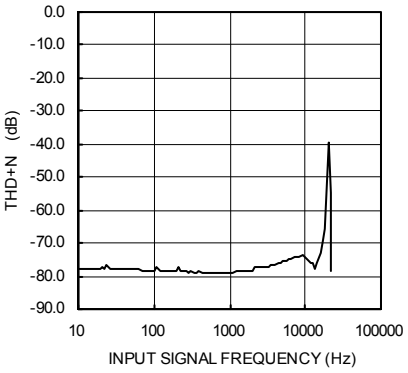


Fig.20 16bit D/A Converter
Total Harmonic Distortion (SPOL)

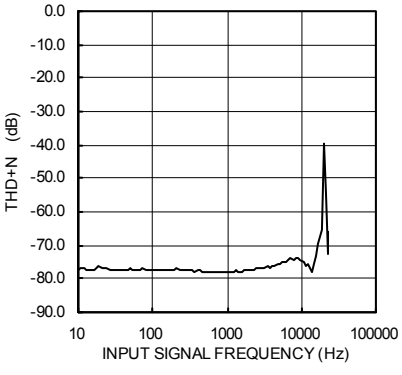


Fig.21 16bit D/A Converter
Total Harmonic Distortion (SPOR)

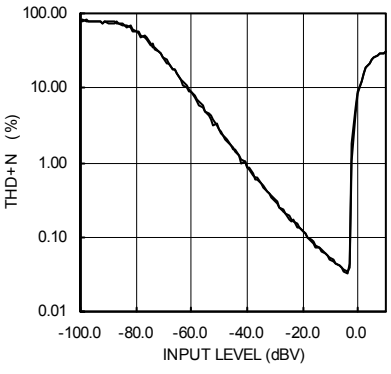


Fig.22 Headphone Amplifier
Total Harmonic Distortion (HPOL / HPOR)

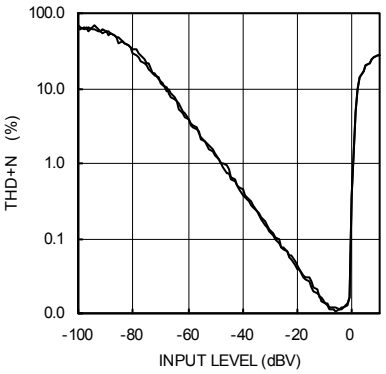


Fig.23 Speaker Preamp
Total Harmonic Distortion (SPOL / SPOR)

●**Block diagram and pin assignment**

【BU7858KN】

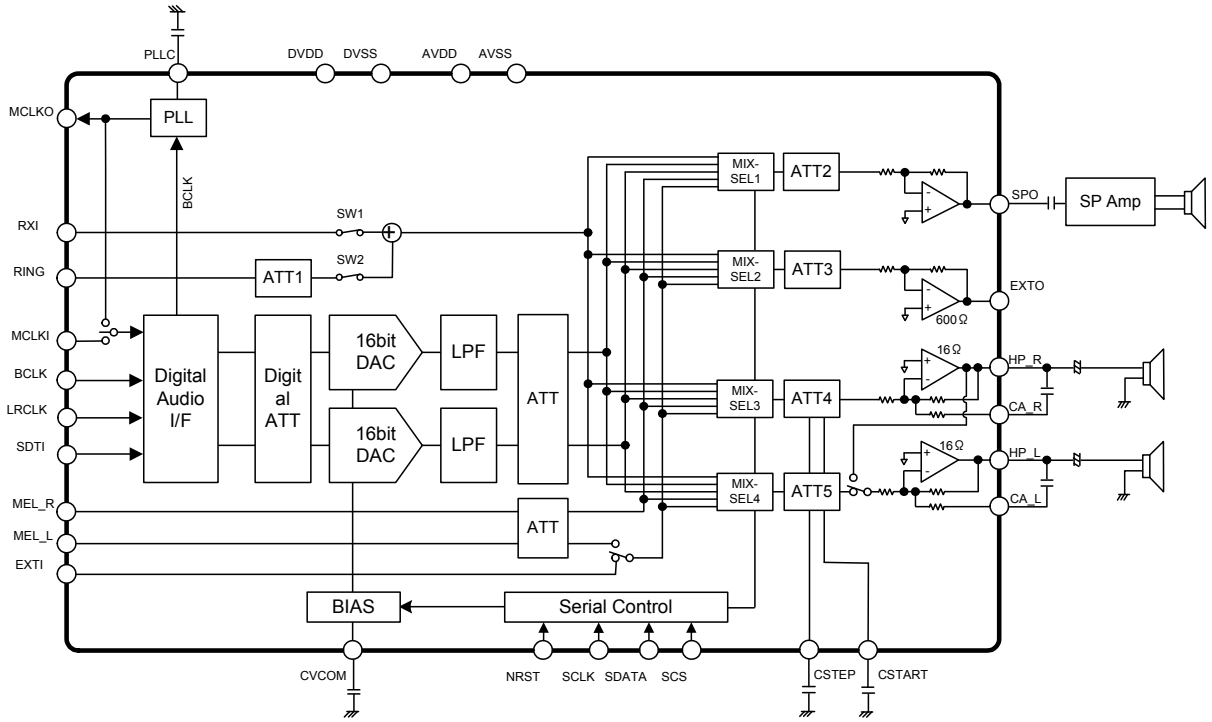


Fig.24 BU7858KN Block Diagram

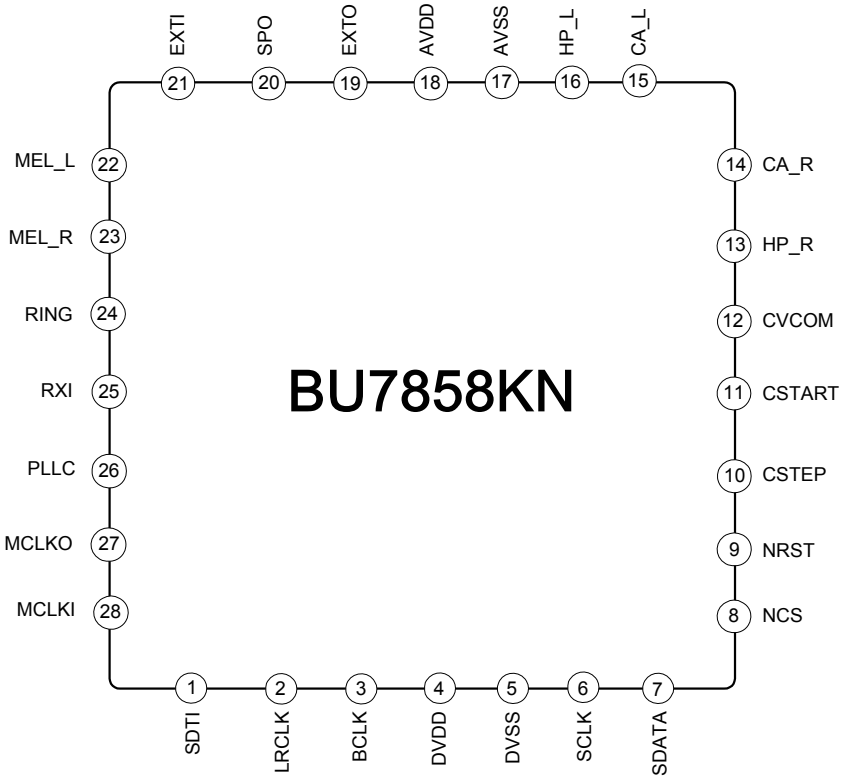


Fig.25 BU7858KN Pin Assignment (TOP VIEW)

【BU7893GU】

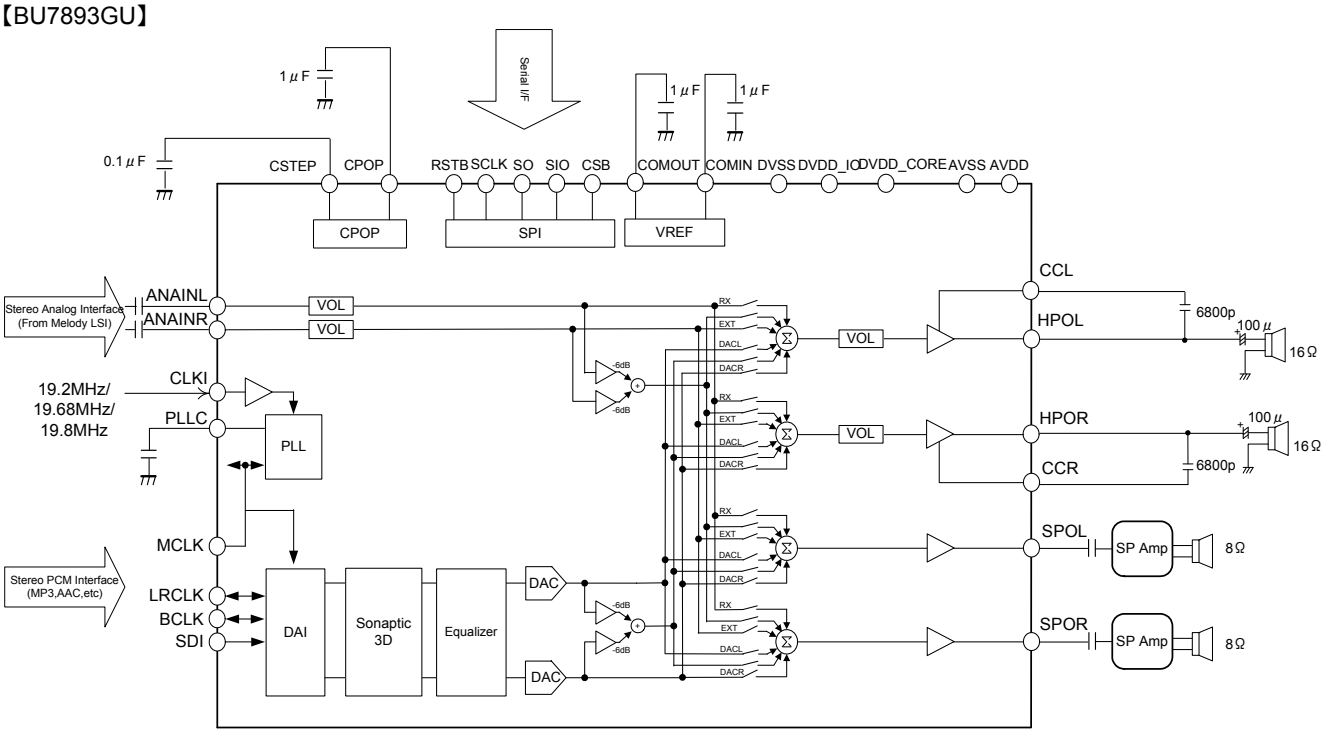


Fig.26 BU7893GU Block diagram

	1	2	3	4	5	6
A	TEST3	HPOR	HPOL	CPOP	SPOL	TEST4
B	CCR	RSTB	DVSS	CCL	SPOR	COMIN
C	SCLK	SO			CSTEP	AVSS
D	SIO	MCLK			COMOUT	ANAINR
E	CSB	PLLC	AVDD	DVDD_CORE	SDI	ANAINL
F	TEST2	CLKI	DVDD_IO	BCLK	LRCLK	TEST1

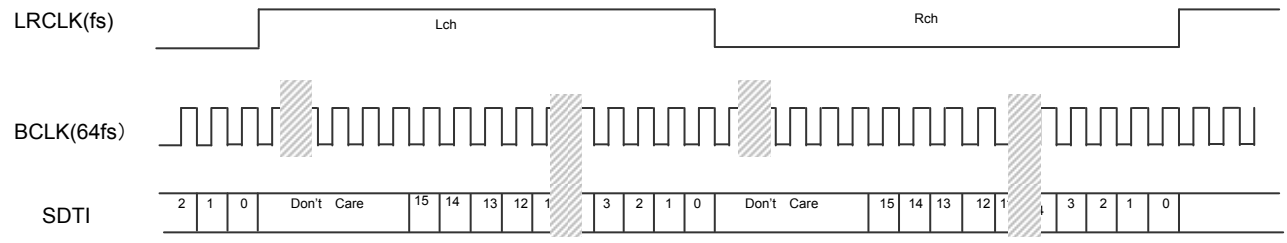
(TOP VIEW)

Fig.27 BU7893GU Ball Assignment

●Digital interface of 16 bit audio D/A converter

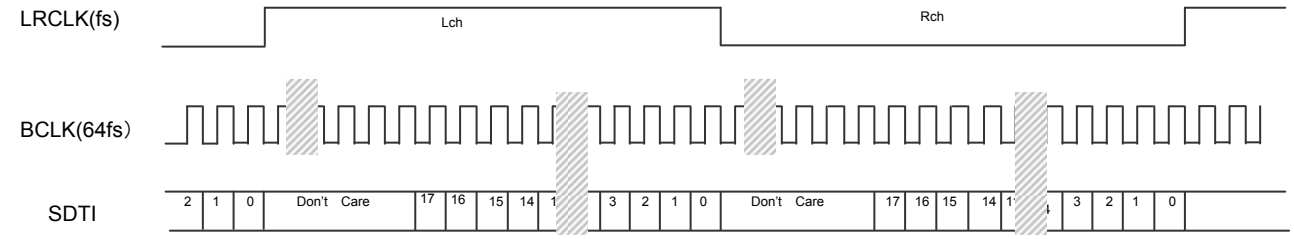
16bit audio D/A converter equipped with this series can be used with the following audio format.
【BU7858KN】

1) MSB first 16bit data (Right justified)



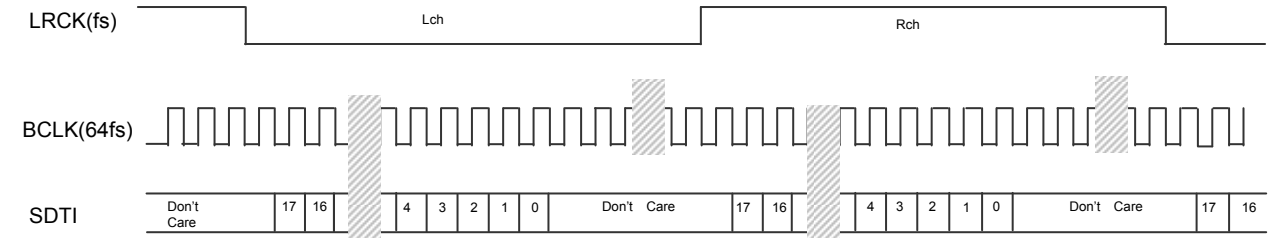
15:MSB, 0:LSB

2) MSB first 18bit data (Right justified)



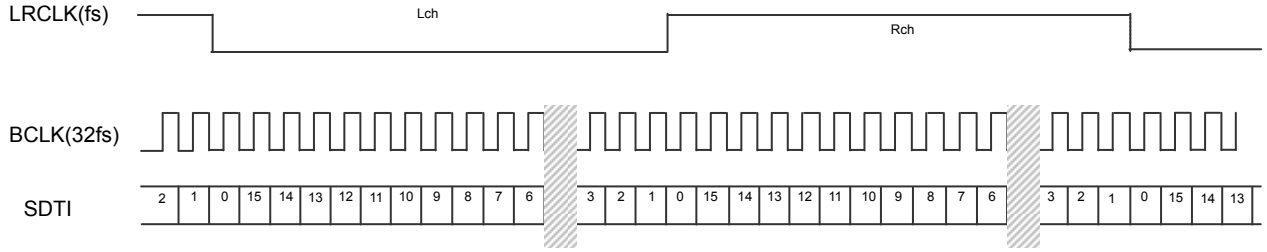
17:MSB, 0:LSB

3) IIS mode 18bit data (Left justified)



17:MSB, 0:LSB

4) IIS mode 16bit data (BCLK=32fs)



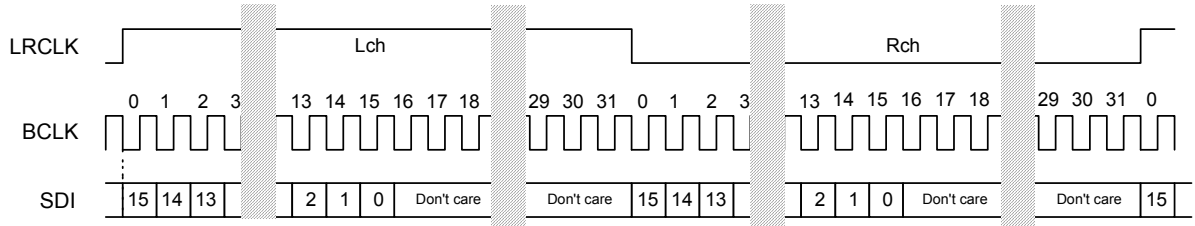
15:MSB, 0:LSB

Fig.28 AUDIO I/F FORMAT (BU7858KN)

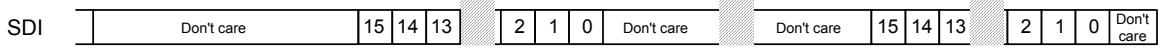
BU7858KN is provided with a mode that generates MCLK (Master Clock) by using the built-in PLL, so it is possible to make a D/A converter operate even if the clocks are only BCLK (64fs/32fs), LRCLK (fs).
The PLL generates MCLK (Master Clock), which is necessary for driving of D/A converter, from BCLK (Bit Clock).
Please connect a capacitor (PLLC) for the filter with DVSS. Moreover, please place the capacitor nearest DVSS of IC in order to reduce the noise interference.
Then it is possible to monitor the master clock that is generated internally from MCLKO, which is after all the monitor terminal, and hence does not guarantee drivability and phase-margin.
Please tie the MCLKI terminal to DVSS when PLL is used. And please tie the PLLC terminal to DVSS when PLL is not used. Moreover, it is not necessary to set the “PLLPDN” and “SMPR” when PLL is not used.

【BU7893GU】

1. MSB first left justified format



2. MSB first right justified format



3. IIS format

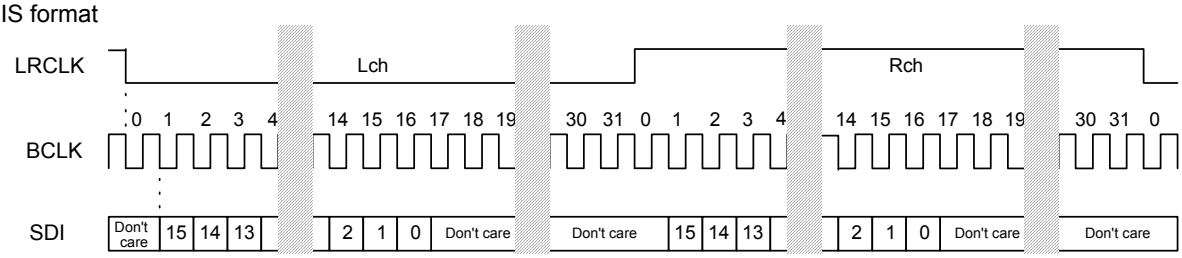


Fig.29 AUDIO I/F Format (BU7893GU)

●3D Surround enhancement function

【BU7893GU】

Even under the circumstances of adjacent arrangement of stereo speakers, the wide-spreading acoustic effect can be achieved because of the output resulting from the digital audio input to which the 3D surround effect has been applied. Moreover, the stereo sound at the time of audio recording can also be played truly. Please tell us about the parameter setting when you use this function.

●Low-band corrective circuit

In the headphone output terminals (HP_L, HP_R or HPOL, HPOR), there is a low-band corrective circuit, which corrects the low-band attenuation.

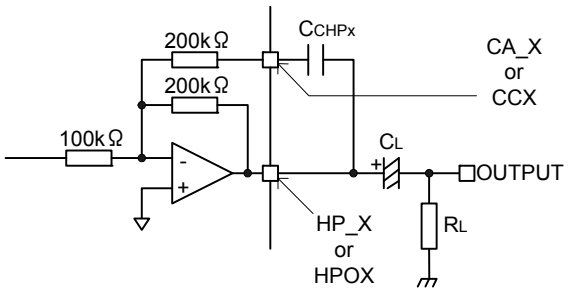


Fig.30 BU7858KN & BU7893GU Headphone Output Equivalent Circuit

Low-band cut-off frequency	$fC = 1/(2 \cdot \pi \cdot CL \cdot RL)$
Low-band boost frequency	$fBOOST = 1/(2 \cdot \pi \cdot CCHPx \cdot 200k\Omega)$
Boost gain	$ABOOST = 20 \cdot \log((200\ k\Omega + 1/(2 \cdot \pi \cdot f \cdot CCHPx))/100\ k\Omega)$ (the maximum low-band boost is 6dB)

For parameter setting, determine the output coupling capacitance CL and the headphone impedance R_L before calculating the low-band cut-off frequency fC. Then determine CCHPx so that the low-band cut-off frequency fC is roughly in agreement with the low-band boost frequency fBOOST.

The recommended parameter setting of BU7858KN and BU7893GU is CCHPx = 6800pF at the time of CL = 100μF and RL = 16Ω.

The frequency characteristic (theorical value) when the recommended constants are used is shown below.

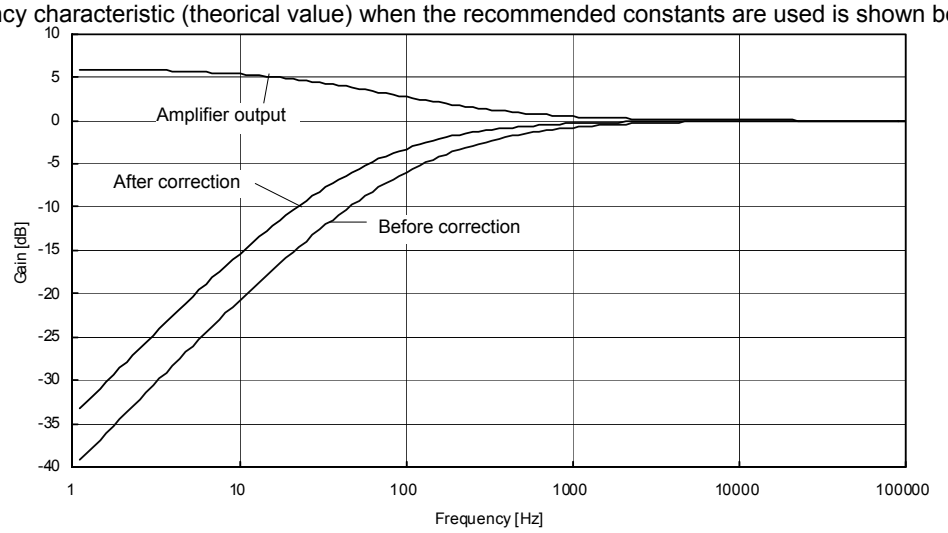


Fig.31 Low-band corrective circuit Frequency characteristic

●CPU Interface

BU7858KN and BU7893GU can be controlled by using CPU interface.

【BU7858KN】

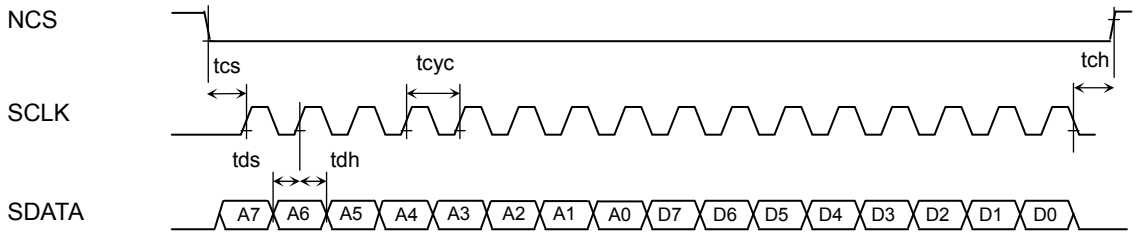


Fig.32 CPU I/F Timing Chart 1 (BU7858KN)

After the falling edge of NCS, SDATA inputs are settled by 16 clock of SCLK, and data is written in the rising edge of NCS.
The data format is “16bit right justified”.
CPU interface is that 1Byte=16bit. It is absolutely necessary to insert the interval of NCS=”H” between first Byte and Second Byte because it is not compatible with continuous data transmission. For the following th, please wait the time more than 1 SCLK Clock. (th≧tcyc)

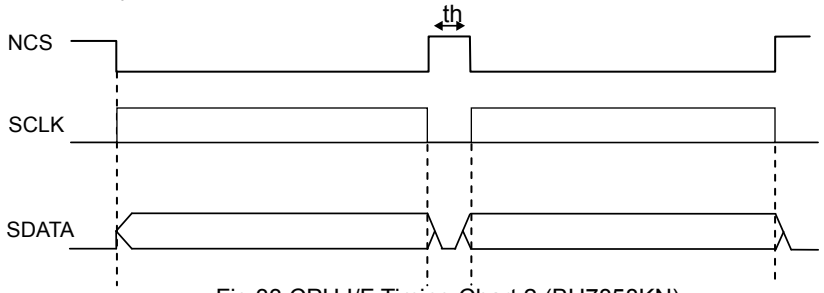


Fig.33 CPU I/F Timing Chart 2 (BU7858KN)

・AC Characteristics

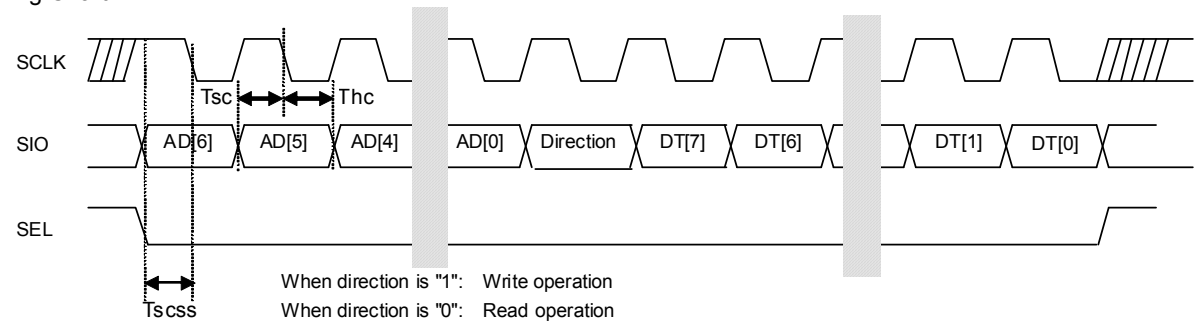
Ta=25℃, AVDD=DVDD=3.0V

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
SCLK Width	tcyc	250	-	-	ns	
SDATA Input Hold Time	tdh	50	-	-	ns	
SDATA Input Set-up Time	tds	50	-	-	ns	
NCS Set-up Time	tcs	50	-	-	ns	
NCS Hold Time	tch	50	-	-	ns	

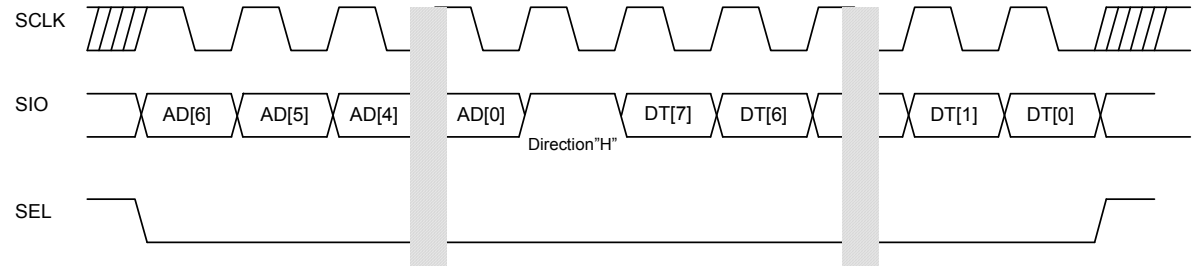
*It is recommended to use exclusive lines for CPU interface.

【BU7893GU】

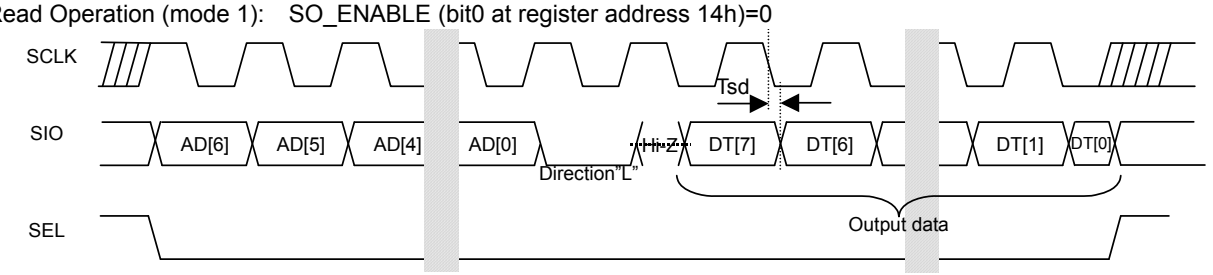
・Timing Chart



・Write Operation



・Read Operation (mode 1): SO_ENABLE (bit0 at register address 14h)=0



・Read Operation (mode 2): SO_ENABLE (bit0 at register address 14h)=1

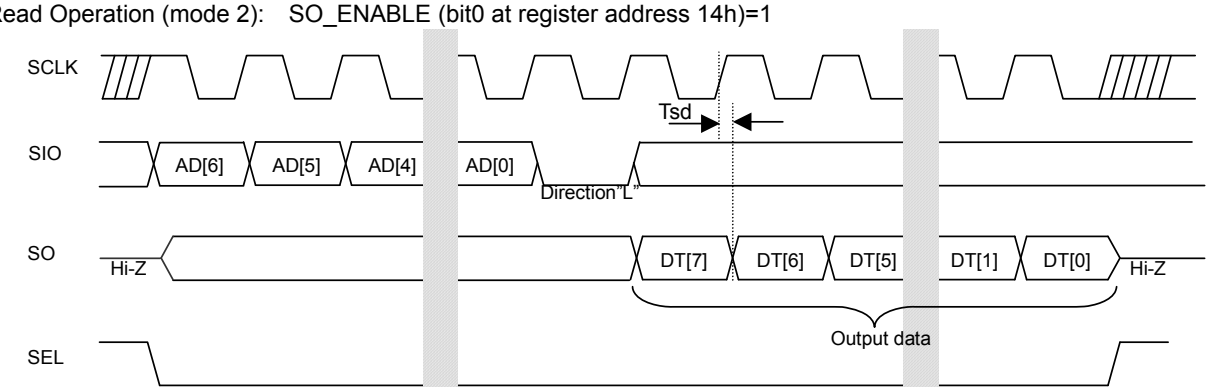


Fig.34 CPU I/F Timing Chart (BU7893GU)

DVDD_IO=1.62～3.3V, Ta=-30～+85℃

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Bit Length	Ncha	16	-	-	bit	MSB first
SCLK Input Frequency	FSCLK	-	-	15	MHz	
SCLK 'L' Pulse Width	Tlsclk	25	-	-	ns	
SCLK 'H' Pulse Width	Thsclk	25	-	-	ns	
SCLK-SEL Set-up Time	Tscss	10	-	-	ns	
Data Set-up Time	Tsc	10	-	-	ns	
Data Hold Time	Thc	10	-	-	ns	
Delay Time of Data Output	Tsd	-	-	30	ns	SIO: Time from SCLK falling edge SO : Time from SCLK rising edge

*It is recommended to use exclusive lines for CPU interface.

●I²C Interface

【BU7893GU】

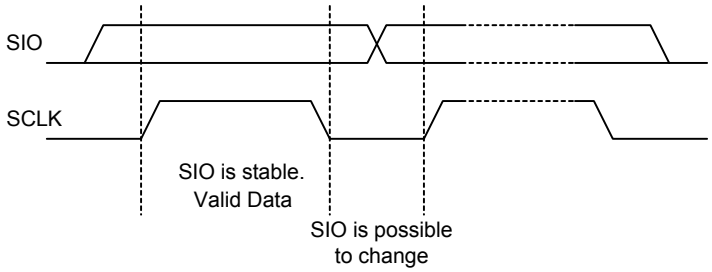
In the BU7893GU, the LSI can be controlled by using I²C interface.
The device's address (slave address) is "1100011(63h)". It is based on the Philips I²C-BUS V2.1's fast-mode, the maximum transfer rate of a bit is 400kbps.

A7	A6	A5	A4	A3	A2	A1	W/R
1	1	0	0	0	1	1	0/1

I²C Slave addresses

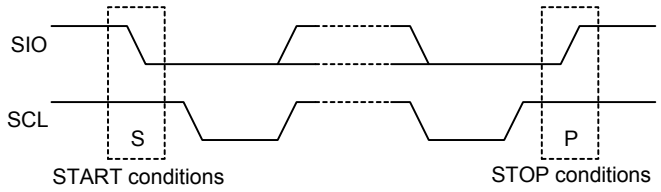
・Bit Transfer

A data is transferred during the HIGH period of the clock . The data on the SIO line must be stable during this period. The HIGH or LOW state of the data line can only change when the clock signal on the SCLK line is LOW. When SCL is H and SDA changes, the START conditions or the STOP condition is generated, and it is interpreted as the control signal.



・START & STOP Conditions

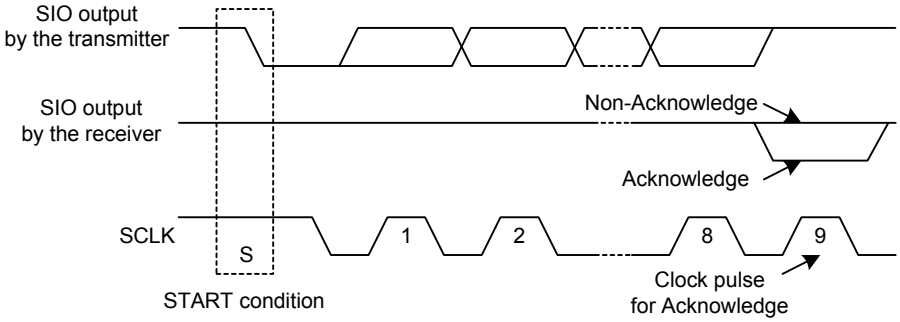
When SIO and SCLK are "H", there is no data transfer performed on the I²C bus. A HIGH to LOW transition on the SIO line while SCLK is HIGH is one such unique case. This situation indicates a START condition (S).
A LOW to HIGH transition on the SIO line while SCLK is HIGH defines a STOP condition (P).



The consecutive START and STOP conditions are acceptable.

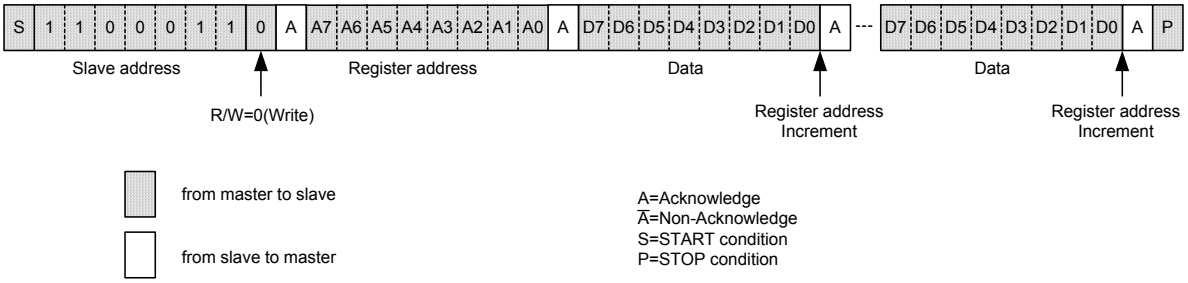
・Acknowledge

After START condition, 8 bits of data is transferred at a time. The transmitter releases the SIO line, and the receiver returns the Acknowledge signal by assuming SIO to be "L".



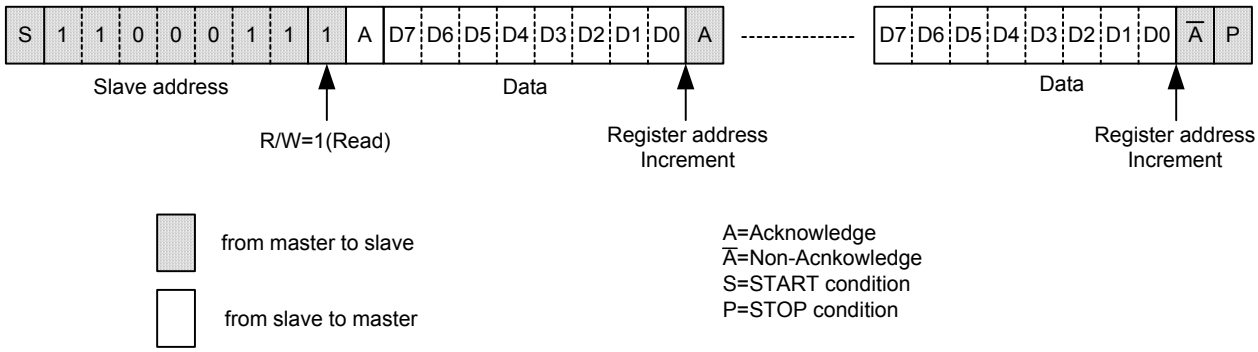
・Writing Protocol

The write protocol is shown below. The register address is transferred in a byte after the slave address and write command are transferred. The third byte writes the data into the internal register that is indicated by the second byte. After that, the register address is incremented on automatically (when the register address is between 00h and 16h). However, when the register address reaches 16h, the register address does not change with the next byte transfer, rather, it accesses the same register address (16h). The register address is incremented after transfer completion.



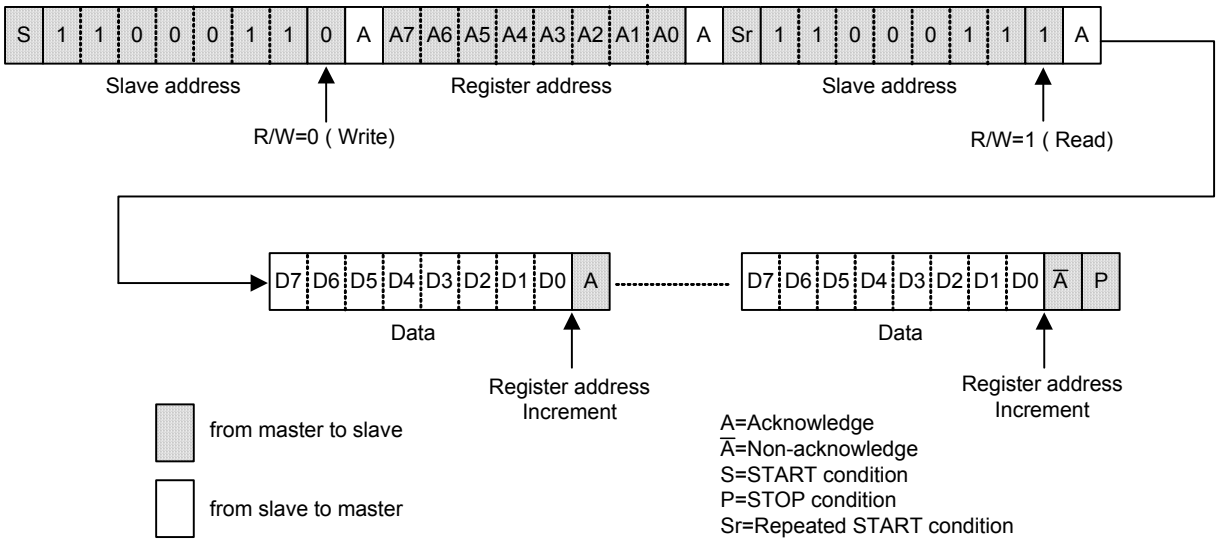
・Reading Protocol

It reads from the next byte after writing the slave address and R/W bit. The read register is the following address accessed at the end. After that, the data of the address incremented is read out. The register addresses are incremented after transfer completion.



・Combined Reading Protocol

After specifying an internal address, it reads by generating resending start conditions and changing the direction of data transfer. Afterwards, data from incremented addresses is read. The register addresses are incremented after transfer completion. Compound writing is possible by writing R/W=0 after resending start condition.



・Timing Diagram

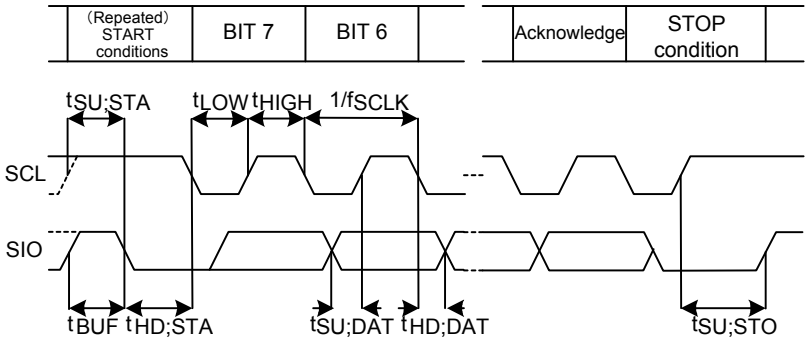


Fig.35 I^2C Timing Diagram

DVDD_IO=1.62～3.3V, Ta=-30～+85℃

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Hold Time at Start Condition	$t_{HD;STA}$	0.6	-	-	μsec	
SCLK “H” Level Time	t_{HIGH}	0.6	-	-	μsec	
SCLK “L” Level Time	t_{LOW}	1.3	-	-	μsec	
Set-up Time for Repeated Start Condition	$t_{SU;STA}$	0.6	-	-	μsec	
Data Hold Time	$t_{HD;DAT}$	0	-	0.9	μsec	
Data Set-up Time	$t_{SU;DAT}$	100	-	-	nsec	
Set-up Time for Stop Condition	$t_{SU;STO}$	0.6	-	-	μsec	
Bus Release Time between Stop Condition and Start Condition	t_{BUF}	1.3	-	-	μsec	

●Pin function

【BU7858KN】

No.	Pin Name	I/O	Pin Function	Power	Equivalent Circuit Diagram
1	SDTI	I	Audio DAC Serial Data Input	DVDD	A
2	LRCLK	I	Audio DAC LR Clock	DVDD	A
3	BCLK	I	Audio DAC BIT Clock	DVDD	A
4	DVDD	-	Digital Power Supply	-	-
5	DVSS	-	Digital Ground	DVDD	-
6	SCLK	I	Serial Clock for CPU Interface	DVDD	A
7	SDATA	I	Serial Data for CPU Interface	DVDD	A
8	NCS	I	Serial Chip Selection for CPU Interface	DVDD	A
9	NRST	I	Reset Input L: Reset	DVDD	A
10	CSTEP	-	Capacitor Connection Terminal for Pop Noise Reduction	AVDD	C
11	CSTART	-	Capacitor Connection Terminal for Pop Noise Reduction at Start-up	AVDD	G
12	CVCOM	-	Capacitor Connection Terminal for Internal Reference Voltage Output	AVDD	G
13	HP_R	O	Headphone Amplifier Output R-ch	AVDD	H
14	CA_R	-	Low-band Correction Capacitor for Headphone Amplifier R-ch	AVDD	C

No.	Pin Name	I/O	Pin Function	Power	Equivalent Circuit Diagram
15	CA_L	-	Low-band Correction Capacitor for Headphone Amplifier L-ch	AVDD	C
16	HP_L	O	Headphone Amplifier Output L-ch	AVDD	H
17	AVSS	-	Analog Ground	-	-
18	AVDD	-	Analog Power Supply	-	-
19	EXTO	O	600Ω Driver Output	AVDD	H
20	SPO	O	Line Output for Speaker	AVDD	H
21	EXTI	I	External Input	AVDD	D
22	MEL_L	I	Melody Input L ch	AVDD	D
23	MEL_R	I	Melody Input R ch	AVDD	D
24	RING	I	RING Input	AVDD	E
25	RXI	I	RXI Input	AVDD	D
26	PLLC	-	Capacitor Connection Terminal for PLL Loop Filter	DVDD	C
27	MCLKO	O	Master Clock Output	DVDD	B
28	MCLKI	I	Master Clock Input	DVDD	A

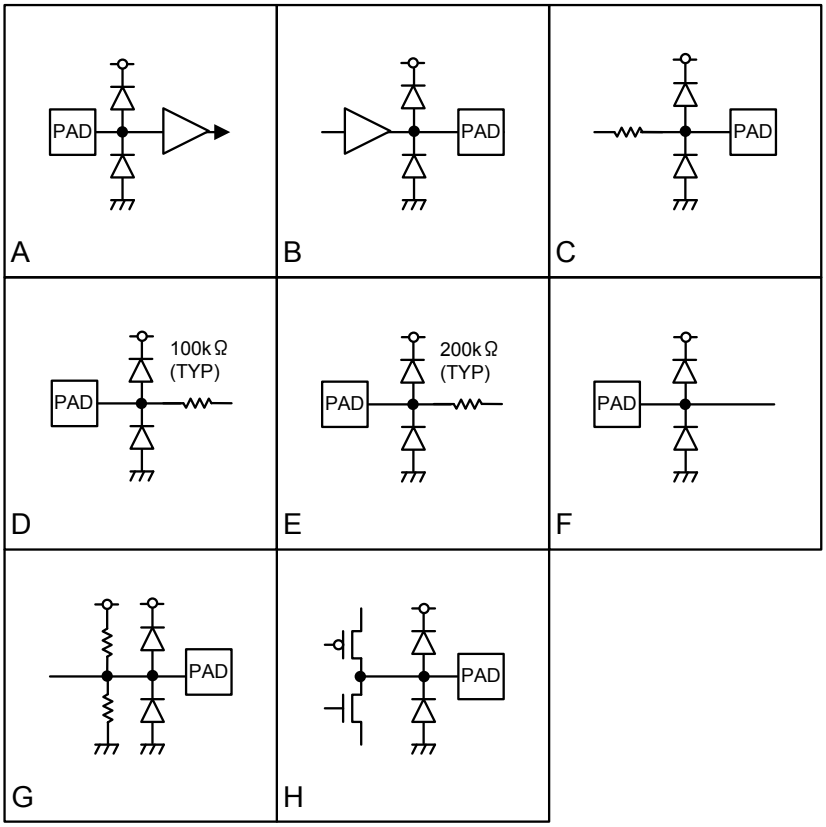


Fig.36 Equivalent Circuit Diagrams (BU7858KN)

【BU7893GU】

No.	Matrix No.	Pin Name	I/O	Pin Function	Terminal Conditions at Reset	Power	Equivalent Circuit Diagram
1	E3	AVDD	-	Analog Power Supply	-	AVDD	-
2	C6	AVSS	-	Analog Ground	-	AVDD	-
3	E6	ANAINL	I	DAC L-ch Input	-	AVDD	G
4	D6	ANAINR	I	DAC R-ch Input	-	AVDD	G
5	A3	HPOL	O	Headphone Amplifier Output L-ch	Pull-down	AVDD	H
6	A2	HPOR	O	Headphone Amplifier Output R-ch	Pull-down	AVDD	H
7	B4	CCL	I	Low-band Correction Capacitor for Headphone Amplifier L-ch	Pull-down	AVDD	I
8	B1	CCR	I	Low-band Correction Capacitor for Headphone Amplifier R-ch	Pull-down	AVDD	I
9	A5	SPOL	O	L-ch Line Output for Speaker	Pull-down	AVDD	H
10	B5	SPOR	O	R-ch Line Output for Speaker	Pull-down	AVDD	H
11	D5	COMOUT	O	Analog Reference Voltage Output	Hi-Z	AVDD	J
12	B6	COMIN	I	Analog Reference Voltage Input	Hi-Z	AVDD	K
13	A4	CPOP	I/O	Capacitor Connection Terminal for Pop Noise Reduction	Hi-Z	AVDD	L
14	C5	CSTEP	I/O	Capacitor Connection Terminal for Noise Reduction during Volume Change	Hi-Z	AVDD	L
15	E2	PLLC	I/O	Capacitor Connection Terminal for PLL Loop Filter	-	AVDD	L
16	E4	DVDD_CORE	-	Digital Core Power Supply	-	DVDD_CORE	-
17	F3	DVDD_IO	-	Digital IO Power Supply	-	DVDD_IO	-
18	B3	DVSS	-	Digital Ground	-	DVDD_IO, DVDD_CORE	-
19	F2	CLKI	I	PLL Reference Clock Input (19.2/19.68/19.8 MHz)	-	DVDD_IO	D
20	B2	RSTB	I	Reset Input L: Reset	-	DVDD_IO	A
21	E1	CSB	I	CPU Interface Select Pin (L :CPU I/F DVDD_IO : I^2C I/F)	-	DVDD_IO	B
22	C1	SCLK	I	CPU Interface Clock	-	DVDD_IO	A
23	D1	SIO	I/O	CPU Interface Data Input/Output (at Reset Input)	Hi-Z	DVDD_IO	F
24	C2	SO	I/O	CPU Interface Data Output (connected to DVSS when not in use)	Hi-Z	DVDD_IO	E
25	E5	SDI	I	Audio DAC Digital Data Input	Hi-Z	DVDD_IO	C
26	F4	BCLK	I/O	Audio DAC Bit Clock (Input State at Reset)	Hi-Z	DVDD_IO	E
27	F5	LRCLK	I/O	Audio DAC LR Clock (Input State at Reset)	Hi-Z	DVDD_IO	E
28	D2	MCLK	I/O	Audio DAC Master Clock (Input State at reset)	Hi-Z	DVDD_IO	E
29	F6	TEST1	I	Test Pin (connected to DVSS during normal operation)	Pull-down	DVDD_IO	C
30	F1	TEST2	I	Test Pin (connected to DVSS during normal operation)	Pull-down	DVDD_IO	C
31	A1	TEST3	I/O	Test Pin (released during normal operation)	-	DVDD_IO	E
32	A6	TEST4	I	Test Pin (released during normal operation)	-	AVDD	-

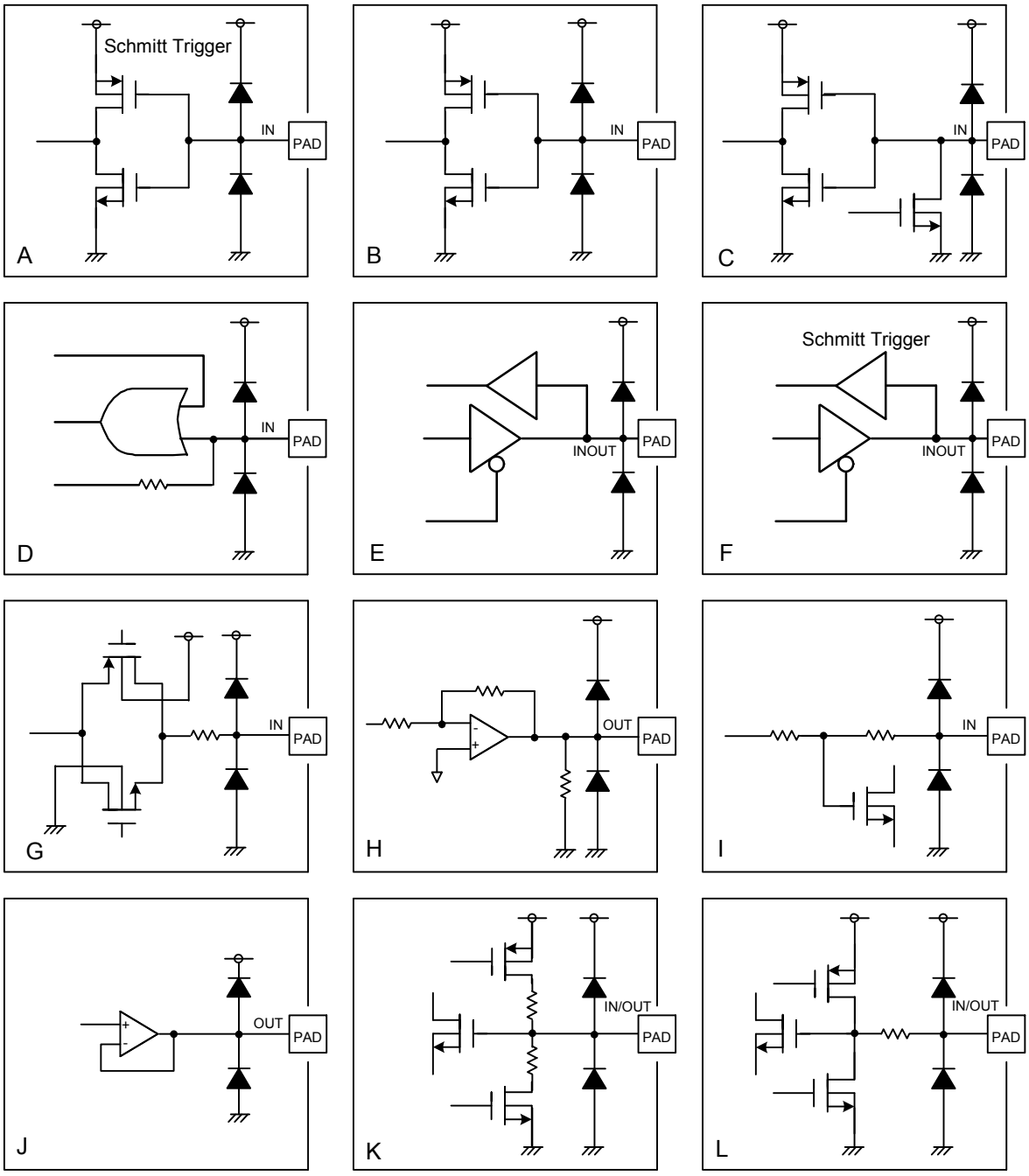
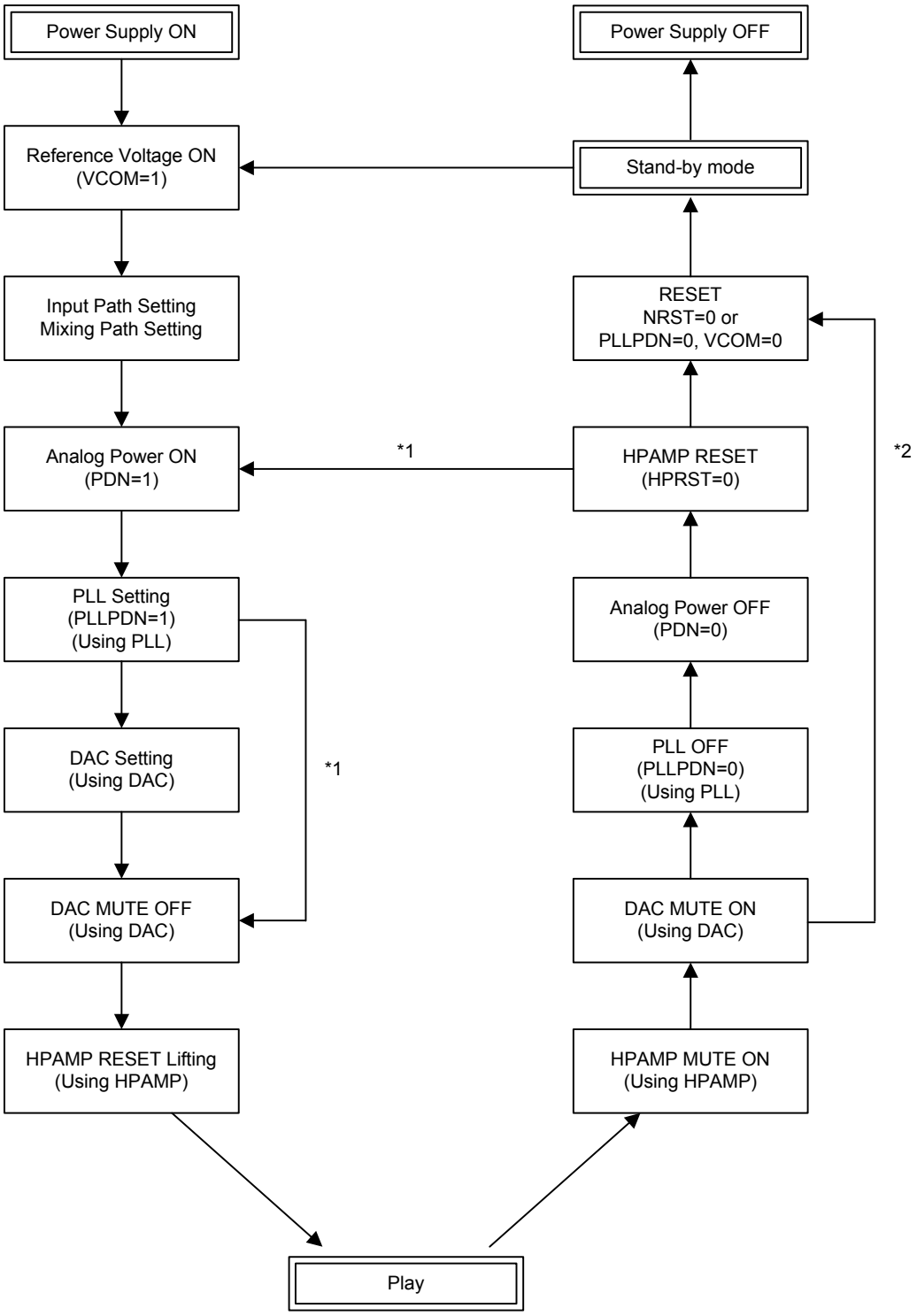


Fig.37 Equivalent Circuit Diagrams (BU7893GU)

●Recommended sequence

【BU7858KN】

Mode setting Flow



*1 : When the analog path setting is not changed (Repeated play)
*2 : When the power supply OFF, after playing

Fig.38 BU7858KN Recommended Sequence Flow Chart

【BU7893GU】
SAMPLE# AUDIO PATH+ AUDIO DAC BLOCK SETTING SEQUENCE

After powering up and canceling reset, set paths according to the sequence shown as below:

(1) Start up reference voltage
Start up the reference voltage in the REF_PWR register (00h).
To start up the VREF block fast, set the REF_ON bit (bit-0) and BST_ON bit (bit-1) to "1" simultaneously. After starting up the reference voltage startup, set just the BST_ON bit (bit-1) to "0".

(2) Start up Audio DAC
When using Audio DAC
(2-1) Enable PLL block clock input and start up PLL
Start up the power supply of the PLL and enable clock input to the PLL in the PLL_PWR register (16h).
Set REF1_ON (bit-1) and PLL_ON (bit-0) to "1" simultaneously.
(2-2) Caution concerning interim between starting up PLL block and starting up Audio DAC block
After starting up the power supply of the PLL in the PLL_PWR register (16h), wait 10 msec before starting up the Audio DAC.
(2-3) Start up Audio DAC block
Start up the power supply of the Audio DAC in the DAC SET4 register (13h).
Set DAC_ON (bit-5) and DAC_RSTB (Bit-4) to "1".
(2-4) Set 3D surround and Equalyzer parameter
Please tell us about the parameter setting when you use this function.

(3) Start up analog input amplifier to use
Start up the power supply of the input amplifier and input volume in the IAMP_PWR register (01h).

(4) Set input volume
Set the input volume in the IVR_1 register (09h).

(5) Set mixing path
Make mixing path settings in the MIX1 register (02h), MIX2 register (03h), MIX3 register (04h), and MIX4 register (05h).

(6) Set startup noise reduction sequence
Set the sequence time in the POP_TM register (07h).

(7) Set click noise reduction sequence
Set the sequence time in the OVR_TM register (0Ah).

(8) Set output path
Enable the relevant output path in the PATH_CNT register (06h).

(9) Set output volume
Set output volume values =0x18(-48dB) in the OVR_1 register (0Bh).

(10) Ramp up output driver amplifier
Ramp up the output driver amplifier in the DRV_PWR register (08h).

(11) Caution concerning interim between ramping up output driver amplifier and canceling mute
After setting the DRV_PWR register (08h), wait the sequence time set in the POP_TM register (07h) before canceling mute.

(12) Cancel mute
Cancel mute state of the output driver amplifier in the DRV_MT register (0Ch).

(13) Caution concerning interim between canceling mute and setting output volume
After setting the DRV_MT register (0Ch), wait the sequence time that is set in the OVR_TM register (0Ah) before subsequently setting output volume.

(14) Set output volume
Set output volume values in the OVR_1 register (0Bh).

Path Modification Sequence

(1) Set output mute
Put the output driver amplifier in a mute state by setting the DRV_MT register (0Ch).

(2) Caution concerning interim between setting mute and ramping down output driver amplifier
After setting the DRV_MT register (0Ch), wait the sequence time that is set in the OVR_TM register (0Ah) before subsequently ramping down the output driver amplifier.

(3) Ramp down output driver amplifier
Ramp down the output driver amplifier by setting the DRV_PWR register (08h).

(4) Set AUDIO DAC (Refer to P.20)

(5) Modify input path, mixing path, output path (Refer to P.20)

(6) Ramp up output driver amplifier
Ramp up output driver amplifier in the DRV_PWR register (08h)
After ramping down output driver at (3), wait the sequence time that is set in the POP_TM register (07h) before subsequently ramping up.

(7) Caution concerning interim between ramping up output driver amplifier and canceling mute
After setting the DRV_PWR register (08h) at (6), wait the sequence time that is set in the POP_TM register (07h) before subsequently canceling mute.

(8) Cancel mute
Cancel output mute in the DRV_MT register (0Ch).

Power-Down Sequence

(1) Set output volume
Set output volume values =0x18(-48dB) in the OVR_1 register (0Bh).

(2) Caution concerning interim between setting output volume and setting mute
After setting the OVR_1 register (0Bh), wait the sequence time that is set in the DRV_MT register (0Ch) before subsequently setting mute.

(3) Put the output driver amplifier in a mute state by using the DRV_MT register (0Ch).

(4) Caution concerning interim between setting mute and ramping down output driver amplifier
After setting the DRV_MT register (0Ch), wait the sequence time that is set in the OVR_TM register (0Ah) before subsequently ramping down the output driver amplifier.

(5) Ramp down output driver amplifier
Ramp down the output driver amplifier in the DRV_PWR register (08h).

(6) Power down AUDIO DAC
When using AUDIO DAC
(6-1) Power down AUDIO DAC block
Power down the AUDIO DAC according to the DAC SET4 register (13h).
Set DAC_ON (bit-5) and DAC_RSTB (Bit-4) to "0".
(6-2) Mask clock input and power down PLL block
Power down the PLL and mask clock input to the PLL according to the PLL_PWR register (16h).
Set REF_ON (bit-1) and PLL_ON (bit-0) to "0" simultaneously.

(7) Input reset
Put a reset state by using RSTB pin input.

(8) Power down

●Notes for use

1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state.
Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

6) Short circuit between terminals and erroneous mounting
In order mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs, Erroneous mounting can break down the ICs. Furthermore, if a shout circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

7) Operation in a strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals, a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the normal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

12) No Connecting input terminals
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

●Ordering part number

B	U	7	8	5	8	K	N	-	E	2

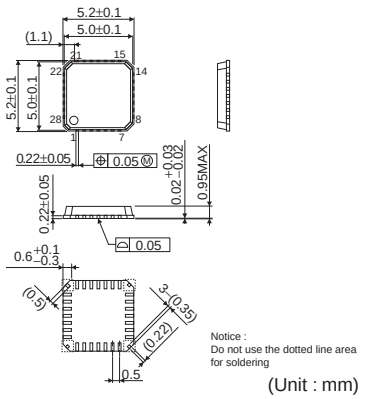
Part No.

Part No.
7858
7893

Package
KN: VQFN28
GU: VCSP85H3

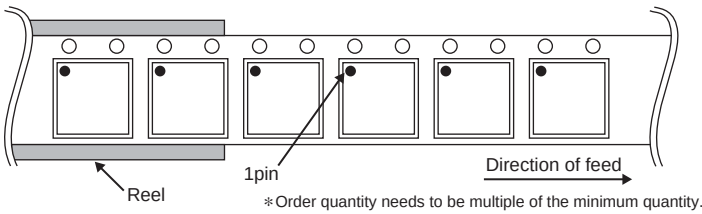
Packaging and forming specification
E2: Embossed tape and reel

VQFN28



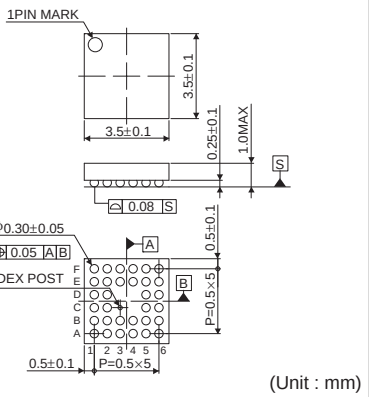
<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



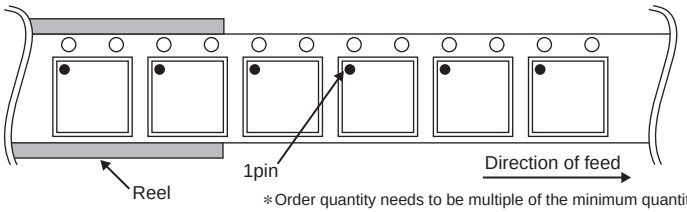
∗Order quantity needs to be multiple of the minimum quantity.

VCSP85H3(BU7893GU)



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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