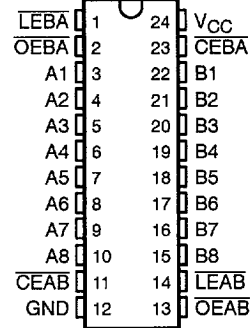


SN74LVC543 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC543 contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

The SN74LVC543 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT B
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	$B_0^\ddagger$
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

‡ Output level before the indicated steady-state input conditions were established.

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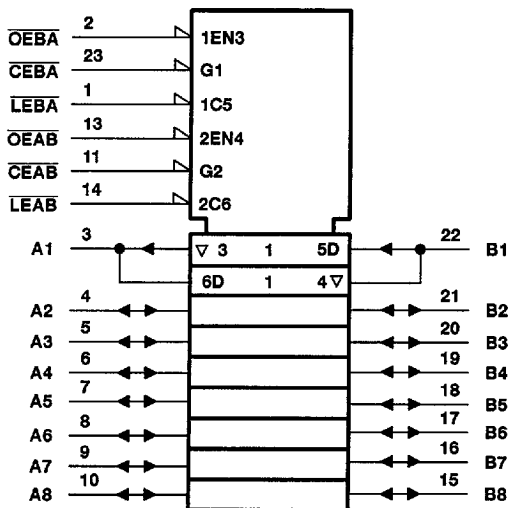
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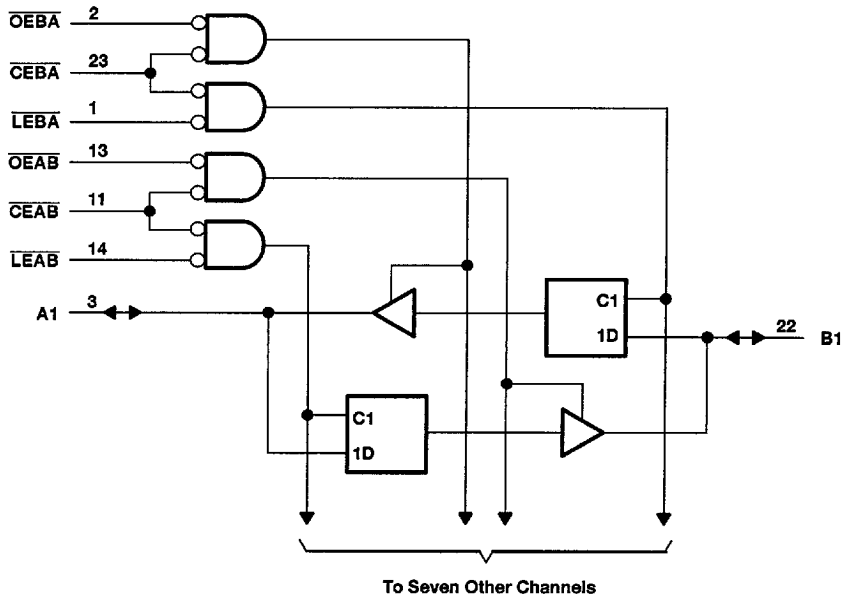
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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**TEXAS
INSTRUMENTS**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports)	–0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.65 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		−12	mA
		V _{CC} = 3 V		−24	
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T _A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

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OCTAL REGISTERED TRANSCEIVER

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} [†]	T _A = –40°C to 85°C			UNIT
				MIN	TYP	MAX	
V _{OH}		I _{OH} = –100 μA	MIN to MAX	V _{CC} – 0.2			V
		I _{OH} = –12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = –24 mA	3 V	2			
V _{OL}		I _{OL} = 100 μA	MIN to MAX	0.2			V
		I _{OL} = 12 mA	2.7 V	0.4			
		I _{OL} = 24 mA	3 V	0.55			
I _I		V _I = V _{CC} or GND	3.6 V	±5			μA
I _{OZ} [‡]		V _O = V _{CC} or GND	3.6 V	±10			μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V	20			μA
ΔI _{CC}		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		500			μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	3			pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	4.3			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t _w	Pulse duration		4		4		ns
t _{su}	Setup time	Data before LE↑ or OE↑	1.5		1.5		ns
t _h	Hold time	Data after LE↑ or OE↑	2.5		2.5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	TYP [§]	MAX	MIN	MAX	
t _{pd}	A or B	B or A	1.5	4	8	9		ns
	LE		1.5	4.4	9.5	10.5		
t _{en}	OE	A or B	1.5	3.9	8.5	9.5		ns
	CE		1.5	4.1	9	10		
t _{dis}	OE	A or B	1.5	4.7	8.5	9.5		ns
	CE		1.5	4.8	9	10		

[§] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

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operating characteristics, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	20	pF
	Outputs disabled		10	

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