SIEMENS

Microcomputer Components

8-Bit CMOS Single-Chip Microcontroller

SAB 80C517A/83C517A-5

Data Sheet 05.94

SIEMENS

High-Performance SAB 80C517A/83C517A-5
8-Bit CMOS Single-Chip Microcontroller

Preliminary

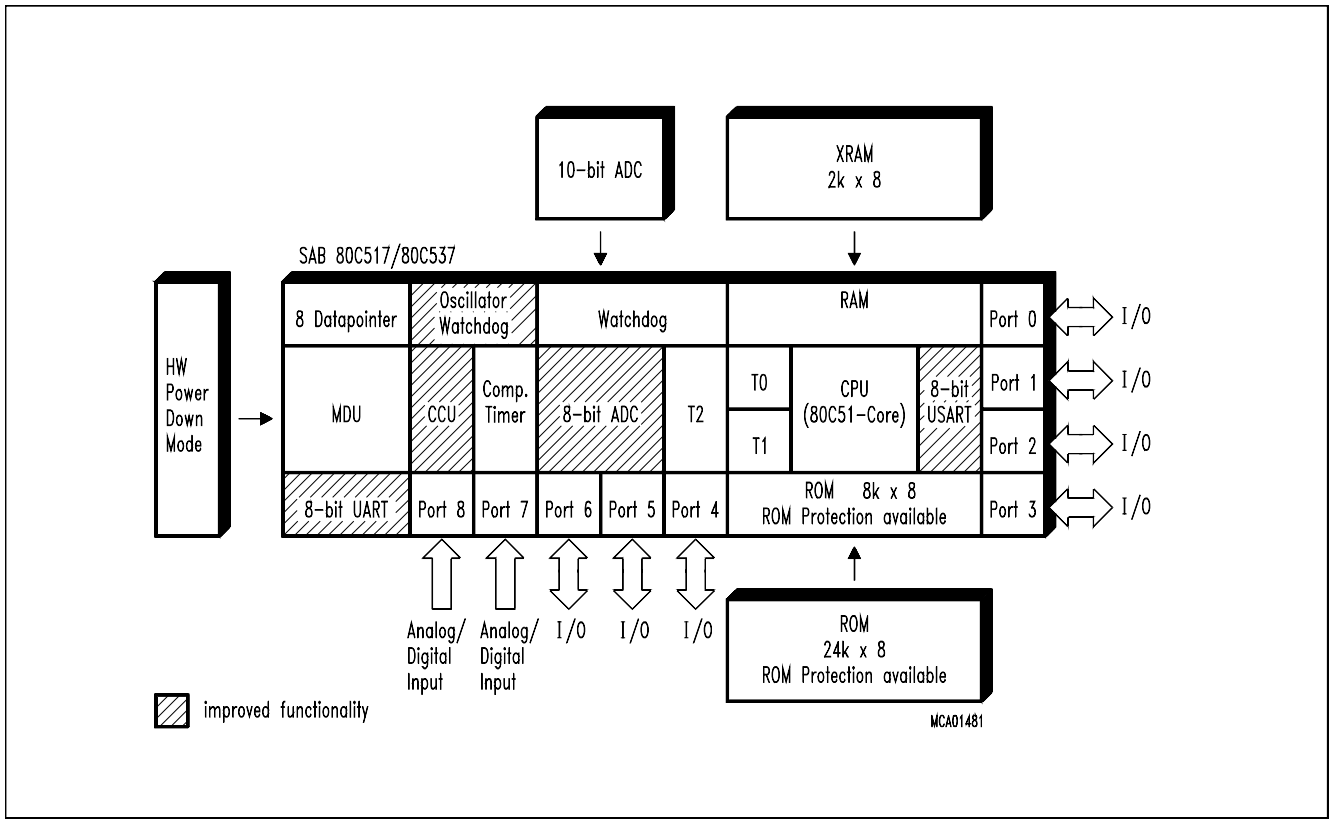
SAB 83C517A-5	Microcontroller with factory mask-programmable ROM
SAB 80C517A	Microcontroller for external ROM

- SAB 80C517A/83C517A-5, up to 18 MHz operation
- 32 K × 8 ROM (SAB 83C517A-5 only, ROM-Protection available)
- 256 × 8 on-chip RAM
- 2 K × 8 on-chip RAM (XRAM)
- Superset of SAB 80C51 architecture:
  - 1 µs instruction cycle time at 12 MHz
  - 666 ns instruction cycle time at 18 MHz
  - 256 directly addressable bits
  - Boolean processor
  - 64 Kbyte external data and program memory addressing
- Four 16-bit timer/counters
- Powerful 16-bit compare/capture unit (CCU) with up to 21 high-speed or PWM output channels and 5 capture inputs
- Versatile "fail-safe" provisions
- Fast 32-bit division, 16-bit multiplication, 32-bit normalize and shift by peripheral MUL/DIV unit (MDU)
- Eight data pointers for external memory addressing
- Seventeen interrupt vectors, four priority levels selectable
- Genuine 10-bit A/D converter with 12 multiplexed inputs
- Two full duplex serial interfaces with programmable Baudrate-Generators
- Fully upward compatible with SAB 80C515, SAB 80C517, SAB 80C515A
- Extended power saving mode
- Fast Power-On Reset
- Nine ports: 56 I/O lines, 12 input lines
- Three temperature ranges available:
  0 to 70 °C (T1)
  – 40 to 85°C (T3)
  – 40 to 110°C (T4)
- Plastic packages: P-LCC-84, P-MQFP-100-2

The SAB 80C517A/83C517A-5 is a high-end member of the Siemens SAB 8051 family of microcontrollers. It is designed in Siemens ACMOS technology and based on SAB 8051 architecture. ACMOS is a technology which combines high-speed and density characteristics with low-power consumption or dissipation.

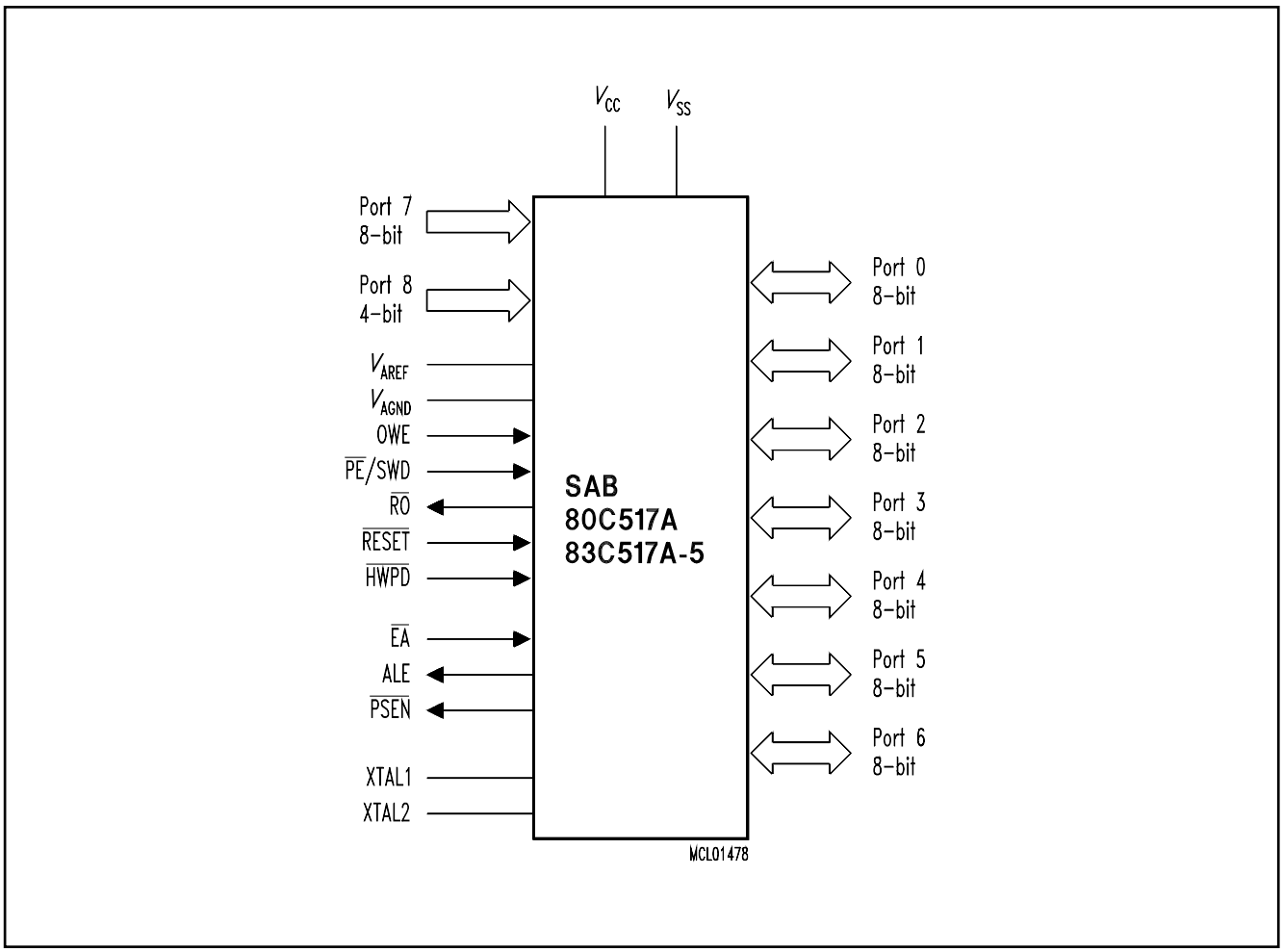
While maintaining all the SAB 80C517 features and operating characteristics the SAB 80C517A is expanded in its "fail-safe" characteristics and timer capabilities.The SAB 80C517A is identical with the SAB 83C517A-5 except that it lacks the on-chip program memory. The SAB 80C517A/83C517A-5 is supplied in a 84-pin plastic leaded chip carrier package (P-LCC-84) and in a 100-pin plastic quad flat package (P-MQFP-100-2).

SAB 80C517A/83C517A-5 Revision History	**05.94**
Previous Releases	01.94/08.93/11.92/10.91/04.91
Page	Subjects (changes since last revision 04.91)
6 4 7-15 several 3 26, 27, 31 34 41 49 60 62 65 several 66 66	– Pin configuration P-MQFP-100-2 added – Pin differences updated – Pin numbers for P-MQFP-100-2 package added – Correction of P-MRFP-100 into P-MQFP-100-2 – Ordering information for -40 to +110°C versions – Correction of register names S0RELL, SCON, ADCON, ICRON, and SBUF – Figure 4 corrected – Figure 8 corrected – $\overline{PE}$/SWD function description completed – Correct ordering numbers – Test condition for V_{OH}, V_{OH1} corrected – t_{PXIZ} name corrected t_{AVIV}, t_{AZPL} values corrected – Minimum clock frequence is now 3.5 MHz – t_{QVWH} (data setup before $\overline{WR}$) corrected and added – t_{LLAX2} corrected
Page	Subjects (changes since last revision 08.93)
26 51 65 65 74	– Corrected SFR name S0RELL – Below "Termination of HWPD Mode": 4th paragraph with ident corrected – Description of t_{LLIV} corrected – Program Memory Read Cycle: t_{PXAV} added – Oscillator circuit drawings: MQFP-100-2 pin numbers added.
Page	Subjects (changes since last revision 01.94)
 47	– Minor changes on several pages – Table 6 corrected



Ordering Information

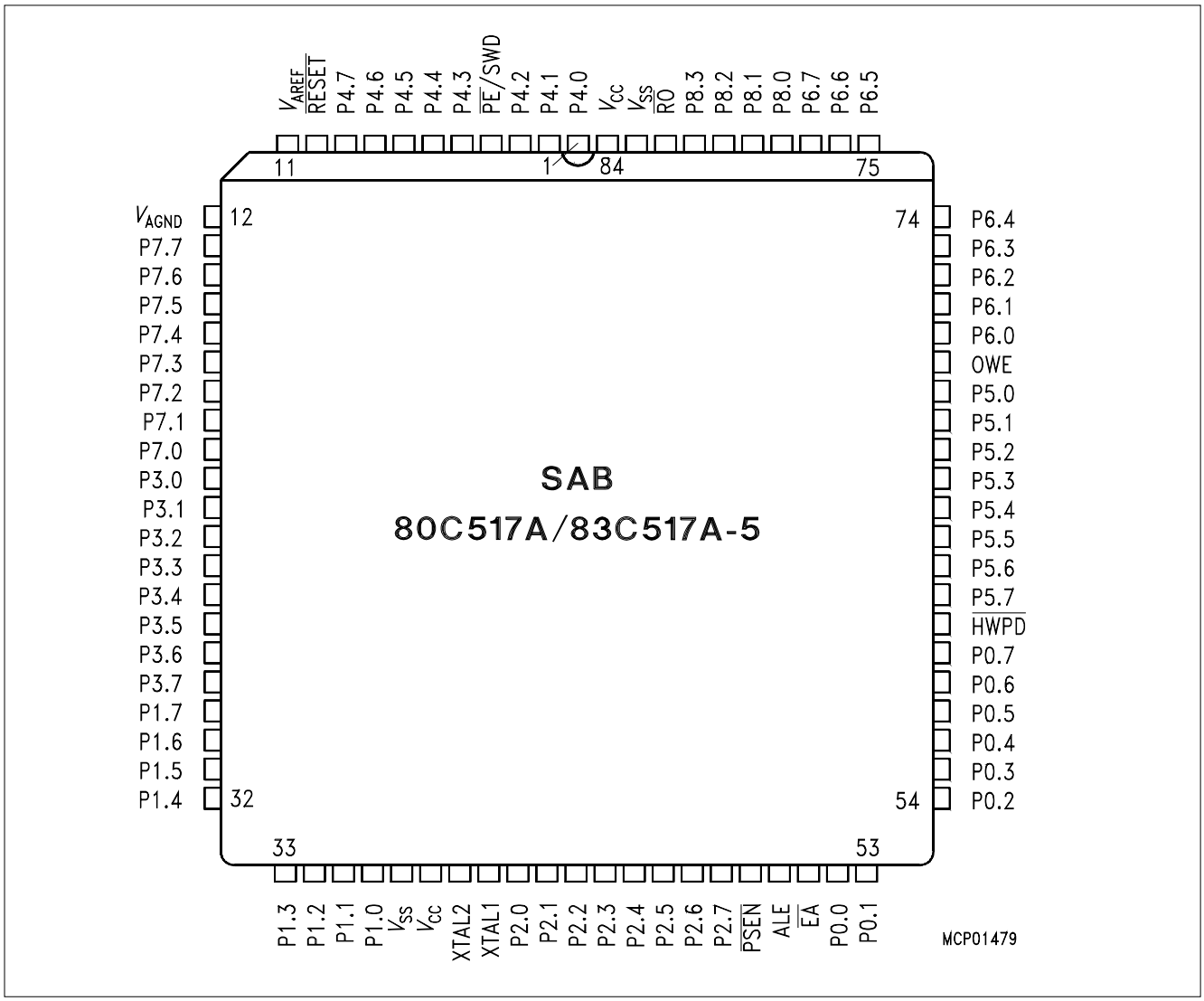
Type	Ordering Code	Package	Description 8-bit CMOS Microcontroller
SAB 80C517A-N18	Q67120-C583	P-LCC-84	for external memory,18 MHz
SAB 80C517A-M18	TBD	P-MQFP-100-2	
SAB 83C517A-5N18	Q67120-C582	P-LCC-84	with mask-programmable ROM, 18 MHz
SAB 80C517A-N18-T3	Q67120-C769	P-LCC-84	for external memory,18 MHz ext. temperature – 40 to 85 °C
SAB 83C517A-5N18-T3	Q67120-C771	P-LCC-84	with mask-programmable ROM, 18 MHz ext. temperature – 40 to 85 °C
SAB 83C517A-N18-T4	TBD	P-LCC-84	for external memory, 18 MHz ext. temperature -40 to +110°C
SAB 83C517A-5N18-T4	TBD	P-LCC-84	with mask-programmable ROM, 18 MHz ext. temperature -40 to +110°C



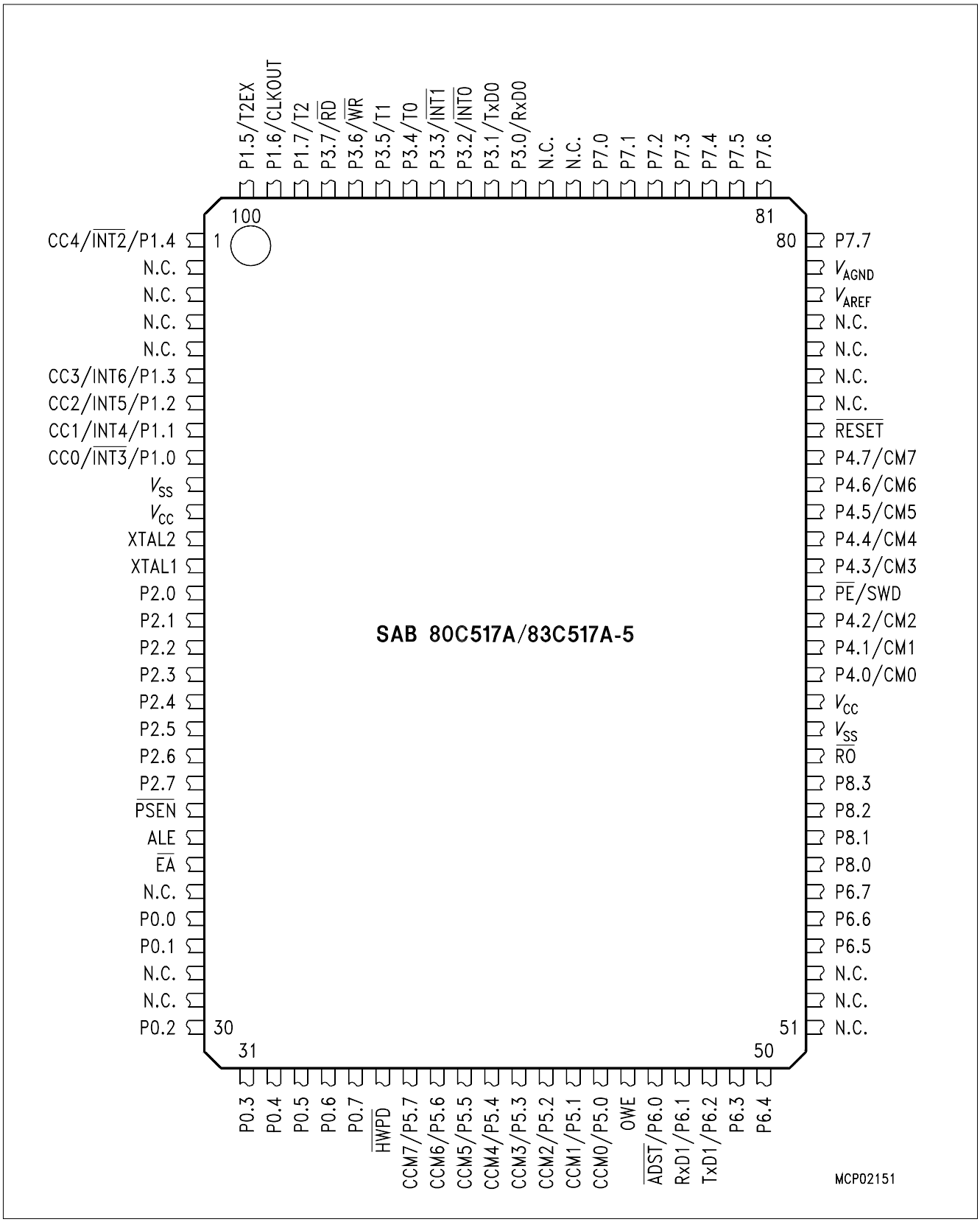
Logic Symbol

The pin functions of the SAB 80C517A are identical with those of the SAB 80C517/80C537 with one exception:

Typ	SAB 80C517A	SAB 80C517/80C537
P-LCC-84, Pin 60	$\overline{\text{HWPD}}$	N.C.
P-MQFP-100-2, Pin 36		



Pin Configuration
(P-LCC-84)



Pin Configuration
(P-MQFP-100-2)

Pin Definitions and Functions

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P4.0 – P4.7	1– 3, 5 – 9	64 - 66, 68 - 72	I/O	**Port 4** is a bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current ($I_{IL,}$ in the DC characteristics) because of the internal pull-up resistors. This port also serves alternate compare functions. The secondary functions are assigned to the pins of port 4 as follows: – CM0 (P4.0): Compare Channel 0 – CM1 (P4.1): Compare Channel 1 – CM2 (P4.2): Compare Channel 2 – CM3 (P4.3): Compare Channel 3 – CM4 (P4.4): Compare Channel 4 – CM5 (P4.5): Compare Channel 5 – CM6 (P4.6): Compare Channel 6 – CM7 (P4.7): Compare Channel 7
$\overline{PE}$/SWD	4	67	I	**Power saving modes $\overline{enable}$ Start Watchdog Timer** A low level on this pin allows the software to enter the power down, idle and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default. Use of the software controlled power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{\text{RESET}}$	10	73	I	$\overline{\text{RESET}}$ A low level on this pin for the duration of one machine cycle while the oscillator is running resets the SAB 80C517A. A small internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11	78		**Reference voltage** for the A/D converter.
V_{AGND}	12	79		**Reference ground** for the A/D converter.
P7.7 -P7.0	13 - 20	80 - 87	I	**Port 7** is an 8-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the lower 8-bit of the multiplexed analog inputs of the A/D converter, simultaneously.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P3.0 - P3.7	21 - 28	90 - 97	I/O	**Port 3** is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current ($I_{IL,}$ in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – R × D0 (P3.0): receiver data input (asynchronous) or data input/output (synchronous) of serial interface – T × D0 (P3.1): transmitter data output (asynchronous) or clock output (synchronous) of serial interface 0 – $\overline{INT0}$ (P3.2): $\overline{interrupt\ 0\ input}$/timer 0 gate control – $\overline{INT1}$ (P3.3): $\overline{interrupt\ 1\ input}$/timer 1 gate control – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{WR}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{RD}$ (P3.7): the read control signal enables the external data memory to port 0

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P1.7 - P1.0	29 - 36	98 - 100, 1, 6 - 9	I/O	**Port 1** is a bidirectional I/O port with internal pull-up resistors. Port 1 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. It is used for the low order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): $\overline{\text{interrupt 3 input}}$/ compare 0 output /capture 0 input – INT4/CC1 (P1.1): interrupt 4 input / compare 1 output /capture 1 input – INT5/CC2 (P1.2): interrupt 5 input / compare 2 output /capture 2 input – INT6/CC3 (P1.3): interrupt 6 input / compare 3 output /capture 3 input – $\overline{\text{INT2}}$/CC4 (P1.4): $\overline{\text{interrupt 2 input}}$ / compare 4 output /capture 4 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
XTAL2	39	12	–	**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL1	40	13	–	**XTAL1** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is devided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.
P2.0 - P2.7	41 - 48	14 - 21	I/O	**Port 2** is a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as in-puts. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing1 s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{\text{PSEN}}$	49	22	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal program execution.
ALE	50	23	O	The **Address Latch Enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periodes except during an external data memory access
$\overline{\text{EA}}$	51	24	I	**External Access Enable** When held at high level, instructions are fetched from the internal ROM (SAB 83C517A-5 only) when the PC is less than 8000H. When held at low level, the SAB 80C517A fetches all instructions from external program memory. For the SAB 80C517A this pin must be tied low
P0.0 - P0.7	52 - 59	26 - 27, 30 - 35	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1 s written to them float, and in that state can be used as high-impe-dance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1 s. Port 0 also out-puts the code bytes during program verification in the SAB 83C517A if ROM-Protection was not enabled. External pull-up resistors are required during program verification.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{\text{HWPD}}$	60	36	I	**$\overline{\text{Hardware Power Down}}$** A low level on this pin for the duration of one machine cycle while the oscillator is running resets the SAB 80C517A. A low level for a longer period will force the part to Power Down Mode with the pins floating. (see table 7)
P5.7 - P5.0	61 - 68	37 - 44	I/O	**Port 5** is a bidirectional I/O port with internal pull-up resistors. Port 5 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. This port also serves the alternate function "Concurrent Compare" and "Set/Reset Compare". The secondary functions are assigned to the port 5 pins as follows: – CCM0 to CCM7 (P5.0 to P5.7): concurrent compare or Set/Reset
			I	
OWE	69	45	I/O	**Oscillator Watchdog Enable** A high level on this pin enables the oscillator watchdog. When left unconnected this pin is pulled high by a weak internal pull-up resistor. When held at low level the oscillator watchdog function is off.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P6.0 - P6.7	70 - 77	46 - 50, 54 - 56	I/O	**Port 6** is a bidirectional I/O port with internal pull-up resistors. Port 6 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 6 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 6 also contains the external A/D converter control pin and the transmit and receive pins for serial channel 1. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 6, as follows: – $\overline{ADST}$ (P6.0): external A/D converter start pin – R × D1 (P6.1): receiver data input of serial interface 1 – T × D1 (P6.2): transmitter data output of serial interface 1
P8.0 - P8.3	78 - 81	57 - 60	I	**Port 8** is a 4-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the higher 4-bit of the multiplexed analog inputs of the A/D converter, simultaneously

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{RO}$	82	61	O	**$\overline{\text{Reset Output}}$** This pin outputs the internally synchronized reset request signal. This signal may be generated by an external hardware reset, a watchdog timer reset or an oscillator watch-dog reset. The reset output is active low.
V_{SS}	37, 83	10, 62	–	**Circuit ground potential**
V_{CC}	38, 84	11, 63	–	**Supply Terminal** for all operating modes
N.C.	–	2 - 5, 25, 28 - 29, 51 - 53, 74 - 77, 88 - 89	–	Not connected

* I = Input
O = Output

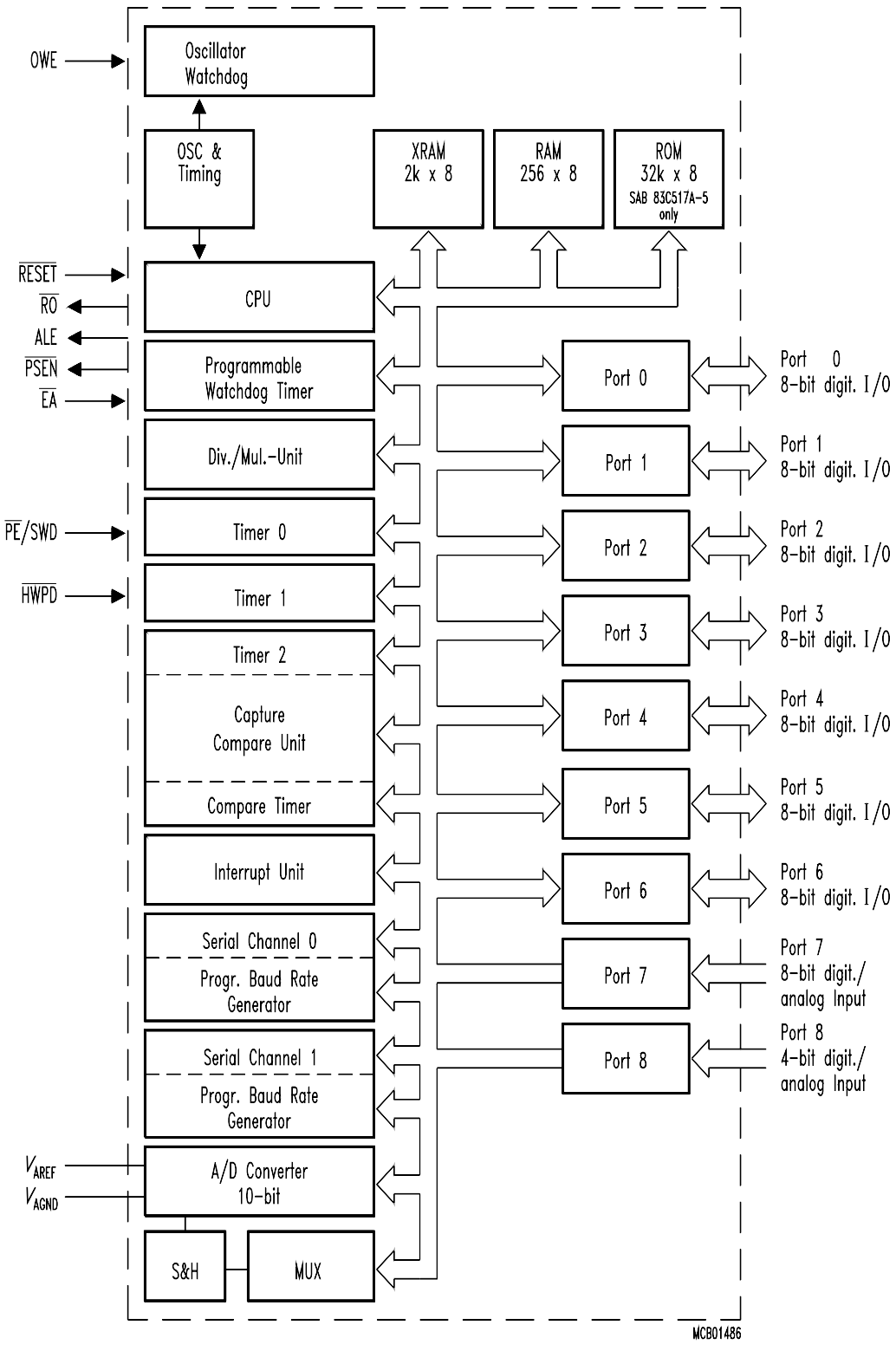


Figure 1
Block Diagram

Functional Description

The SAB 80C517A is based on 8051 architecture. It is a fully compatible member of the Siemens SAB 8051/80C51 microcontroller family being an significantly enhanced SAB 80C517. The SAB 80C517A is therefore compatible with code written for the SAB 80C517.

Having an 8-bit CPU with extensive facilities for bit-handling and binary BCD arithmetics the SAB 80C517A is optimized for control applications. With a 18 MHz crystal, 58 % of the instructions are executed in 666.67 ns.

Being designed to close the performance gap to the 16-bit microcontroller world, the SAB 80C517A's CPU is supported by a powerful 32-/16-bit arithmetic unit and a more flexible addressing of external memory by eight 16-bit datapointers.

Memory Organisation

According to the SAB 8051 architecture, the SAB 80C517A has separate address spaces for program and data memory. Figure 2 illustrates the mapping of address spaces.

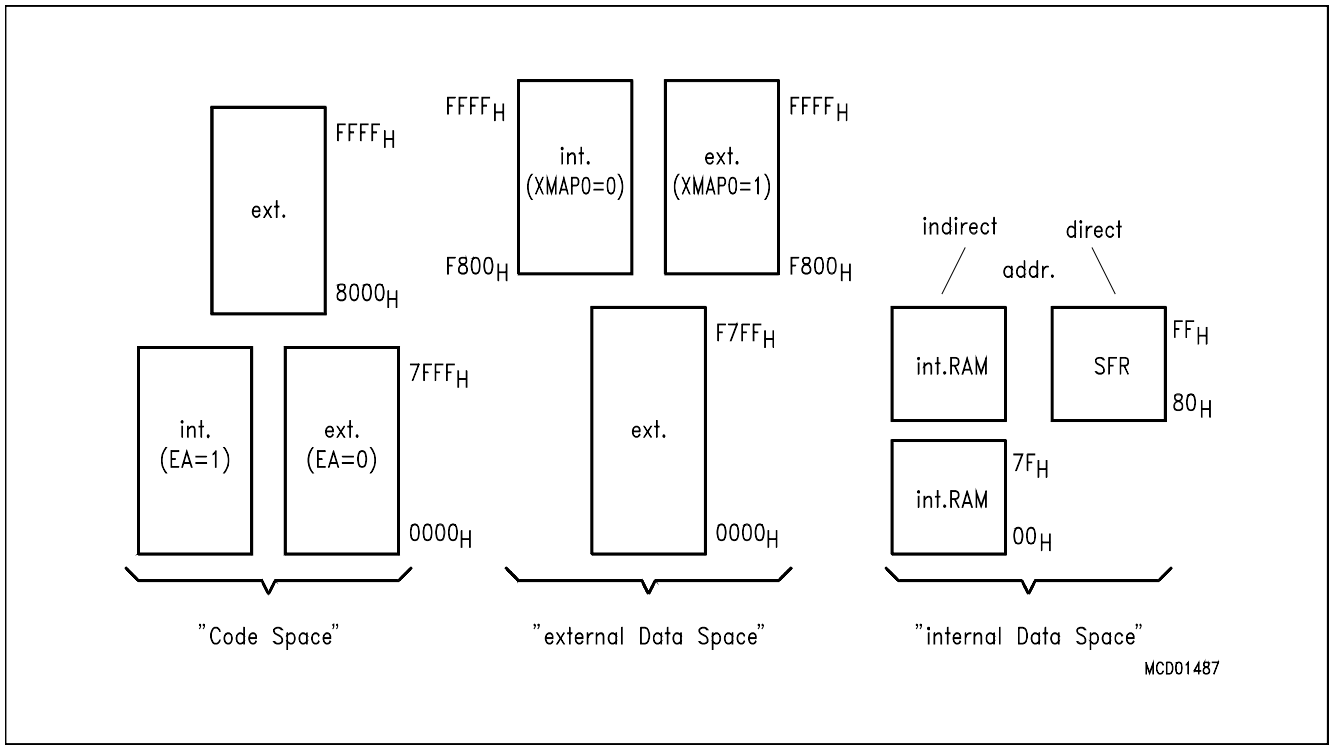


Figure 2
Memory Map

Program Memory ('Code Space')

The SAB 83C517A-5 has 32 Kbyte of on-chip ROM, while the SAB 80C517A has no internal ROM. The program memory can externally be expanded up to 64 Kbyte. Pin $\overline{EA}$ controls whether program fetches below address 8000H are done from internal or external memory.

As a new feature the SAB 83C517A-5 offers the possibility of protecting the internal ROM against unauthorized access. This protection is implemented in the ROM-Mask.Therefore, the decision ROM-Protection 'yes' or 'no' has to be made when delivering the ROM-Code. Once enabled, there is no way of disabling the ROM-Protection.

Effect: The access to internal ROM done by an externally fetched MOVC instruction is disabled. Nevertheless, an access from internal ROM to external ROM is possible.

To verify the read protected ROM-Code a special ROM-Verify-Mode is implemented. This mode also can be used to verify unprotected internal ROM.

ROM -Protection	**ROM-Verification Mode (see 'AC Characteristics')**	**Restrictions**
no	ROM-Verification Mode 1 (standard 8051 Verification Mode) ROM-Verification Mode 2	–
yes	ROM-Verification Mode 2	– standard 8051 Verification Mode is disabled – externally applied MOVC accessing internal ROM is disabled

Data Memory ('Code Space')

The data memory space consists of an internal and an external memory space. The SAB 80C517A contains another 2 Kbyte on On-Chip RAM above the 256-bytes internal RAM of the base type SAB 80C517. This RAM is called XRAM in this document.

External Data Memory

Up to 64 Kbyte external data memory can be addressed by instructions that use 8-bit or 16-bit indirect addressing. For 8-bit addressing MOVX instructions in combination with registers R0 and R1 can be used. A 16-bit external memory addressing is supported by eight 16-bit datapointers. Registers XPAGE and SYSCON are controlling whether data fetches at addresses $F800_H$ to $FFFF_H$ are done from internal XRAM or from external data memory.

Internal Data Memory

The internal data memory is divided into four physically distinct blocks:

– the lower 128 bytes of RAM including four banks containing eight registers each

– the upper 128 byte of RAM

– the 128 byte special function register area.

– a 2 K $\times$ 8 area which is accessed like external RAM (MOVX-instructions), implemented on chip at the address range from $F800_H$ to $FFFF_H$. Special Function Register SYSCON controls whether data is read or written to XRAM or external RAM.

A mapping of the internal data memory is also shown in figure 2. The overlapping address spaces are accessed by different addressing modes (see User's Manual SAB 80C517). The stack can be located anywhere in the internal data memory.

Architecture for the XRAM

The contents of the XRAM is not affected by a reset or HW Power Down. After power-up the contents is undefined, while it remains unchanged during and after a reset or HW Power Down if the power supply is not turned off.

The additional On-Chip RAM is logically located in the "external data memory" range at the upper end of the 64 Kbyte address range ($F800_H$-$FFFF_H$). It is possible to enable and disable (only by reset) the XRAM. If it is disabled the device shows the same behaviour as the parts without XRAM, i.e. all MOVX accesses use the external bus to physically external data memory.

Accesses to XRAM

Because the XRAM is used in the same way as external data memory the same instruction types must be used for accessing the XRAM.

Note: *If a reset occurs during a write operation to XRAM, the effect on XRAM depends on the cycle which the reset is detected at (MOVX is a 2-cycle instruction):*

Reset detection at cycle 1: *The new value will not be written to XRAM. The old value is not affected.*

Reset detection at cycle 2: *The old value in XRAM is overwritten by the new value.*

Accesses to XRAM using the DPTR

There are a Read and a Write instruction from and to XRAM which use one of the 16-bit DPTR for indirect addressing. The instructions are:

MOVX A, @DPTR (Read)

MOVX @DPTR, A (Write)

Normally the use of these instructions would use a physically external memory. However, in the SAB 80C517A the XRAM is accessed if it is enabled and if the DPTR points to the XRAM address space (DPTR $\geqq$ $F800_H$).

Accesses to XRAM using the Registers R0/R1

The 8051 architecture provides also instructions for accesses to external data memory range which use only an 8-bit address (indirect addressing with registers R0 or R1). The instructions are:

MOVX A, @Ri (Read)

MOVX @Ri, A (Write)

In application systems, either a real 8-bit bus (with 8-bit address) is used or Port 2 serves as page register which selects pages of 256-byte. However, the distinction, whether Port 2 is used as general purpose I/O or as "page address" is made by the external system design. From the device’s point of view it cannot be decided whether the Port 2 data is used externally as address or as I/O data!

Hence, a special page register is implemented into the SAB 80C517A to provide the possibility of accessing the XRAM also with the MOVX @Ri instructions, i.e. XPAGE serves the same function for the XRAM as Port 2 for external data memory.

Special Function Register XPAGE

Addr. 91_H									XPAGE

The reset value of XPAGE is 00_H.

XPAGE can be set and read by software.

The register XPAGE provides the upper address byte for accesses to XRAM with MOVX @Ri instructions. If the address formed from XPAGE and Ri is less than the XRAM address range, then an external access is performed. For the SAB 80C517A the contents of XPAGE must be greater or equal than F8H in order to use the XRAM. Of course, the XRAM must be enabled if it shall be used with MOVX @Ri instructions.

Thus, the register XPAGE is used for addressing of the XRAM; additionally its contents are used for generating the internal XRAM select. If the contents of XPAGE is less than the XRAM address range then an external bus access is performed where the upper address byte is provided by P2 and not by XPAGE!

Therefore, the software has to distinguish two cases, if the MOVX @Ri instructions with paging shall be used:

a) Access to XRAM:	The upper address byte must be written to XPAGE or P2; both writes selects the XRAM address range.
b) Access to external memory:	The upper address byte must be written to P2; XPAGE will be loaded with the same address in order to deselect the XRAM.

Control of XRAM in the SAB 80C517A

There are two control bits in register SYSCON which control the use and the bus operation during accesses to the additional On-Chip RAM (XRAM).

Special Function Register SYSCON

Addr. $0B1_H$	—	—	—	—	—	—	XMAP1	XMAP0	SYSCON

Bit	Function
XMAP0	Global enable/disable bit for XRAM memory. XMAP0 = 0: The access to XRAM (= On-Chip XDATA memory) is enabled. XMAP0 = 1: The access to XRAM is disabled. All MOVX accesses are performed by the external bus (reset state).
XMAP1	Control bit for $\overline{RD}$/$\overline{WR}$ signals during accesses to XRAM; this bit has no effect if XRAM is disabled (XMAP0 = 1) or if addresses exceeding the XRAM address range are used for MOVX accesses. XMAP1 = 0: The signals $\overline{RD}$ and $\overline{WR}$ are not activated during accesses to XRAM. XMAP1 = 1: The signals $\overline{RD}$ and $\overline{WR}$ are activated during accesses to XRAM.

Reset value of SYSCON is xxxx xx01B.

The control bit XMAP0 is a global enable/disable bit for the additional On-Chip RAM (XRAM). If this bit is set, the XRAM is disabled, all MOVX accesses use external memory via the external bus. In this case the SAB 80C517A does not use the additional On-Chip RAM and is compatible with the types without XRAM.

XMAP0 is hardware protected by an unsymmetric latch. An unintentional disabling of XRAM could be dangerous since indeterminate values would be read from external bus. To avoid this the XMAP-bit is forced to '1' only by reset. Additionally, during reset an internal capacitor is loaded. So after reset state XRAM is disabled. Because of the load time of the capacitor XMAP0-bit once written to '0' (that is, discharging capacitor) cannot be set to '1' again by software. On the other hand any distortion (software hang up, noise, ...) is not able to load this capacitor, too. That is, the stable status is XRAM enabled. The only way to disable XRAM after it was enabled is a reset.

The clear instruction for XMAP0 should be integrated in the program initialization routine before XRAM is used. In extremely noisy systems the user may have redundant clear instructions.

The control bit XMAP1 is relevant only if the XRAM is accessed. In this case the externa $\overline{RD}$ and $\overline{WR}$ signals at P3.6 and P3.7 are not activated during the access, if XMAP1 is cleared. For debug purposes it might be useful to have these signals and the addresses at Ports 0.2 available. This is performed if XMAP1 is set.

The behaviour of Port 0 and P2 during a MOVX access depends on the control bits in register SYSCON and on the state of pin $\overline{EA}$. The table 1 lists the various operating conditions. It shows the following characteristics:

a) Use of P0 and P2 pins during the MOVX access.

   Bus: The pins work as external address/data bus. If (internal) XRAM is accessed, the data written to the XRAM can be seen on the bus in debug mode.

   I/0: The pins work as Input/Output lines under control of their latch.

b) Activation of the $\overline{RD}$ and $\overline{WR}$ pin during the access.

c) Use of internal or external XDATA memory.

The shaded areas describe the standard operation as each 80C51 device without on-chip XRAM behaves.

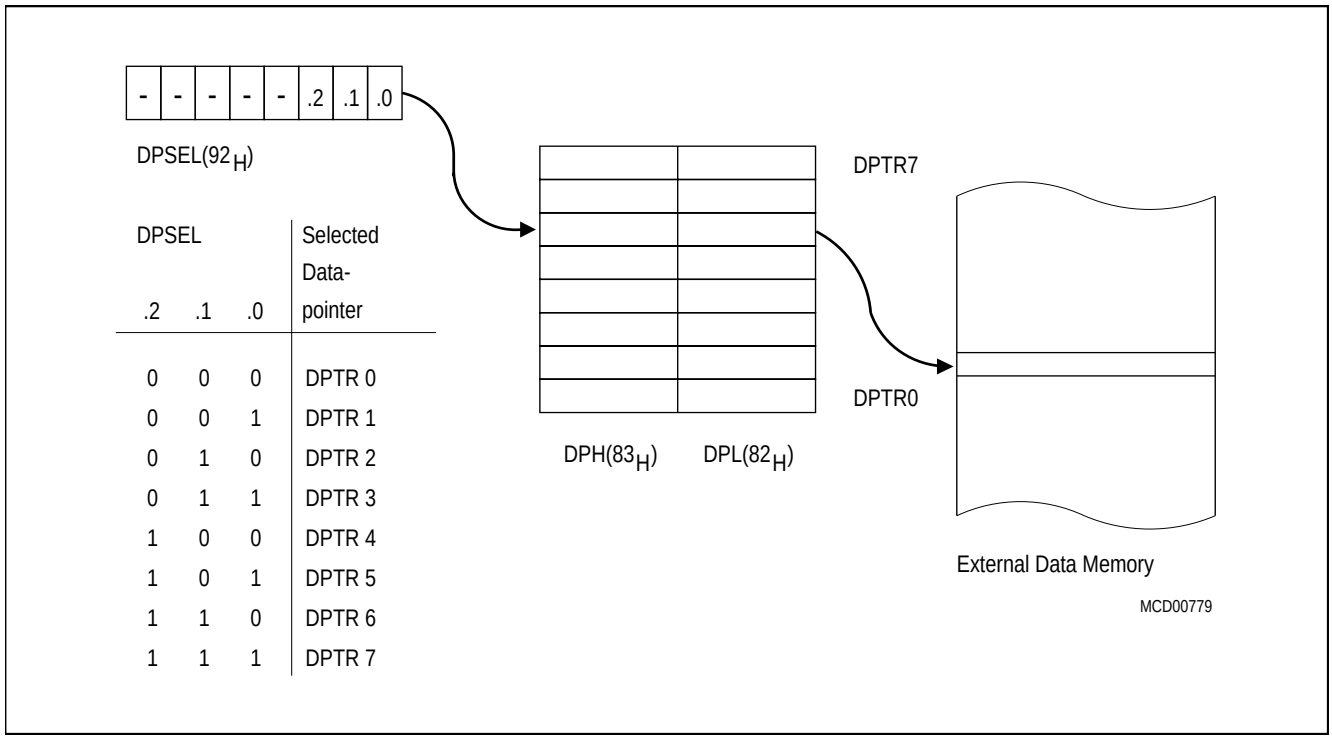
Table 1:
Behaviour of P0/P2 and $\overline{RD}$/$\overline{WR}$ during MOVX accesses

		$\overline{EA}$ = 0			$\overline{EA}$ = 1		
		XMAP1, XMAP0			XMAP1, XMAP0		
		00	10	X1	00	10	X1
MOVX @DPTR	DPTR < XRAM address range	a) P0/P2→Bus b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used
	DPTR ≥ XRAM address range	a) P0/P2→BUS ($\overline{WR}$ -Data only) b) $\overline{RD}$/$\overline{WR}$ inactive c) XRAM is used	a) P0/P2→BUS ($\overline{WR}$ -Data only) b) $\overline{RD}$/$\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used	a) P0/P2→I/0 b) $\overline{RD}$/$\overline{WR}$ inactive c) XRAM is used	a) P0/P2→BUS ($\overline{WR}$ -Data only) b) $\overline{RD}$/$\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used
MOVX @Ri	XPAGE < XRAM addr. page range	a) P0→Bus P2→I/0 b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used
	XPAGE ≥ XRAM addr. page range	P0/P2→BUS /R -Data only) 2→I/0 $\overline{RD}$/$\overline{WR}$ inactive XRAM is used	a) P0/P2→BUS ($\overline{WR}$ -Data only) P2→I/0 b) $\overline{RD}$/$\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/0 b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used	a) P0/P2→I/0 b) $\overline{RD}$/$\overline{WR}$ inactive c) XRAM is used	a) P0→BUS ($\overline{WR}$ -Data only) P2→I/0 b) $\overline{RD}$/$\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/0 b) $\overline{RD}$/$\overline{WR}$ active c) ext. memory is used

(shaded) modes compatible to 8051 - family

Multiple Datapointers

As a functional enhancement to standard 8051 controllers, the SAB 80C517A contains eight 16-bit datapointers. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointer is done in special function register DPSEL (data pointer select, addr. 92_H). Figure 3 illustrates the addressing mechanism.



DPSEL .2	.1	.0	Selected Data-pointer
0	0	0	DPTR 0
0	0	1	DPTR 1
0	1	0	DPTR 2
0	1	1	DPTR 3
1	0	0	DPTR 4
1	0	1	DPTR 5
1	1	0	DPTR 6
1	1	1	DPTR 7

Figure 3
Addressing of External Data Memory

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The 81 special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripherals. There are also 128 directly addressable bits within the SFR area. All special function registers are listed in table 1 and table 2.

In table 1 they are organized in numeric order of their addresses. In table 2 they are organized in groups which refer to the functional blocks of the SAB 80C517A.

Table 2
Special Function Register

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80_H	**P0** [1]	**FF_H**	**98_H**	**S0CON** [1]	**00_H**
81_H	SP	07_H	99_H	S0BUF	XX_H
82_H	DPL	00_H	$9A_H$	IEN2	$XX00\ 00X0_B$
83_H	DPH	00_H	$9B_H$	S1CON	$0X00\ 0000_B$
84_H	(WDTL) [3]	(00_H)	$9C_H$	S1BUF	XX_H
85_H	(WDTH) [3]	(00_H)	$9D_H$	S1RELL	00_H
86_H	WDTREL	00_H	$9E_H$	reserved	XX_H
87_H	PCON	00_H	$9F_H$	reserved	XX_H
88_H	**TCON** [1]	**00_H**	**$A0_H$**	**P2** [1]	**FF_H**
89_H	TMOD	00_H	$A1_H$	COMSETL	00_H
$8A_H$	TL0	00_H	$A2_H$	COMSETH	00_H
$8B_H$	TL1	00_H	$A3_H$	COMCLRL	00_H
$8C_H$	TH0	00_H	$A4_H$	COMCLRH	00_H
$8D_H$	TH1	00_H	$A5_H$	SETMSK	00_H
$8E_H$	reserved	XX_H [2]	$A6_H$	CLRMSK	00_H
$8F_H$	reserved	XX_H [2]	$A7_H$	reserved	XX_H [2]
90_H	**P1** [1]	**FF_H**	**$A8_H$**	**IEN0** [1]	**00_H**
91_H	XPAGE	00_H	$A9_H$	IP0	00_H
92_H	DPSEL	$XXXXX000_B$	AA_H	S0RELL	$D9_H$
93_H	reserved	XX_H [2]	AB_H	reserved	XX_H [2]
94_H	reserved	XX_H [2]	AC_H	reserved	XX_H [2]
95_H	reserved	XX_H [2]	AD_H	reserved	XX_H [2]
96_H	reserved	XX_H [2]	AE_H	reserved	XX_H [2]
97_H	reserved	XX_H [2]	AF_H	reserved	XX_H [2]

[1] Bit-addressable special function registers
[2] X means that the value is indeterminate and the location is reserved
[3] ( )... SFRs not user accessable

Table 2
Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$B0_H$	**P3** [1]	**FF_H**	**$D0_H$**	**PSW** [1]	**00_H**
$B1_H$	SYSCON	$XXXX\ XX01_B$	$D1_H$	IRCON1	00_H
$B2_H$	reserved	XX_H [2]	$D2_H$	CML0	00_H
$B3_H$	reserved	XX_H [2]	$D3_H$	CMH0	00_H
$B4_H$	reserved	XX_H [2]	$D4_H$	CML1	00_H
$B5_H$	reserved	XX_H [2]	$D5_H$	CMH1	00_H
$B6_H$	reserved	XX_H [2]	$D6_H$	CML2	00_H
$B7_H$	reserved	XX_H [2]	$D7_H$	CMH2	00_H
$B8_H$	**IEN1** [1]	**00_H**	**$D8_H$**	**ADCON0** [1]	**00_H**
$B9_H$	IP1	$XX00\ 0000_B$	$D9_H$	ADDATH	00_H
BA_H	S0RELH	$XXXX\ XX11_B$	DA_H	ADDATL	00_H
BB_H	S1RELH	$XXXX\ XX11_B$	DB_H	P7	XX_H
BC_H	reserved	XX_H	DC_H	ADCON1	$XXXX0000_B$
BD_H	reserved	XX_H	DD_H	P8	XX_H
BS_H	reserved	XX_H	DE_H	CTRELL	00_H
BF_H	reserved	XX_H	DF_H	CTRELH	00_H
$C0_H$	**IRCON0** [1]	**00_H**	**$E0_H$**	**ACC** [1]	**00_H**
$C1_H$	CCEN	00_H	$E1_H$	CTCON	$0X00\ 0000_B$
$C2_H$	CCL1	00_H	$E2_H$	CML3	XX_H
$C3_H$	CCH1	00H	$E3_H$	CMH3	00_H
$C4_H$	CCL2	00_H	$E4_H$	CML4	00_H
$C5_H$	CCH2	00_H	$E5_H$	CMH4	00_H
$C6_H$	CCL3	00_H	$E6_H$	CML5	00_H
$C7_H$	CCH3	00_H	$E7_H$	CMH5	00_H
$C8_H$	**T2CON** [1]	**00_H**	**$E8_H$**	**P4** [1]	**FF_H**
$C9_H$	CC4EN	00_H	$E9_H$	MD0	XX_H
CA_H	CRCL	00_H	EA_H	MD1	XX_H
CB_H	CRCH	00_H	EB_H	MD2	XX_H
CC_H	TL2	00_H	EC_H	MD3	XX_H
CD_H	TH2	00_H	ED_H	MD4	XX_H
CE_H	CCL4	00_H	EE_H	MD5	XX_H
CF_H	CCH4	00_H	EF_H	ARCON	$0XXX\ XXXX_B$

[1] Bit-addressable special function registers
[2] X means that the value is indeterminate and the location is reserved
[3] ( )... SFRs not user accessable

Table 2
Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$F0_H$	**B** [1]	**00_H**	**$F8_H$**	**P5** [1]	**FF_H**
$F1_H$	reserved	XX_H	$F9_H$	reserved	XX_H
$F2_H$	CML6	00_H	FA_H	P6	FF_H
$F3_H$	CMH6	00_H	FB_H	reserved	XX_H
$F4_H$	CML7	00_H	FC_H	reserved	XX_H
$F5_H$	CMH7	00_H	FD_H	(IS0)	XX_H
$F6_H$	CMEN	00_H	FE_H	(IS1)	XX_H
$F7_H$	CMSEL	00_H	FF_H	reserved	XX_H

[1] Bit-addressable special function registers
[2] X means that the value is indeterminate and the location is reserved
[3] ( )... SFRs not user accessable

Table 3
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** [1]	00_H
	B	B-Register	**$F0_H$** [1]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	92_H	$XXXX\ X000_B$ [3]
	PSW	Program Status Word Register	**$D0_H$** [1]	00_H
	SP	Stack Pointer	81_H	07_H
A/D-Converter	ADCON0	A/D Converter Control Register 0	**$D8_H$** [1]	00_H
	ADCON1	A/D Converter Control Register 1	DC_H	00_H
	ADDATH	A/D Converter Data Reg. High Byte	$D9_H$	00_H
	ADDATL	A/D Converter Data Reg. Low Byte	DA_H	00_H
Interrupt System	IEN0	Interrupt Enable Register 0	**$A8_H$** [1]	**00_H**
	CTCON [2]	Com. Timer Control Register	$E1_H$	$0XXX.0000_B$
	IEN1	Interrupt Enable Register 1	**$B8_H$** [1]	**00_H**
	IEN2	Interrupt Enable Register 2	$9A_H$	$XXXX.00X0_B$ [3]
	IP0	Interrupt Priority Register 0	$A9_H$	00_H
	IP1	Interrupt Priority Register 1	$B9_H$	$XX00\ 0000_B$
	IRCON0	Interrupt Request Control Register	**$C0_H$** [1]	00_H
	IRCON1	Interrupt Request Control Register	$D1_H$	00_H
	TCON [2]	Timer Control Register	**88_H** [1]	00_H
	TCON [2]	Timer 2 Control Register	**$C8_H$**	00_H
MUL/DIV Unit	ARCON	Arithmetic Control Register	EF_H	$0XXXX\ XXXX_B$
	MD0	Multiplication/Division Register 0	$E9_H$	XX_H
	MD1	Multiplication/Division Register 1	EA_H	XX_H
	MD2	Multiplication/Division Register 2	EB_H	XX_H
	MD3	Multiplication/Division Register 3	EC_H	XX_H
	MD4	Multiplication/Division Register 4	ED_H	XX_H
	MD5	Multiplication/Division Register 5	EE_H	XX_H

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Compare/ Capture- Unit (CCU) Timer 2	CCEN	Comp./Capture Enable Reg.	$C1_H$	00_H
	CC4EN	Comp./Capture Enable 4 Reg.	$C9_H$	00_H
	CCH1	Comp./Capture Reg. 1, High Byte	$C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$C7_H$	00_H
	CCH4	Comp./Capture Reg. 4, High Byte	CF_H	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$C2_H$	00_H
	CCL2	Comp./Capture Reg. 2, Low Byte	$C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$C6_H$	00_H
	CCL4	Comp./Capture Reg. 4, Low Byte	CE_H	00_H
	CMEN	Compare Enable Register	$F6_H$	00_H
	CMH0	Compare Register 0, High Byte	$D3_H$	00_H
	CMH1	Compare Register 1, High Byte	$D5_H$	00_H
	CMH2	Compare Register 2, High Byte	$D7_H$	00_H
	CMH3	Compare Register 3, High Byte	$E3_H$	00_H
	CMH4	Compare Register 4, High Byte	$E5_H$	00_H
	CMH5	Compare Register 5, High Byte	$E7_H$	00_H
	CMH6	Compare Register 6, High Byte	$F3_H$	00_H
	CMH7	Compare Register 7, High Byte	$F5_H$	00_H
	CML0	Compare Register 0, Low Byte	$D2_H$	00_H
	CML1	Compare Register 1, Low Byte	$D4_H$	00_H
	CML2	Compare Register 2, Low Byte	$D6_H$	00_H
	CML3	Compare Register 3, Low Byte	$E2_H$	00_H
	CML4	Compare Register 4, Low Byte	$E4_H$	00_H
	CML5	Compare Register 5, Low Byte	$E6_H$	00_H
	CML6	Compare Register 6, Low Byte	$F2_H$	00_H
	CML7	Compare Register 7, Low Byte	$F4_H$	00_H
	CMSEL	Compare Input Select	$F7_H$	00_H
	CRCH	Com./Rel./Capt. Reg. High Byte	CB_H	00_H
	CRCL	Com./Rel./Capt. Reg. Low Byte	CA_H	00_H
	COMSETL	Compare Register, Low Byte	$A1_H$	00_H
	COMSETH	Compare Register, High Byte	$A2_H$	00_H
	COMCLRL	Compare Register, Low Byte	$A3_H$	00_H
	COMCLRH	Compare Register, High Byte	$A4_H$	00_H
	SETMSK	Mask Register, concerning COMSET	$A5_H$	00_H

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Compare/ Capture- Unit (CCU), (cont'd)	CLRMSK	Mask Register, concerning COMCLR	$A6_H$	00_H
	CTCON	Com. Timer Control Reg.	$E1_H$	$0X00\ 0000_B$ 3)
	CTRELH	Com. Timer Rel. Reg., High Byte	DF_H	00_H
	CTRELL	Com. Timer Rel. Reg., Low Byte	DE_H	00_H
	TH2	Timer 2, High Byte	CD_H	00_H
	TL2	Timer 2, Low Byte	CC_H	00_H
	T2CON	Timer 2 Control Register	**$C8_H$** 1)	00_H
Ports	P0	Port 0	**80_H** 1)	FF_H
	P1	Port 1	**90_H** 1)	FF_H
	P2	Port 2	**$A0_H$** 1)	FF_H
	P3	Port 3	**$B0_H$** 1)	FF_H
	P4	Port 4	**$E8_H$** 1)	FF_H
	P5	Port 5	**$F8_H$** 1)	FF_H
	P6	Port 6,	FA_H	FF_H
	P7	Port 7, Analog/Digital Input	DB_H	
	P8	Port 8, Analog/Digital Input, 4-bit	DD_H	
Pow.Sav. Modes	PCON	Power Control Register	87_H	00_H
Serial Channels	**ADCON0** 2)	**A/D Converter Control Reg.**	**$D8_H$** 1)	**00_H**
	PCON 2)	Power Control Register	87_H	00_H
	S0BUF	Serial Channel 0 Buffer Reg.	99_H	XX_H 3)
	S0CON	**Serial Channel 0 Control Reg**.	**98_H** 1)	**00_H**
	S0RELL	Serial Channel 0, Reload Reg., low byte	$B2_H$	$0D9_H$
	S0RELH	Serial Channel 0, Reload Reg., high byte	BA_H	$XXXX.XX11_B$ 3)
	S1BUF	Serial Channel 1 Buffer Reg.,	$9C_H$	$0XX_H$ 3)
	S1CON	Serial Channel 1 Control Reg.	$9B_H$	$0X00.0000_B$ 3)
	S1REL	Serial Channel 1 Reload Reg., low byte	$9D_H$	00_H
	S1RELH	Serial Channel 1 Reload Reg., high byte	BB_H	$XXXX.XX11_B$ 3)

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Timer 0/ Timer 1	TCON	Timer Control Register	**88_H** [1]	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Watchdog	IEN0 [2]	Interrupt Enable Register 0	**$A8_H$** [1]	00_H
	IEN1 [2]	Interrupt Enable Register 1	**$B8_H$** [1]	00_H
	IP0 [2]	Interrupt Priority Register 0	$A9_H$	00_H
	IP1 [2]	Interrupt Priority Register 1	$B9_H$	$XX00\ 0000_B$ [3]
	WDTREL	Watchdog Timer Reload Reg.	86_H	00_H

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

A/D Converter

In the SAB 80C517A a new high performance / high-speed 12-channel 10-bit A/D-Converter is implemented. Its successive approximation technique provides 7 µs con-version time (f_{OSC}= 16 MHz). The conversion principle is upward compatible to the one used in the SAB 80C517. The main functional blocks are shown in figure 4.

The comparator is a fully differential comparator for a high power supply rejection ratio and very low offset voltages. The capacitor network is binary weighted providing genuine 10-bit resolution.

The table below shows the sample time T_S and the conversion time T_C, which are dependend on f_{OSC} and a new prescaler (see also Bit ADCL in SFR ADCON 1).

f_{OSC} [MHz]	Prescaler	f_{ADC} [MHz]	Sample Time T_S [µs]	Conversion Time (incl. sample time) T_C [µs]
12	÷ 8	1.5	2.67	9.33
	÷ 16	0.75	5.33	18.66
16	÷ 8	2.0	2.0	7.0
	÷ 16	1.0	4.0	14.0
18	÷ 8	–	–	–
	÷ 16	1.125	3.55	12.4

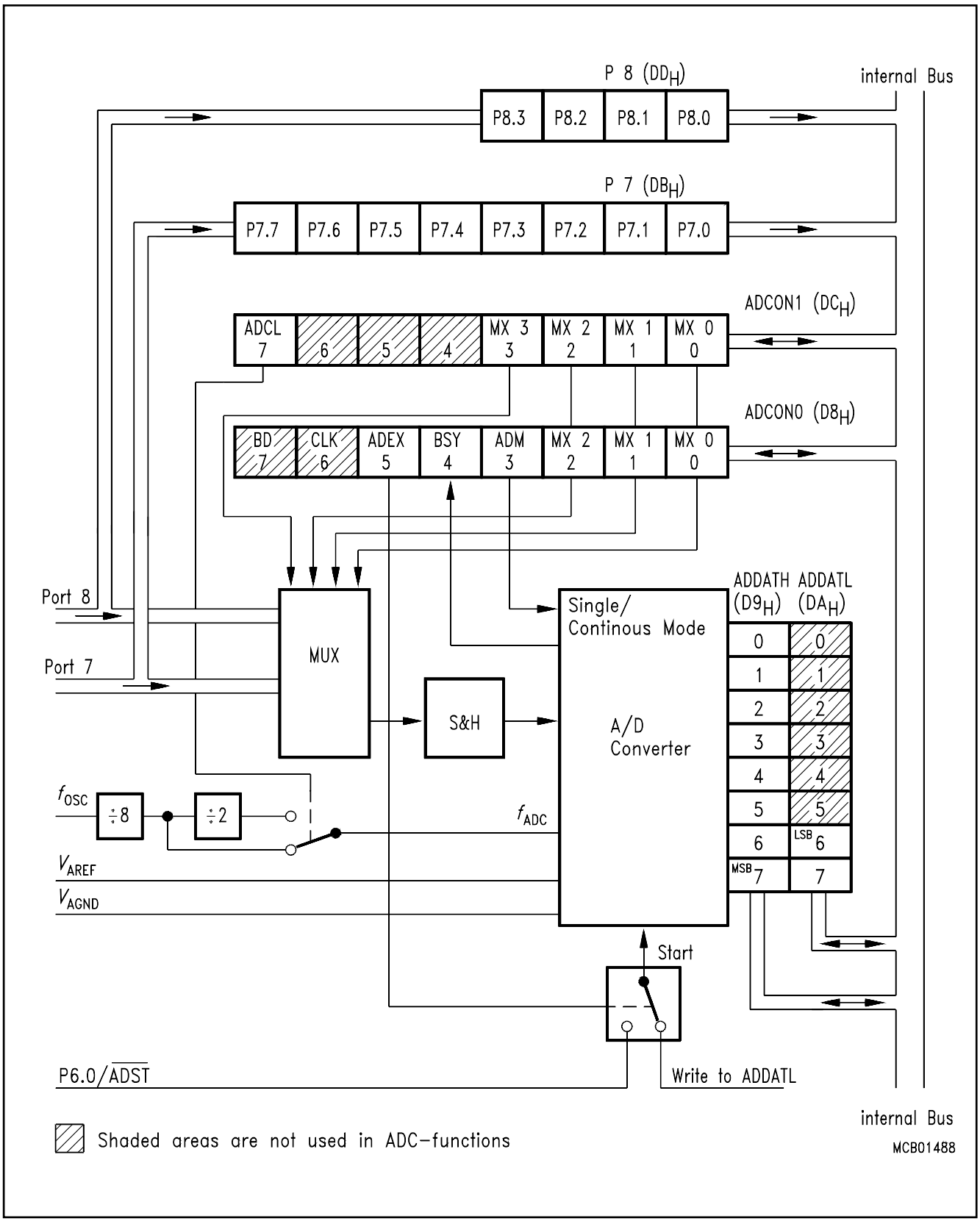


Figure 4
Block Diagram A/D Converter

Compare/Capture Unit (CCU)

The compare/capture unit is a complex timer/register array for applications that require high speed I/O pulse width modulation and more timer/counter capabilities.
The CCU contains

- one 16-bit timer/counter **(timer2)** with 2-bit prescaler, reload capability and a max. clock frequency of $f_{OSC/12}$ (1 MHz with a 12 MHz crystal).
- one 16-bit timer **(compare timer)** with 8-bit prescaler, reload capability and a max. clock frequency of $f_{OSC/2}$ (6 MHz with a 12 MHz crystal).
- fifteen 16-bit compare registers.
- five of which can be used as 16-bit capture registers.
- up to 21 output lines controlled by the CCU.
- nine interrupts which can be generated by CCU-events.

Figure 5 shows a block diagram of the CCU. Eight compare registers (CM0 to CM7) can individually be assigned to either timer 2 or the compare timer. Diagrams of the two timers are shown in figures 6 and 7. The four compare/capture registers, the compare/reload/capture register and the comset/comclr register are always connected to timer 2. Depending on the register type and the assigned timer three different compare modes can be selected.
Table 3 illustrates possible combinations and the corresponding output lines.

Table 4
CCU Compare Configuration

Assigned Timer	Compare Register	Compare Output	Possible Modes
Timer 2	CRCH/CRCL	P1.0/$\overline{\text{INT3}}$/CC0	Comp. mode 0, 1 + Reload
	CC1H/CC1L	P1.1/INT4/CC1	Comp. mode 0, 1
	CC2H/CC2L	P1.2/INT5/CC2	Comp. mode 0, 1
	CC3H/CC3L	P1.3/INT6/CC3	Comp. mode 0, 1
	CC4H/CC4L	P1.4/$\overline{\text{INT2}}$/CC4	Comp. mode 0, 1
	CC4H/CC4L	P5.0/CCM0	Comp. mode 1
	:	:	:
	CC4H/CC4L	P5.7/CCM7	Comp. mode 1
	COMSETL/COMSETH	P5.0/CCM0	Comp. mode 2
		:	:
		P5.7/CCM7	Comp. mode 2
	COMCLRL/	P5.0/CCM0	Comp. mode 2
	COMCLRH	:	:
		P5.7/CCM7	Comp. mode 2
		P4.0/CM0	Comp. mode 1
	CM0H/CM0L	:	:
	:	P4.7/CM7	Comp. mode 1
	CM7H/CM7L		
Compare timer	CM0H/CM0L	P4.0/CM0	Comp. mode 0 (with shadow latches)
	:	:	:
	CM7H/CM7L	P4.7/CM7	Comp. mode 0 (with shadow latches)

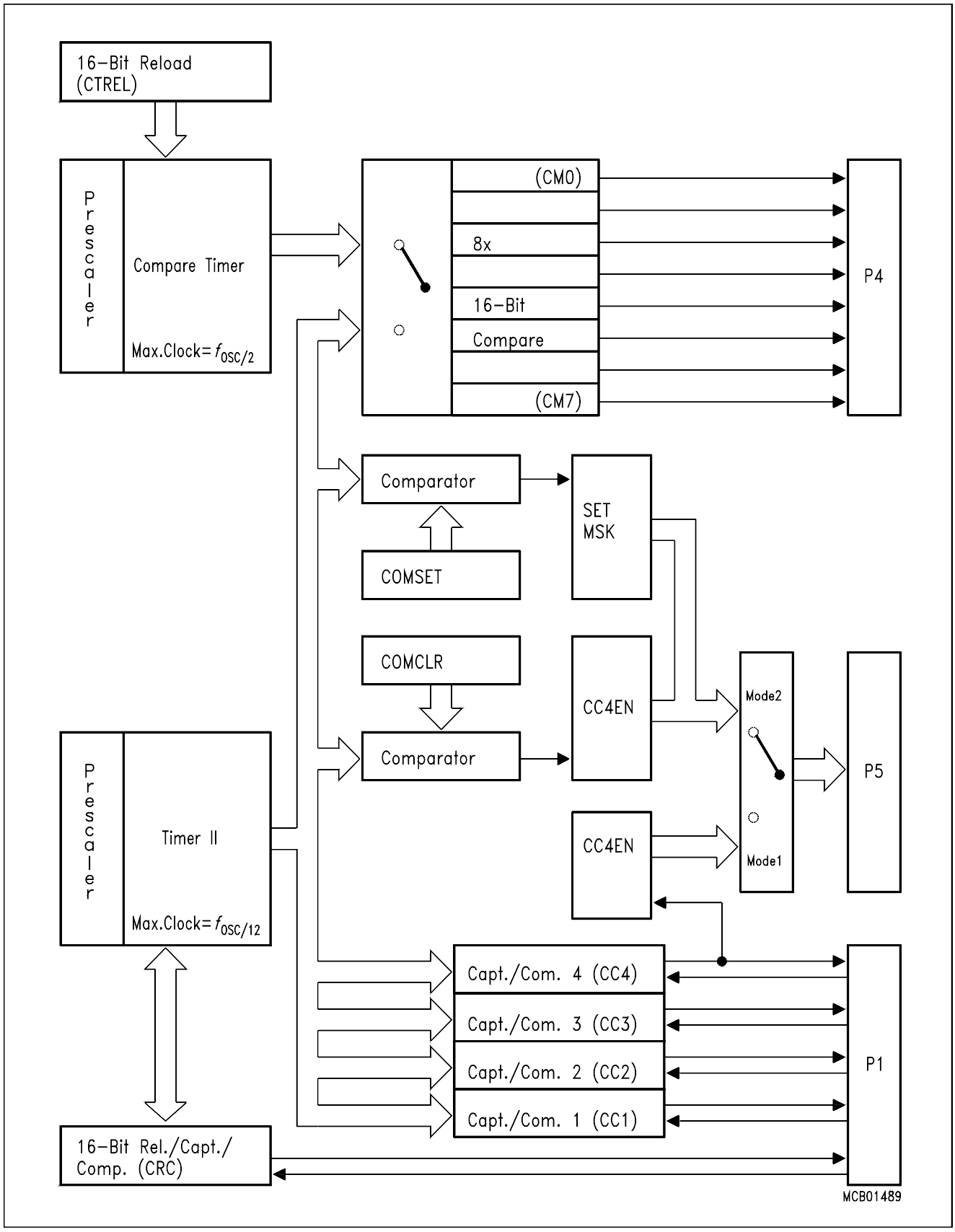


Figure 5
Block Diagram of the Compare/Capture Unit

Compare

In compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 register or the compare timer register. If the count value in the timer registers matches one of the stored value, an appropriate output signal is generated at the corresponding pin(s) and an interrupt is requested. Three compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It returns to low level at timer overflow.

Mode 1: The transition of the output signal can be determined by software. A timer overflow signal does not affect the compare-output.

Mode 2: In compare mode 2 the concurrent compare output pins on Port 5 are used as follows (see figure 9)

- When a compare match occurs with register COMSET, a high level appears at the pins of port 5 whose corresponding bits in the mask register SETMSK (address $0A5_H$) are set.
- When a compare match occurs in register COMCLR, a low level appears at the pins of port 5 whose corresponding bits in the mask register CLRMSK (address $0A6_H$) are set.

  Additionally the Port 5 pins used for compare mode 2 may also be directly written to by write instructions to SFR P5. Of course, the pins can also be read under program control.

Compare registers CM0 to CM7 use additional compare latches when operated in mode 0. Figure 8 shows the function of these latches. The latches are implemented to prevent from loss of compare matches which may occur when loading of the compare values is not correlated with the timer count. The compare latches are automatically loaded from the compare registers at every timer overflow.

Capture

This feature permits saving of the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to 'freeze' the current 16-bit value of timer 2 registers into a dedicated capture register.

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Reload of Timer 2

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Timer/Counters 0 and 1

These timer/counters are fully compatible with timer/counter 0 or 1 of the SAB 8051 and can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

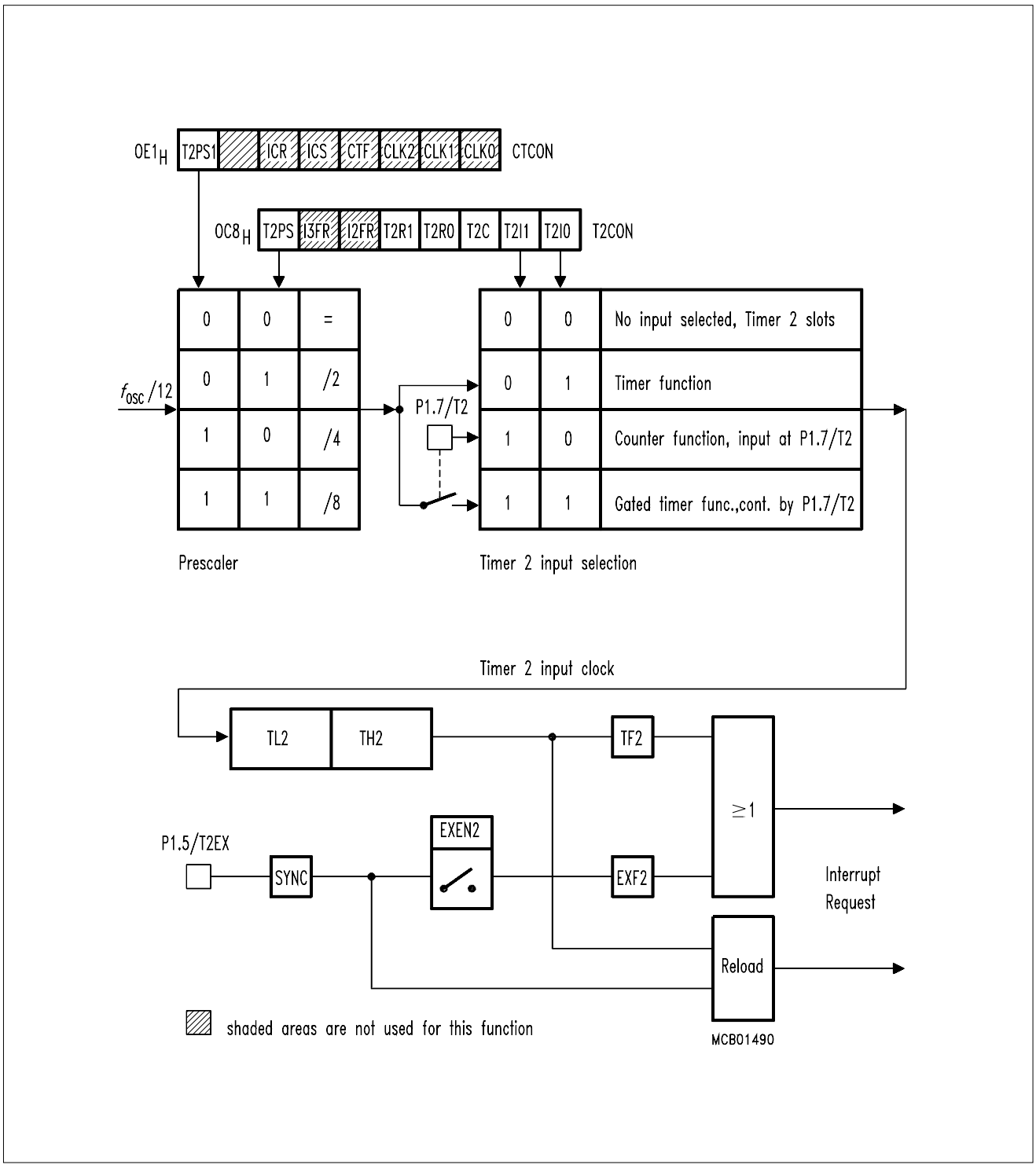


Figure 6
Block Diagram of Timer 2

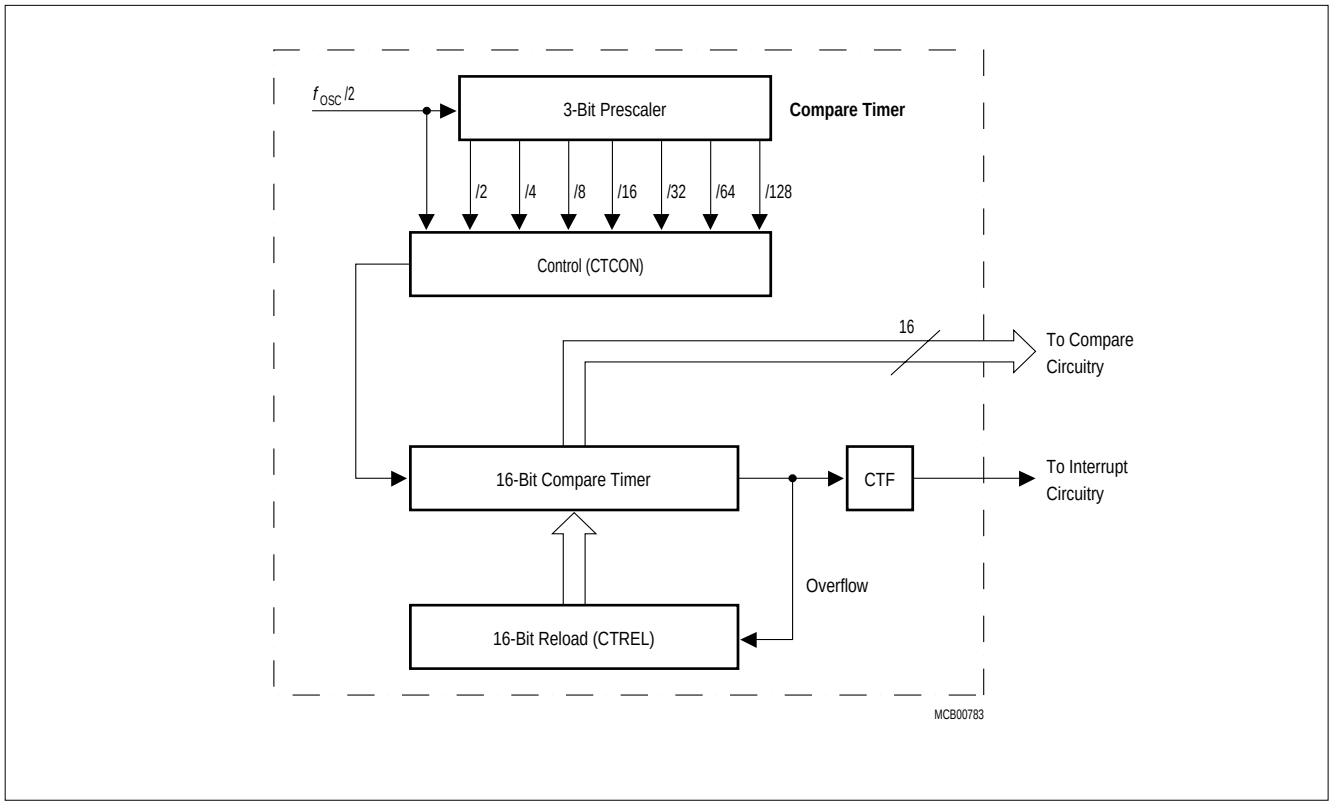


Figure 7
Block Diagram of the Compare Timer

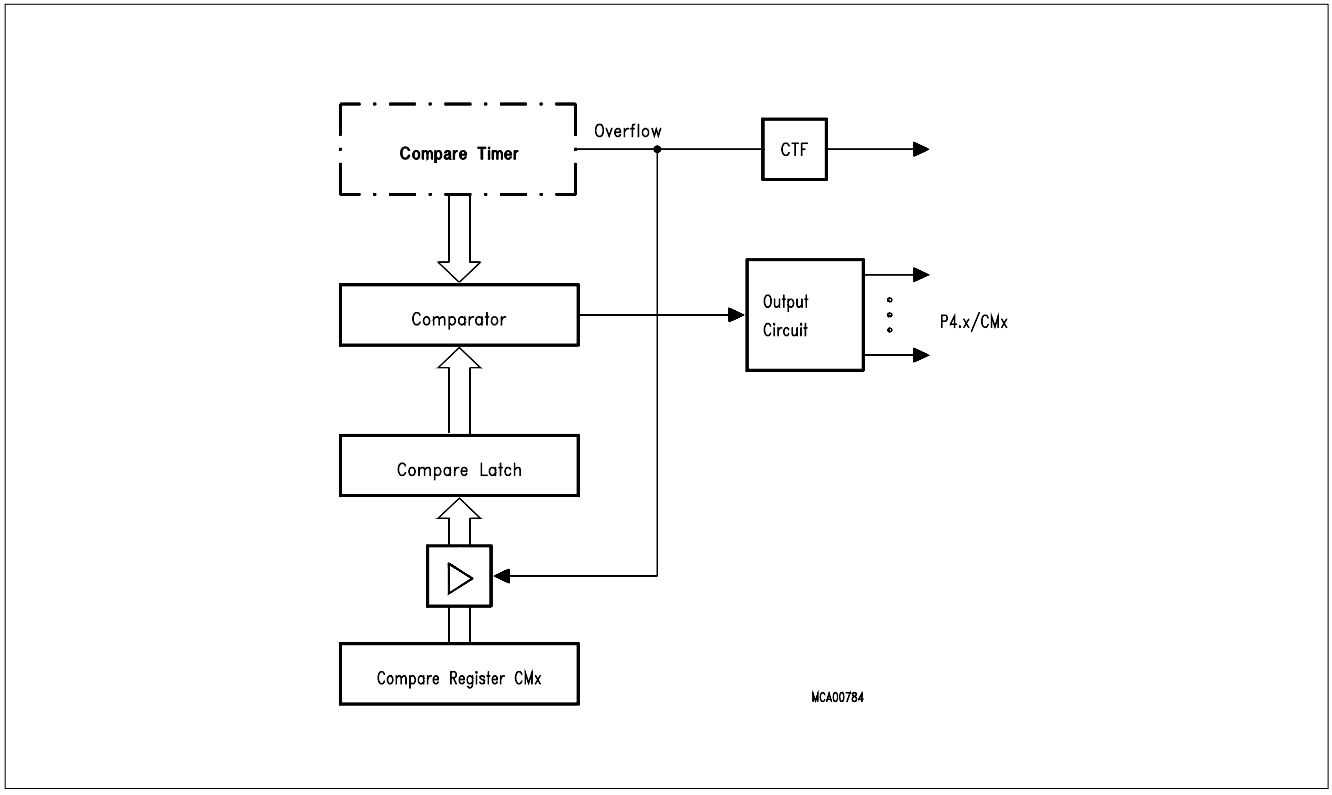


Figure 8
Compare-Mode 0 with Registers CM0 to CM7

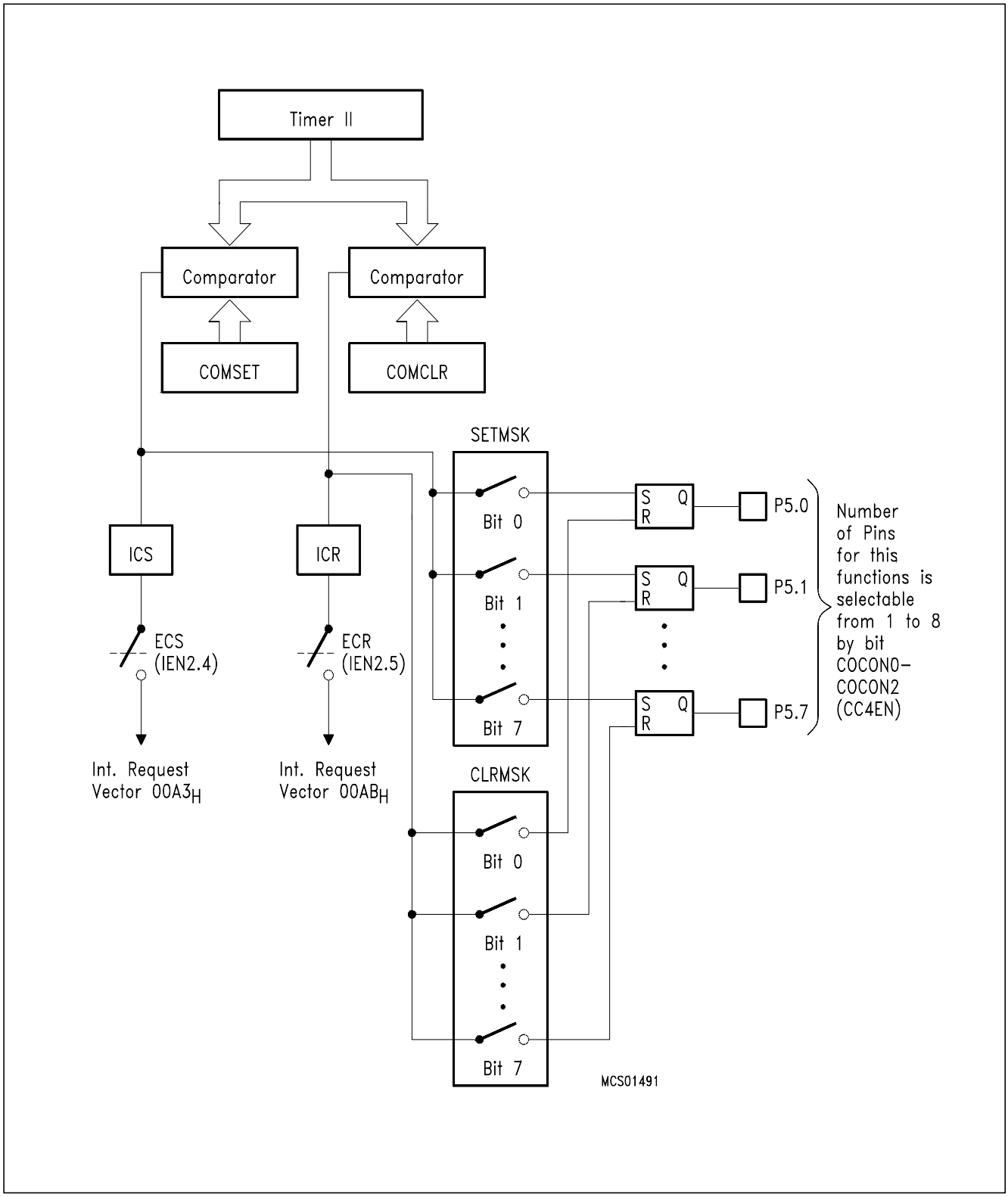


Figure 9
Compare-Mode 2 (Port 5 only)

Interrupt Structure

The SAB 80C517A has 17 interrupt vectors with the following vector addresses and request flags.

Table 5
Interrupt Sources and Vectors

Interrupt Request Flags	Interrupt Vector Address	Interrupt Source
IE0	0003_H	External interrupt 0
TF0	$000B_H$	Timer 0 overflow
IE1	0013_H	External interrupt 1
TF1	$001B_H$	Timer 1 overflow
RI0 + TI0	0023_H	Serial channel 0
TF2 + EXF2	$002B_H$	Timer 2 overflow/ext. reload
IADC	0043_H	A/D converter
IEX2	$004B_H$	External interrupt 2
IEX3	0053_H	External interrupt 3
IEX4	$005B_H$	External interrupt 4
IEX5	0063_H	External interrupt 5
IEX6	$006B_H$	External interrupt 6
RI1/TI1	0083_H	Serial channel 1
ICMP0 to ICMP7	0093_H	Compare match interrupt of Compare Registers CM0-CM7 assigned to Timer 2
CTF	$009B_H$	Compare timer overflow
ICS	$00A3_H$	Compare match interrupt of Compare Register COMSET
ICR	$00AB_H$	Compare match interrupt of Compare Register COMCLR

Each interrupt vector can be individually enabled/disabled. The response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 2 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs or triples. Each pair or triple can be programmed individually to one of four priority levels by setting or clearing one bit in special function register IP0 and one in IP1. Figure 9 shows the interrupt request sources, the enabling and the priority level structure.

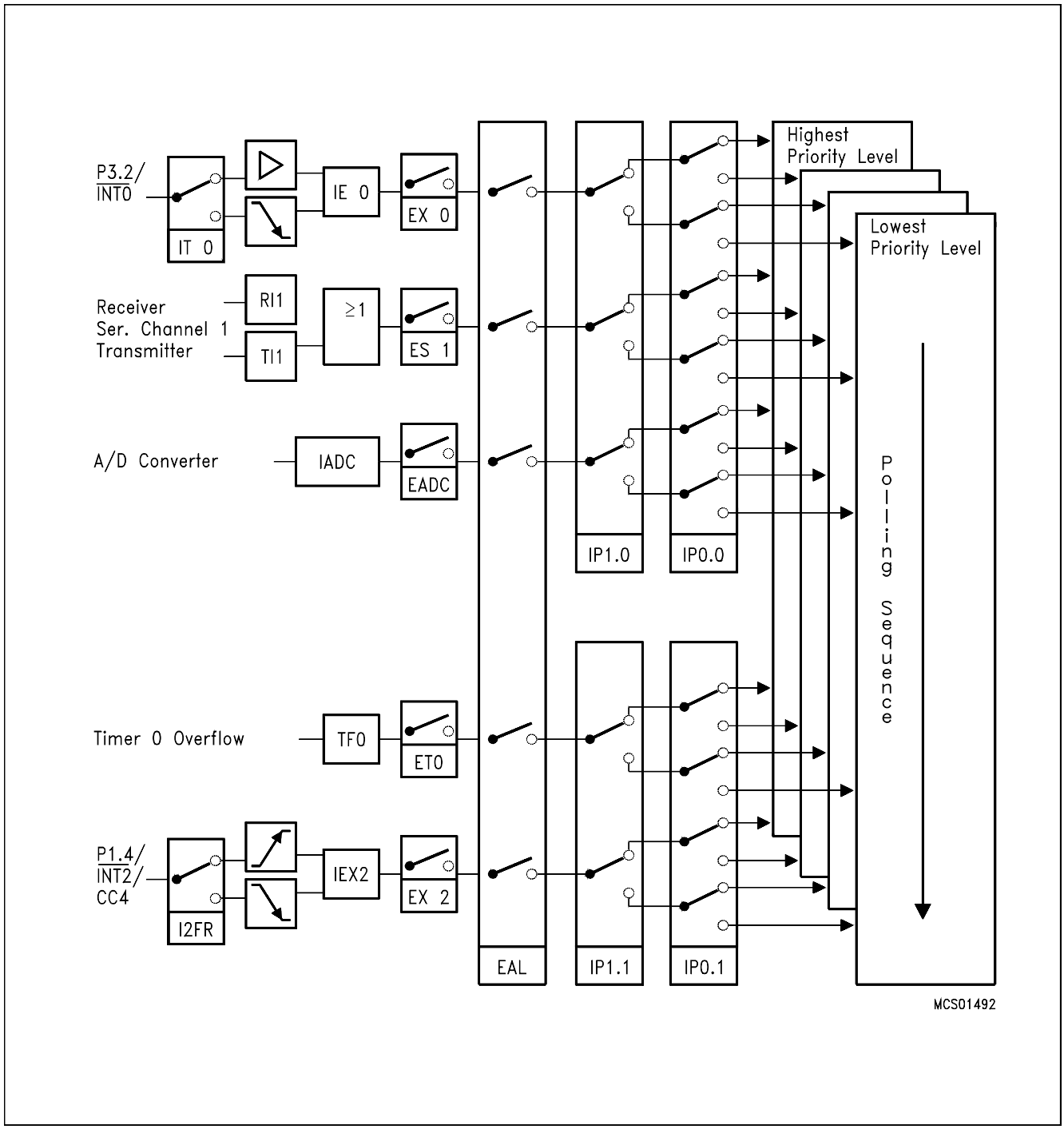


Figure 10
Interrupt Structure of the SAB 80C517A

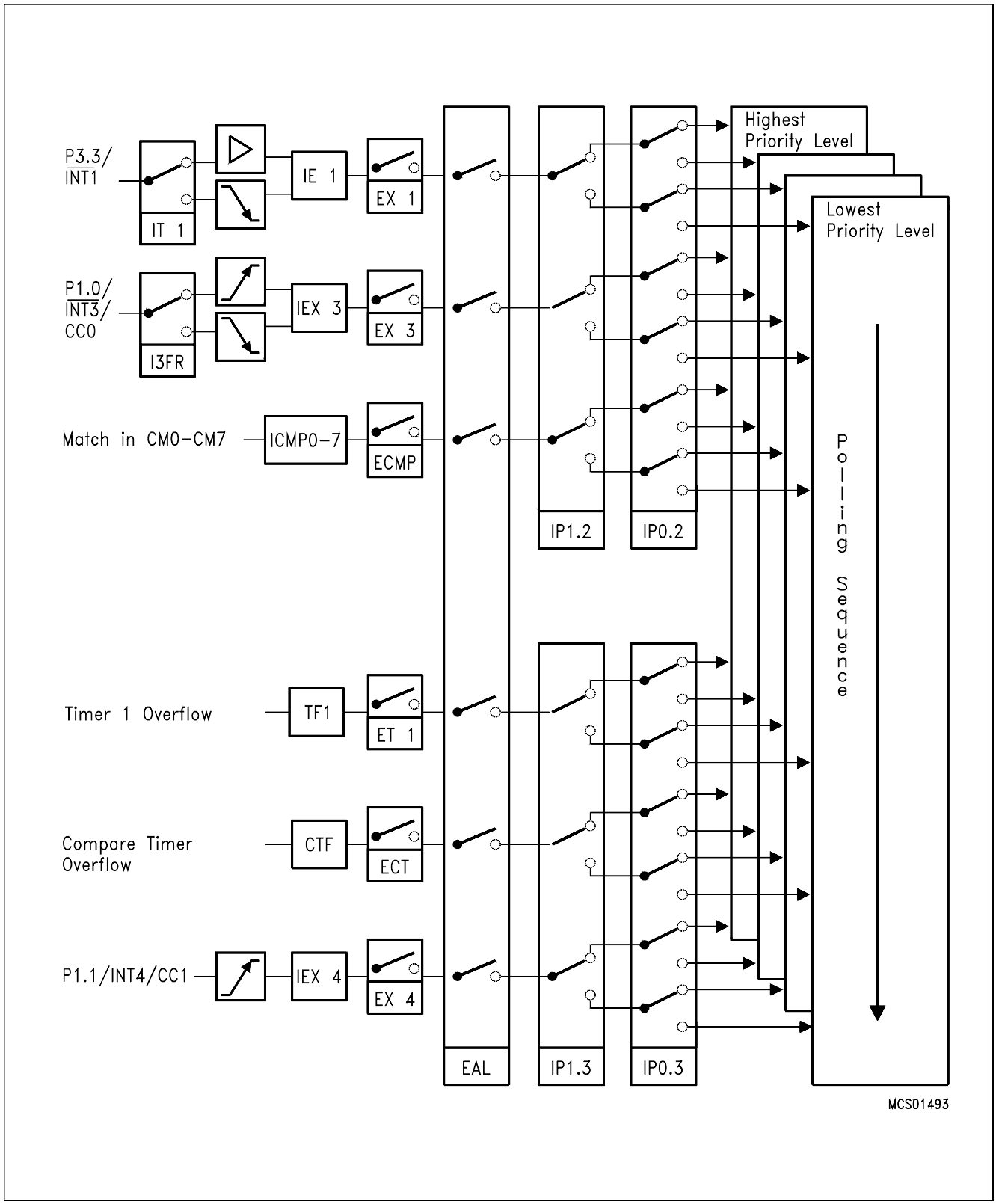


Figure 10
Interrupt Structure of the SAB 80C517A (cont'd)

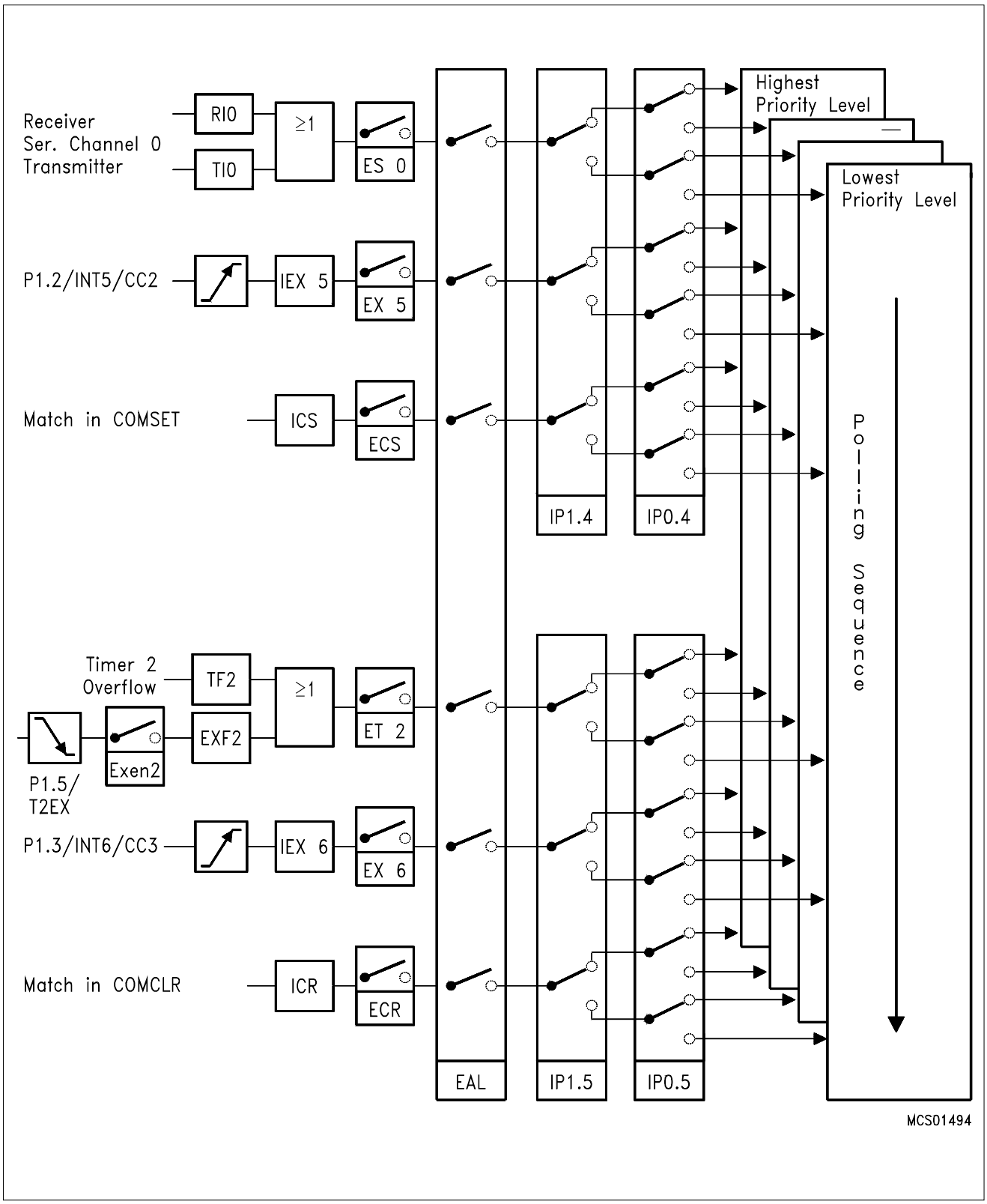


Figure 10
Interrupt Structure of the SAB 80C517A (cont'd)

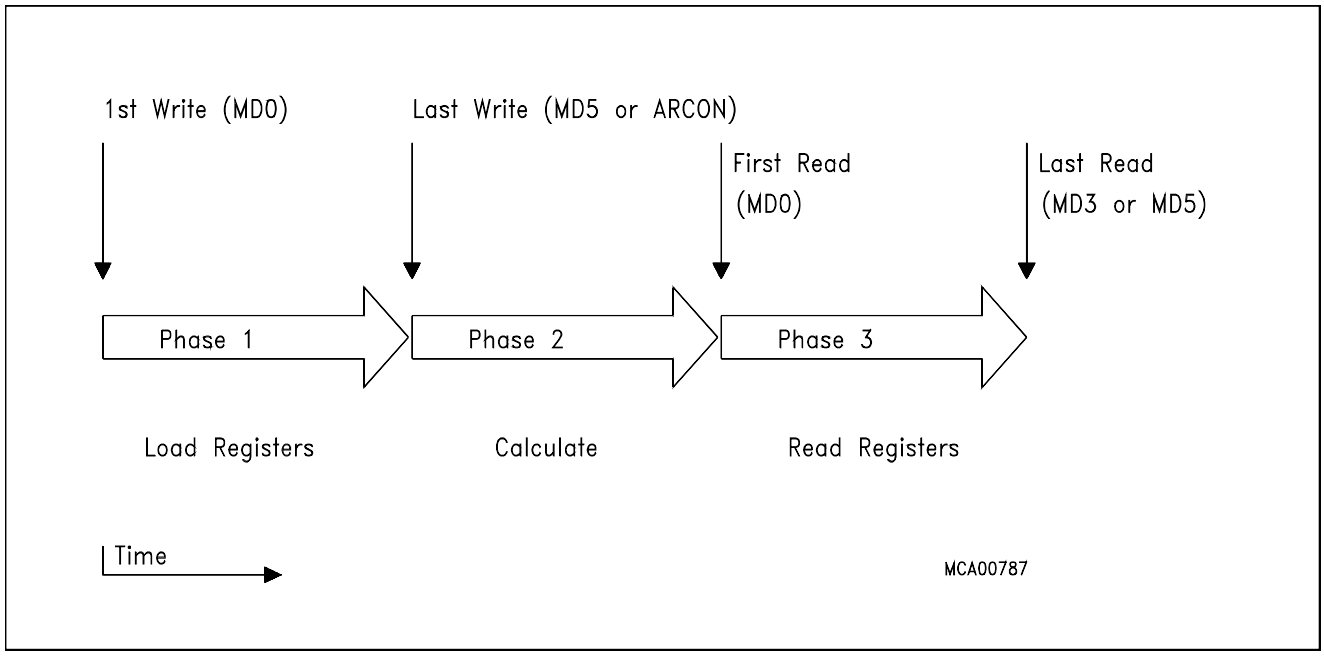
Multiplication/Division Unit

This on-chip arithmetic unit provides fast 32-bit division, 16-bit multiplication as well as shift and normalize features. All operations are integer operation.

Operation	Result	Remainder	Execution Time
32-bit/16-bit	32-bit	16-bit	6 t_{cy} [1]
16-bit/16-bit	16-bit	16-bit	4 t_{cy}
16-bit *16-bit	32-bit	–	4 t_{cy}
32-bit normalize	–	–	6 t_{cy} [2]
32-bit shift left/right	–	–	6 t_{cy} [2]

[1] 1 t_{cy} = 1 µs @ 12 MHz oscillator frequency.
[2] The maximal shift speed is 6 shifts/cycle.

The MDU consists of six registers used for operands and results and one control register. Operation of the MDU can be divided in three phases:



Operation of the MDU

To start an operation, register MD0 to MD5 (or ARCON) must be written to in a certain sequence according to table 5 or 6. The order the registers are accessed determines the type of the operation. A shift operation is started by a final write operation to register ARCON (see also the register description).

I/O Ports

The SAB 80C517A has seven 8-bit I/O ports and two input ports (8-bit and 4-bit wide).

Port 0 is an open-drain bidirectional I/O port, while ports 1 to 6 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 6 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pull-up FET. Port 1, 3, 4, 5 and port 6 provide several alternate functions. Please see the "Pin Description" for details.

Port pins show the information written to the port latches, when used as general purpose port. When an alternate function is used, the port pin is controlled by the respective peripheral unit. Therefore the port latch must contain a "one" for that function to operate. The same applies when the port pins are used as inputs. Ports 1, 3, 4 and 5 are bit- addressable.

The SAB 80C517A has two dual-purpose input ports. The twelve port lines at port 7 and port 8 can be used as analog inputs for the A/D converter. If input voltages at P7 and P8 meet the specified digital input levels (V_{IL} and V_{IH}) the port can also be used as digital input port.

In Hardware Power Down Mode the port pins and several control lines enter a floating state. For more details see the section about Hardware Power Down Mode.

Power Saving Modes

The SAB 80C517A provides – due to Siemens ACMOS technology – four modes in which power consumption can be significantly reduced.

– The **Slow Down Mode**
  The controller keeps up the full operating functionality, but is driven with one eighth of its normal operating frequency. Slowing down the frequency remarkable reduces power consumption.

– The **Idle Mode**
  The CPU is gated off from the oscillator, but all peripherals are still supplied with the clock and continue working.

– The **Power Down Mode**
  Operation of the SAB 80C517A is stopped, the on-chip oscillator and the RC-oscillator are turned off. This mode is used to save the contents of the internal RAM with a very low standby current.

– **The Hardware Power Down Mode**
  Operation of the SAB 80C517A is stopped, the on-chip oscillator and the RC-Oscillator are turned off. The pin $\overline{\text{HWPD}}$ controls this mode. Port pins and several control lines enter a floating state. The Hardware Power Down Mode is independent of the state of pin $\overline{\text{PE}}$/SWD.

Hardware Enable for Software controlled Power Saving Modes

A dedicated Pin $\overline{\text{PE}}$/SWD) of the SAB 80C517A allows to block the Software controlled power saving modes. Since this pin is mostly used in noise-critical application it is combined with an automatic start of the Watchdog Timer.

$\overline{\text{PE}}$/SWD = V_{IH} (logic high level):	Using of the power saving modes is not possible. The watchdog timer starts immediately after reset. The instruction sequences used for entering of power saving modes will not affect the normal operation of the device.
$\overline{\text{PE}}$/SWD = V_{IL} (logic low level):	All power saving modes can be activated by software.

When left unconnected, Pin /$\overline{\text{PE}}$/SWD is pulled high by a weak internal pullup. This is done to provide system protection on default.

The logic-level applied to pin $\overline{\text{PE}}$/SWD can be changed during program execution to allow or to block the use of the power saving modes without any effect on the on-chip watchdog circuitry.

Requirements for Hardware Power Down Mode

There is no dedicated pin to enable the Hardware Power Down Mode. Nevertheless for a correct function of the Hardware Power Down Mode the oscillator watchdog unit including its internal RC oscillator is needed. Therefore this unit must be enabled by pin OWE (OWE = high). However, the control pin $\overline{PE}$/SWD has no control function in this mode. It enables and disables only the use of software controlled power saving modes.

Software controlled power saving modes

All of these modes are entered by software. Special function register PCON (power control register, address is 87_H) is used to select one of these modes.

Slow Down Mode

During slow down operation all signal frequencies that are derived from the oscillator clock, are divided by eight, also the clockout signal and the watchdog timer count.

The slow down mode is enabled by setting bit SD. The controller actually enters the slow down mode after a short synchronisation period (max. 2 machine cycles).

The slow down mode is disabled by clearing bit SD.

Idle Mode

During idle mode all peripherals of the SAB 80C517A (except for the watchdog timer) are still supplied by the oscillator clock. Thus the user has to take care which peripheral should continue to run and which has to be stopped during Idle.

The procedure to enter the idle mode is similar to the one entering the power down mode. The two bits IDLE and IDLS must be set by two consecutive instructions to minimize the chance of unintentional activating of the idle mode.

There are two ways to terminate the idle mode:

– The idle mode can be terminated by activating any enabled interrupt. This interrupt will be serviced and the instruction to be executed following the RETI instruction will be the one following the instruction that set the bit IDLS.

– The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. The control signals ALE and hold at logic high levels $\overline{PSEN}$ (see table 8).

Power Down Mode

The power down mode is entered by two consecutive instructions directly following each other. The first instruction has to set the flag PDE (power down enable) and must not set PDS (power down set). The following instruction has to set the start bit PDS. Bits PDE and PDS will automatically be cleared after having been set.

The instruction that sets bit PDS is the last instruction executed before going into power down mode. The only exit from power down mode is a hardware reset.

The status of all output lines of the controller can be looked up in table 8.

Hardware Controlled Power Down Mode

The pin $\overline{\text{HWPD}}$ controls this mode. If it is on logic high level (inactive) the part is running in the normal operating modes. If pin $\overline{\text{HWPD}}$ gets active (low level) the part enters the Hardware Power Down Mode; this is independent of the state of pin $\overline{\text{PE}}$/SWD.

$\overline{\text{HWPD}}$ is sampled once per machine cycle. If it is found active, the device starts a complete internal reset sequence. The watchdog timer is stopped and its status flag WDTS is cleared exactly the same effects as a hardware reset. In this phase the power consumption is not yet reduced. After completion of the internal reset both oscillators of the chip are disabled. At the same time the port pins and several control lines enter a floating state as shown in table 8. In this state the power consumption is reduced to the power down current IPD. Also the supply voltage can be reduced. Table 8 also lists the voltages which may be applied at the pins during Hardware Power Down Mode without affecting the low power consumption.

Termination of HWPD Mode:

This power down state is maintained while pin $\overline{\text{HWPD}}$ is held active. If HWPD goes to high level (inactive state) an automatic start up procedure is performed:

- First the pins leave their floating condition and enter their default reset state (as they had immediately before going to float state).
- Both oscillators are enabled (only if OWE = high). The oscillator watchdog's RC oscillator starts up very fast (typ. less than 2 microseconds).
- Because the oscillator watchdog is active it detects a failure condition if the on-chip oscillator hasn't yet started. Hence, the watchdog keeps the part in reset and supplies the internal clock from the RC oscillator.
- Finally, when the on-chip oscillator has started, the oscillator watchdog releases the part from reset with oscillator watchdog status flag not set. When automatic start of the watchdog was enabled ($\overline{\text{PE}}$/SWD connected to V_{CC}), the Watchdog Timer will start, too (with its default reload value for time-out period).
- The $\overline{\text{Reset}}$ pin overrides the Hardware Power Down function, i.e. if reset gets active during Hardware Power Down it is terminated and the device performs the normal reset function. (Thus, pin $\overline{\text{Reset}}$ has to be inactive during Hardware Power Down Mode).

Table 8
Status of all pins during Idle Mode, Power Down Mode and Hardware Power Down Mode

Pins	Idle Mode Last instruction executed from		Power Down Mode Last instruction executed from		Hardware Power Down	
	internal ROM	external ROM	internal ROM	external ROM	Status	Voltage range at pin
P0	Data	float	Data	float		
P1	Data alt outputs	Data alt outputs	Data last outputs	Data last outputs	floating	
P2	Data	Address	Data	Data	output	
P3	Data alt outputs	Data alt outputs	Data last output	Data last output	outputs	
P4	Data alt outputs	Data alt outputs	Data last outputs	Data last output	disabled	$V_{SS} \leq V_{IN} \leq V_{CC}$
P5	Data alt output	Data alt output	Data last output	Data last output	input	
P6	Data alt output	Data alt output	Data last output	Data last output	function	
P7						
P8						
EA					active input	$V_{IN} = V_{CC}$ or $V_{IN} = V_{SS}$
$\overline{PE}$/SWD					active input pull-up disabled	$V_{IN} = V_{CC}$ or $V_{IN} = V_{SS}$
XTAL1					active output	pin may not be driven
XTAL2					disabled input functions	$V_{SS} \leq V_{IN} \leq V_{CC}$

Table 8
Status of all pins during Idle Mode, Power Down Mode and Hardware Power Down Mode (cont'd)

Pins	Idle Mode Last instruction executed from		Power Down Mode Last instruction executed from		Hardware Power Down	
	internal ROM	**external ROM**	**internal ROM**	**external ROM**	**Status**	**Voltage range at pin**
$\overline{\text{PSEN}}$					floating outp. disabled input functions	$V_{SS} \le V_{IN} \le V_{CC}$
ALE						
VAREF VAGND					active supply pins	$V_{AGND} \le V_{IN} \le V_{CC}$
OWE					active input, must be high pull-up disabl.	$V_{IN} = V_{CC}$
$\overline{\text{RESET}}$					active input must be high	$V_{IN} = V_{CC}$
$\overline{\text{RO}}$					floating output	$V_{SS} \le V_{IN} \le V_{CC}$

Serial Interfaces

The SAB 80C517A has two serial interfaces. Both interfaces are full duplex and receive buffered. They are functionally identical with the serial interface of the SAB 8051 when working as asynchronous channels. Serial interface 0 additionally has a synchronous mode. Table 9 shows possible configurations and the according baud rates.

Table 9
Baud Rate Generation

	Mode		**Mode 0**			–
8-Bit syn-chron-ous channel	Baud-rate	f_{OSC} =1 2 MHz	1MHz			–
		f_{OSC} = 16 MHz	1.33 MHz			–
		f_{OSC} = 18 MHz	1.5 MHz			–
	derived from		f_{OSC}			–
	Mode		**Mode 1**			**Mode B**
8-Bit UART	Baud-rate	f_{OSC} = 12 MHz	1 Baud – 62.5 kBaud		183 Baud – 375 kBaud	366 Baud – 375 kBaud
		f_{OSC} = 16 MHz	1 Baud – 83 kBaud		244 Baud – 500 kBaud	244 Baud – 500 kBaud
		f_{OSC} = 18 MHz	1 Baud – 93.7 kBaud		2375 Baud – 562.5 kBaud	549 Baud – 562.5 kBaud
	derived from		Timer 1		10-Bit Baudrate Generator	10-Bit Baudrate Generator
	Mode		**Mode 2**	**Mode 3**		**Mode A**
9-Bit UART	Baud-rate	f_{OSC} = 12 MHz	187.5 kBaud/ 375 kBaud	1 Baud – 62.5 kBaud	183 Baud – 75 kBaud	183 Baud – 75 kBaud
		f_{OSC}= 16 MHz	250 Baud/ 500 kBaud	1 Baud – 83.3 kBaud	244 Baud – 500 kBaud	244 Baud – 500 kBaud
		f_{OSC} = 18 MHz	281.2 kBaud/ 562.5 kBaud	1 Baud – 93.7 kBaud	275 Baud 562.5 kBaud	549 Baud – 562.5 kBaud
	derived from	$f_{OSC}/2$	Timer 1	10-Bit Baudrate Generator		10-Bit Baudrate Generator

Serial Interface 0

Serial Interface 0 can operate in 4 modes:

Mode 0: Shift register mode:
Serial data enters and exits through R × D0. T × D0 outputs the shift clock 8 data bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 8-bit UART, variable baud rate:
10-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB80 in special function register S0CON. The baud rate is variable.

Mode 2: 9-bit UART, fixed baud rate:
11-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On transmission, the 9th data bit (TB80 in S0CON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB80 or a second stop bit by setting TB80 to 1. On reception the 9th data bit goes into RB80 in special function register S0CON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 9-bit UART, variable baud rate:
11-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). In fact, mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable.

Variable Baud Rates for Serial Interface 0

Variable baud rates for modes 1 and 3 of serial interface 0 can be derived from either timer 1 or a dedicated Baudrate Generator.

The baud rate is generated by a free running 10-bit timer with programmable reload register.

$$\text{Mode 1.3 baud rate} = \frac{2^{SMOD} * f_{OSC}}{64*(2^{10}\text{-S0REL})}$$

The default value after reset in the reload registers S0RELL and S0RELH provide a baud rate of 4.8 kBaud (SMOD = 0) or 9.6 kBaud (SMOD = 1) at 12 MHz oscillator frequency. This guarantees full compatibility to the SAB 80C517.

Serial Interface 1

Serial interface 1 can operate in two asynchronous modes:

Mode A: 9-bit UART, variable baud rate.
11 bits are transmitted (through T × D1) or received (through R × D1):
a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1).
On transmission, the 9th data bit (TB81 in S1CON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB81 or a second stop bit by setting TB81 to 1. On reception the 9th data bit goes into RB81 in special function register S1CON, while the stop bit is ignored.

Mode B: 8-bit UART, variable baud rate.
10 bits are transmitted (through T × D1) or received (through R × D1):
a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB81 in special function register S1CON.

Variable Baud Rates for Serial Interface 1.

Variable baud rates for modes A and B of serial interface 1 are derived from a dedicated baud rate generator.

The baud rate clock (baud rate = $\frac{\text{baud rate clock}}{16}$) is generated by an 10-bit free running timer with programmable reload register.

Mode A, B baudrate = $\frac{f_{OSC}}{32 * (2^{10} - \text{SREL})}$

Watchdog Units

The SAB 80C517A offers two enhanced fail safe mechanisms, which allow an automatic recovery from hardware failure or software upset:

– programmable watchdog timer (WDT), variable from 512 µs up to appr. 1.1 s time-out period @12 MHz. Upward compatible to SAB 80515 watchdog.

– oscillator watchdog (OWD), monitors the on-chip oscillator and forces the micro-controller into reset state, in case the on-chip oscillator fails, controls the restart from the Hardware Power Down Mode and provides clock for a fast internal reset after power-on.

Programmable Watchdog Timer

The WDT can be activated by hardware or software.

Hardware initialization is done when pin $\overline{PE}$/SWD (Pin 4) is held high during RESET. The SAB 80C517A then starts program execution with the WDT running. Since Pin $\overline{PE}$/SWD is only sampled during Reset (and hardware power down at parts with stepping code AD and later) dynamical switching of the WDT is not possible.

Software initialization is done by setting bit SWDT.

A refresh of the watchdog timer is done by setting bits WDT and SWDT consecutively.

A block diagram of the watchdog timer is shown in figure 11.

When a watchdog timer resest occurs, the watchdog timer keeps on running, but a status flag WDTS is set. This flag can also be cleared by software.

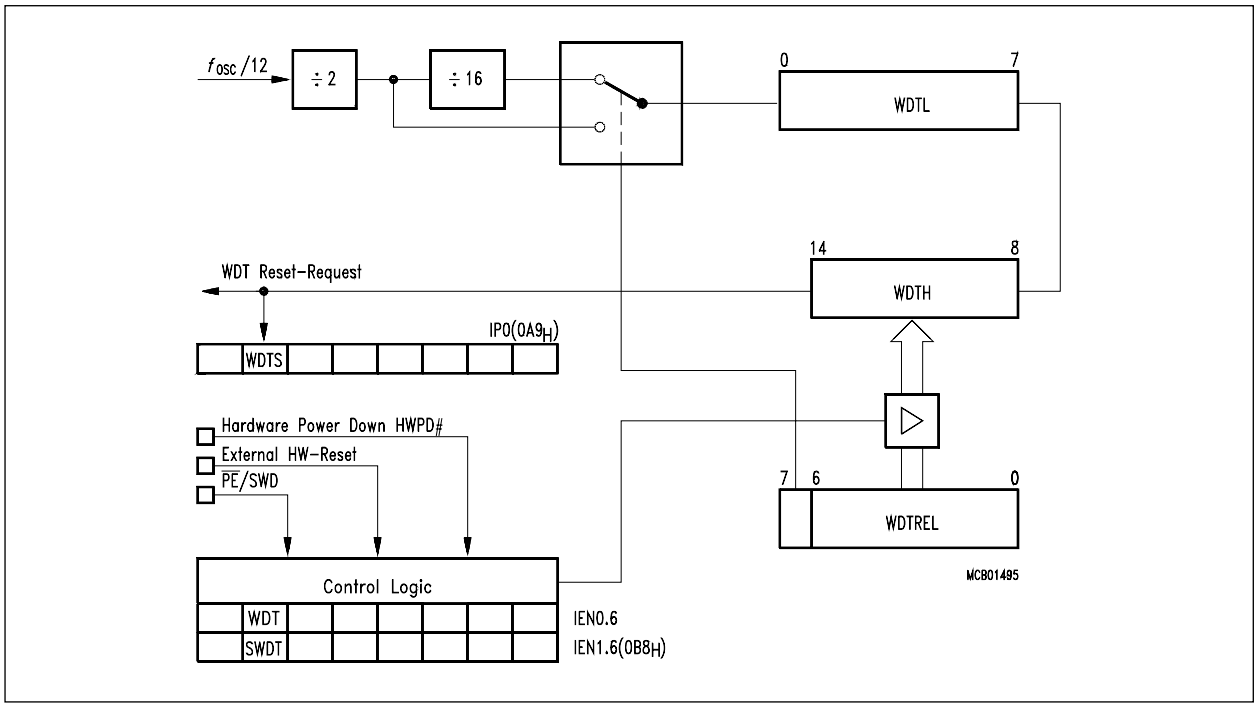


Figure 11
Block Diagram of the Programmable Watchdog Timer

Oscillator Watchdog

The unit serves three functions:

– Monitoring of the on-chip oscillator's function.
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is forced into reset; if the failure condition disappears (i.e. the on-chip oscillator has again a higher frequency than the RC oscillator), the part executes a final reset phase of appr. 0.25 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.

– Restart from the Hardware Power Down Mode.
  If the Hardware Power Down Mode is terminated the oscillator watchdog has to control the correct start-up of the on-chip oscillator and to restart the program. The oscillator watchdog function is only part of the complete Hardware Power Down sequence; however, the watchdog works identically to the monitoring function.

– Fast internal reset after power-on.
  In this function the oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. In this case the oscillator watchdog unit also works identically to the monitoring function.

If the oscillator watchdog unit is to be used it must be enabled (this is done by applying high level to the control pin OWE).

Figure 12 shows the block diagram of the oscillator watchdog unit. It consists of an internal RC oscillator which provides the reference frequency of the on-chip oscillator. The RC oscillator can be enabled/disabled by the control pin OWE. If it is disabled the complete unit has no function.

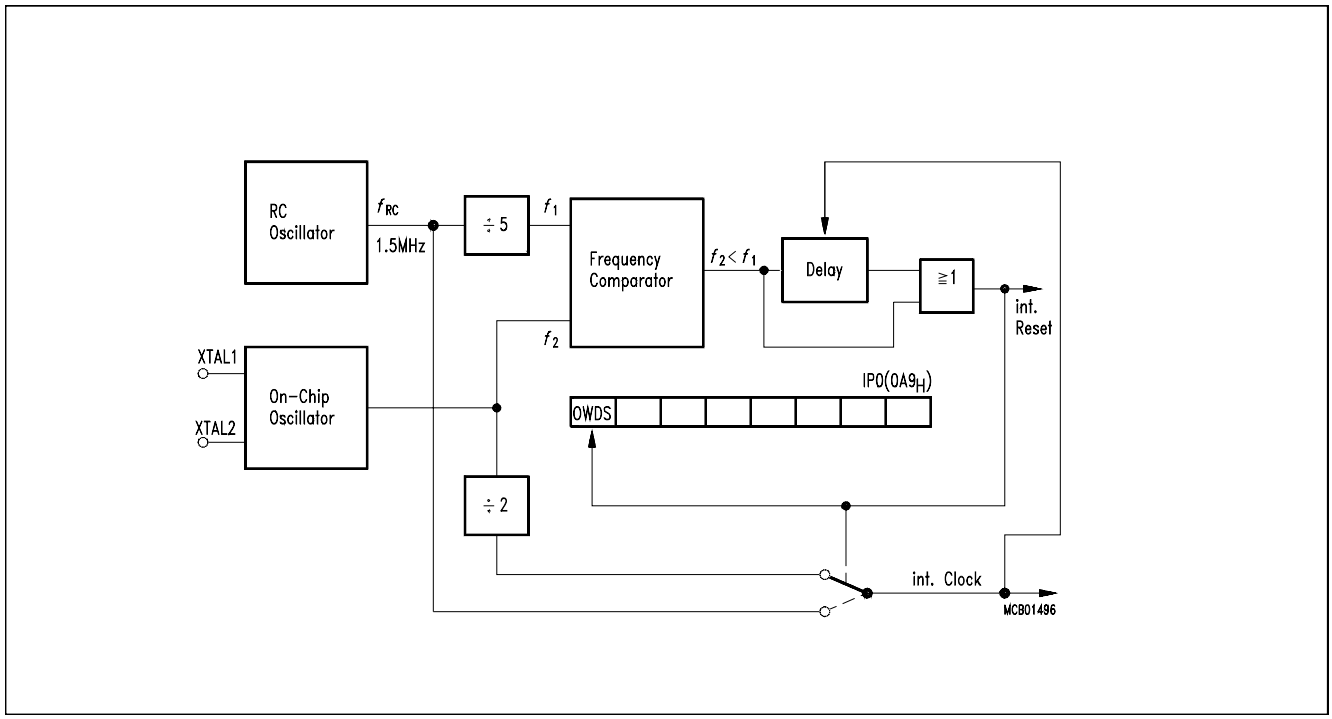


Figure 12
Functional Block Diagram of the Oscillator Watchdog

Fast internal reset after power-on

The SAB 80C517A can use the oscillator watchdog unit for a fast internal reset procedure after power-on.

Normally members of the 8051 family (like the SAB 80C517) enter their default reset state not before the on-chip oscillator starts. The reason is that the external reset signal must be internally synchronized and processed in order to bring the device into the correct reset state. Especially if a crystal is used the start up time of the oscillator is relatively long (typ. 1 ms). During this time period the pins have an undefined state which could have severe effects e.g. to actuators connected to port pins.

In the SAB 80C517A the oscillator watchdog unit avoids this situation. However, the oscillator watchdog must be enabled. In this case, after power-on the oscillator watch-dog's RC oscillator starts working within a very short start-up time (typ. less than 2 micro-seconds). In the following the watchdog circuitry detects a failure condition for the on-chip oscillator because this has not yet started (a failure is always recognized if the watchdog's RC oscillator runs faster than the on-chip oscillator). As long as this condition is valid the watchdog uses the RC oscillator output as clock source for the chip rather than the on-chip oscillator's output.This allows correct resetting of the part and brings also all ports to the defined state.

Delay time between power-on and correct reset state:

Typ.: 18 µs
Max.: 34 µs

Instruction Set

The SAB 80C517A / 83C517A-5 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-H6497-X-X-7600

Absolute Maximum Ratings

Ambient temperature under bias ..... – 40 to 110° C
Storage temperature ..... – 65 to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... – 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 to V_{CC} +0.5 V
Input current on any pin during overload condition ..... – 10mA to +10mA
Absolute sum of all input currents during overload condition ..... |100mA|
Power dissipation ..... 1 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions (V_{IN} > V_{CC} or V_{IN} < V_{SS}) theVoltage on V_{CC} pins with respect to ground (V_{SS}) must not exeed the values definded by the absolute maximum ratings.*

DC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
T_A = 0 to 70 °C for the SAB 80C517A/83C517A-5
T_A = – 40 to 85 °C for the SAB 80C517A-T3/83C517A-5-T3
T_A = – 40 to 110 °C for the SAB 80C517A-T4/83C517A-5-T4

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, $\overline{RESET}$, $\overline{HWPD}$)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage ($\overline{HWPD}$, $\overline{RESET}$)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except $\overline{RESET}$, XTAL2 and $\overline{HWPD}$	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to $\overline{RESET}$ and $\overline{HWPD}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Output low voltage (ports 1, 2, 3, 4, 5, 6)	V_{OL}	–	0.45	V	I_{OL}=1.6 mA[1]
Output low voltage (ports ALE, $\overline{PSEN}$, $\overline{RO}$)	V_{OL1}	–	0.45	V	I_{OL}=3.2 mA [1]
Output high voltage (ports 1, 2, 3, 4, 5, 6)	V_{OH}	2.4 0.9 V_{CC}	– –	V V	I_{OH} =–80 µA I_{OH} =–10 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{RO}$)	V_{OH1}	2.4 0.9 V_{CC}	– –	V V	I_{OH} =–800 µA[2] I_{OH} =–80 µA[2]
Logic input low current (ports 1, 2, 3, 4, 5, 6)	I_{IL}	– 10	– 70	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3, 4, 5, 6)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$, ports 7, 8, $\overline{HWPD}$)	I_{LI}	–	± 100	nA	0.45 < V_{IN} < V_{CC}
			± 150	nA	0.45 < V_{IN} < V_{CC} T_A > 100 °C
Input low current to $\overline{RESET}$ for reset	I_{IL2}	– 10	–100	µA	V_{IN} = 0.45 V
Input low current (XTAL2)	I_{IL3}	–	– 15	µA	V_{IN} = 0.45 V
Input low current ($\overline{PE}$/SWD, OWE)	I_{IL4}	–	– 20	µA	V_{IN} = 0.45 V
Pin capacitance	C_{IO}	–	10	pF	f_C= 1 MHz T_A= 25 °C
Power supply current: Active mode, 12 MHz[7] Active mode, 18 MHz[7] Idle mode, 12 MHz[7] Idle mode, 18 MHz[7] Slow down mode, 12 MHz Slow down mode, 18 MHz Power Down Mode	 I_{CC} I_{CC} I_{CC} I_{CC} I_{CC} I_{CC} I_{PD}	 – – – – – – –	 28 37 24 31 12 16 50	 mA mA mA mA mA mA µA	 V_{CC} = 5 V,[4] V_{CC} = 5 V,[4] V_{CC} = 5 V,[5] V_{CC} = 5 V,[5] V_{CC} = 5 V,[6] V_{CC} = 5 V,[6] V_{CC} = 2...5.5 V, [3]

Notes see page 61.

Notes for page 62:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4, 5 and 6. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (Power down mode) is measured with:
$\overline{EA}$ = $\overline{RESET}$ = $V_{CC;}$ Port0 = Port7 = Port8 = V_{CC}; XTAL1 = N.C.; XTAL2 = V_{SS};
$\overline{PE}$/SWD = OWE = V_{SS};$\overline{HWDP}$ = V_{CC} (Software Power Down mode); V_{ARef} = V_{CC};
V_{AGND} = V_{SS}; all other pins are disconnected. Hardware Powerdown I_{PD} : OWE =V_{CC} or V_{SS}. No certain pin connection for the other pins.

4) I_{CC} (active mode) is measured with:
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL1 = N.C.;
$\overline{EA}$ = $\overline{PE}$/SWD = V_{CC}; Port0 = Port7 = Port8 = V_{CC}; $\overline{HWPD}$ = V_{CC}; $\overline{RESET}$ = V_{SS}
all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V;
XTAL1 = N.C.; $\overline{RESET}$ = V_{CC}; $\overline{HWPD}$ = V_{CC}; Port0 = Port7 = Port8 =V_{CC} ;
$\overline{EA}$ = $\overline{PE}$/SWD = V_{SS}; all other pins are disconnected;

6) I_{CC} (slow down mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} =V_{CC} – 0.5 V;
XTAL1 = N.C.;$\overline{RESET}$= V_{CC}; $\overline{HWPD}$ = V_{CC}; Port7 = Port8 = V_{CC}; $\overline{EA}$ = $\overline{PE}$/SWD = V_{SS} ;
all other pins are disconnected;

7) $I_{CC\,Max}$ at other frequencies is given by:
active mode: I_{CC} (max) = 1.50* f_{OSC} + 10
idle mode: I_{CC} (max) = 1.17* f_{OSC} + 10
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

A/D Converter Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
V_{AREF} = V_{CC} ± 5%; V_{AGND} = V_{SS} ± 0.2 V;
T_A = 0 to 70 °C for the SAB 80C517A/83C517A-5
T_A = – 40 to 85 ° C for the SAB 80C517A-T3/83C517A-5-T3
T_A = – 40 to 110 °C for the SAB 80C517A-T4/83C517A-5-T4

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Analog input capacitance	C_I		25	70	pF	
Sample time (inc. load time)	T_S			4 t_{CY} [1]	µs	[2]
Conversion time (inc. sample time)	T_C			14 t_{CY} [1]	µs	[3]
Total unadjusted error	TUE			± 2	LSB	V_{AREF} = V_{CC} V_{AGND} = V_{SS}
V_{AREF} supply current	I_{REF}		± 20		µA	[4]

1) t_{CY} = (8*2^{ADCL}) /f_{OSC}; (t_{CY} = 1/f_{ADC}; f_{ADC} = f_{OSC}/(8*2^{ADCL}))
2) This parameter specifies the time during the input capacitance C_I, can be charged/discharged by the external source. It must be guaranteed, that the input capacitance C_I, is fully loaded within this time. 4TCY is 2 µs at the f_{OSC}= 16 MHz. After the end of the sample time T_S, changes of the analog input voltage have no effect on the conversion result.
3) This parameter includes the sample time T_S. 14TCY is 7 µs at f_{OSC} = 16 MHz.
4) The differencial impedance r_D of the analog reference source must be less than 1 KΩ at reference supply voltage.

AC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB 80C517A/83C517A-5
T_A = – 40 to 85 °C for the SAB 80C517A-T3/83C517A-5-T3
T_A = – 40 to110 ° C for the SAB 80C517A-T4/83C517A-5-T4

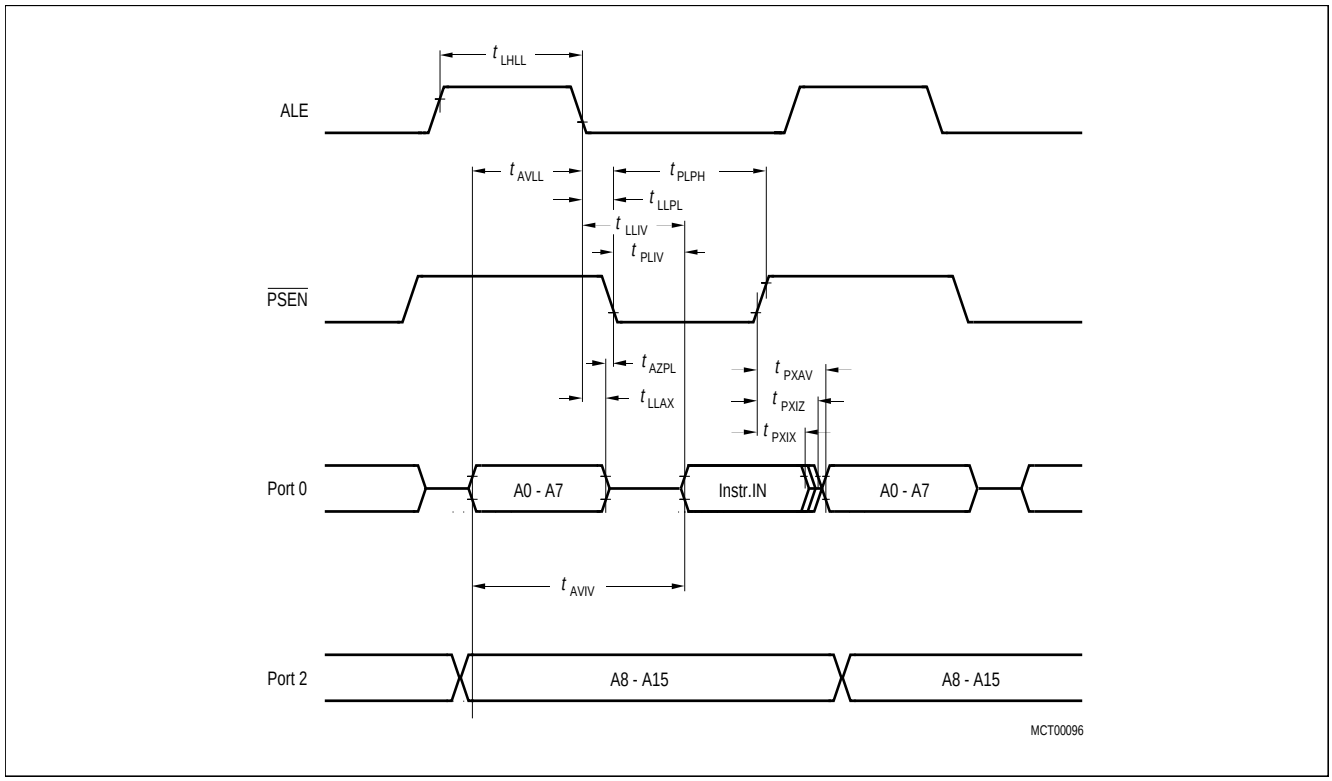
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Parameter	Symbol	Limit Values				Unit
		18 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	71	–	2 t_{CLCL} – 40	–	ns
Address setup to ALE	t_{AVLL}	26	–	t_{CLCL} – 30	–	ns
Address hold after ALE	t_{LLAX}	26	–	t_{CLCL} – 30	–	ns
ALE to valid instruction	t_{LLIV}	–	122	–	4t_{CLCL} – 100	ns
ALE to $\overline{PSEN}$	t_{LLPL}	31	–	t_{CLCL} – 25	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	132	–	3 t_{CLCL} – 35	–	ns
$\overline{PSEN}$ to valid instruction	t_{PLIV}	–	92	–	3t_{CLCL} – 75	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0		ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}	–	46	–	t_{CLCL} – 10	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	48	–	t_{CLCL} – 8	–	ns
Address to valid instr in	t_{AVIV}	–	218	–	5t_{CLCL} – 60	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

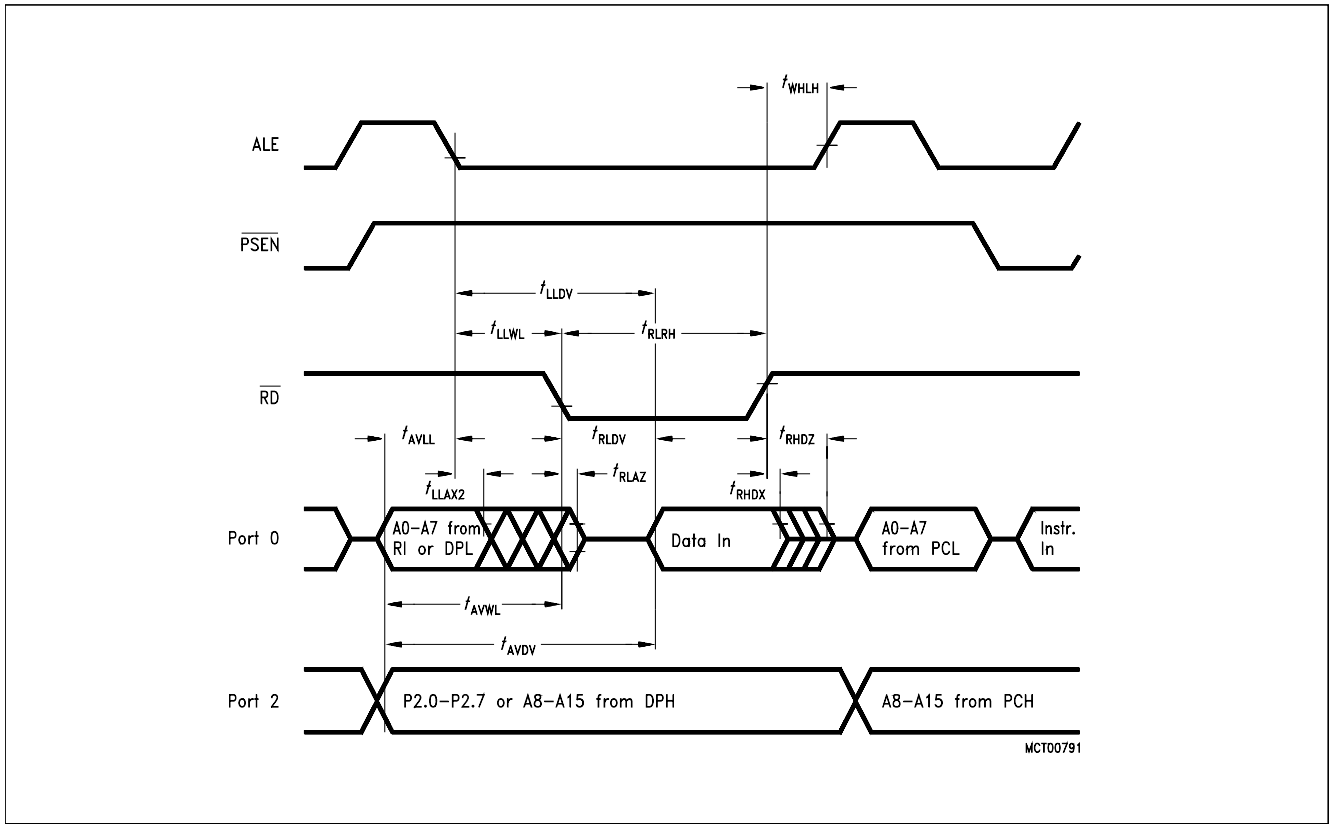
*) Interfacing the SAB 80C517A to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

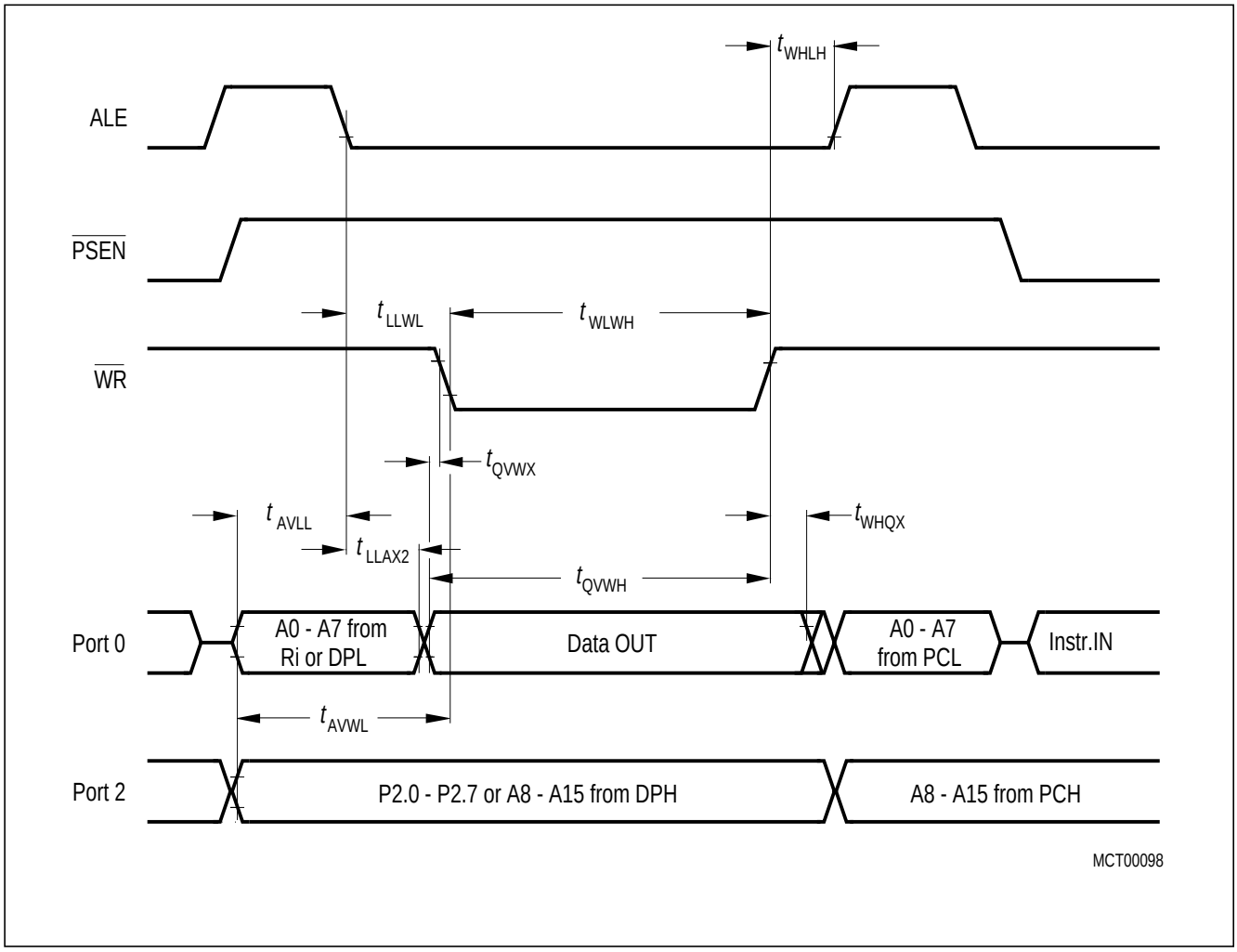
Parameter	Symbol	Limit Values				Unit
		18 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min.	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	233	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	233	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	81	–	2 t_{CLCL} – 30	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	128	–	5 t_{CLCL} – 150	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	51	–	2 t_{CLCL} – 60	ns
ALE to valid data in	t_{LLDV}	–	294	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	335	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	117	217	3 t_{CLCL} – 50	3 t_{CLCL} +50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	16	96	t_{CLCL} – 40	t_{CLCL} +40	ns
Address valid to $\overline{WR}$	t_{AVWL}	92	–	4 t_{CLCL} – 130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	11	–	t_{CLCL} – 45	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	239	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	16	–	t_{CLCL} – 40	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns



Program Memory Read Cycle



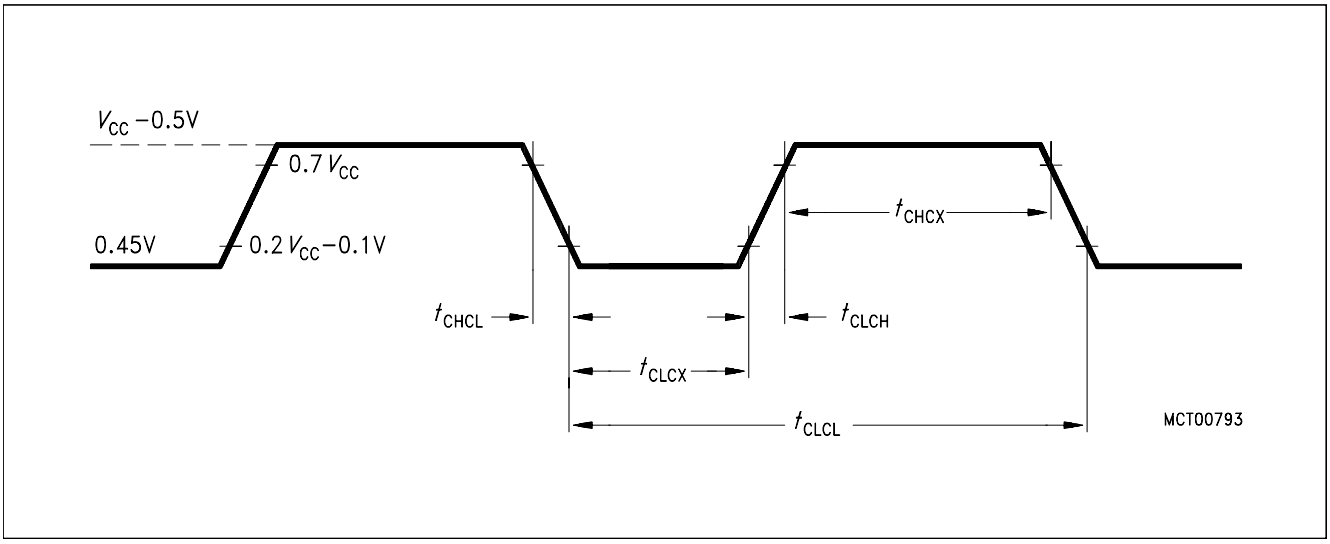
Data Memory Read Cycle



Data Memory Write Cycle

AC Characteristics (cont'd)

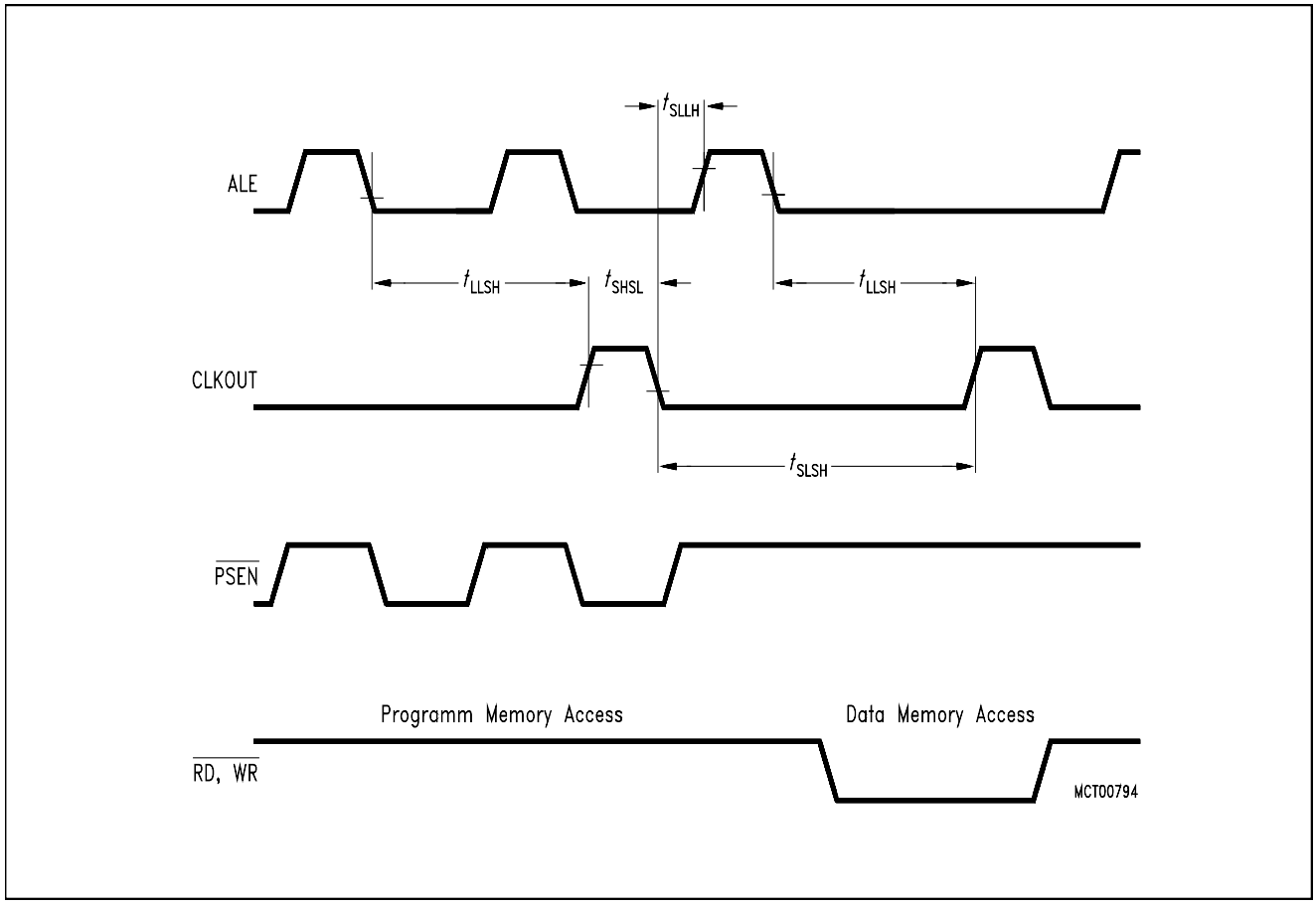
Parameter	Symbol	Limit Values		Unit
		Variable clock Frequ. = 3.5 MHz to 18 MHz		
		min.	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	55.6	285	ns
High time	t_{CHCX}	20	t_{CLCL}-t_{CHCX}	ns
Low time	t_{CLCX}	20	t_{CLCL}-t_{CHCX}	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns
Oscillator frequency	$1/t_{CLC}$	3.5	18	MHz



External Clock Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit Values				Unit
		18 MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	349	–	7 t_{CLCL} – 40	–	ns
CLKOUT high time	t_{SHSL}	71	–	2 t_{CLCL} – 40	–	ns
CLKOUT low time	t_{SLSH}	516	–	10 t_{CLCL} – 40	–	ns
CLKOUT low to ALE high	t_{SLLH}	16	96	t_{CLCL} – 40	t_{CLCL} +40	ns



System Clock Timing

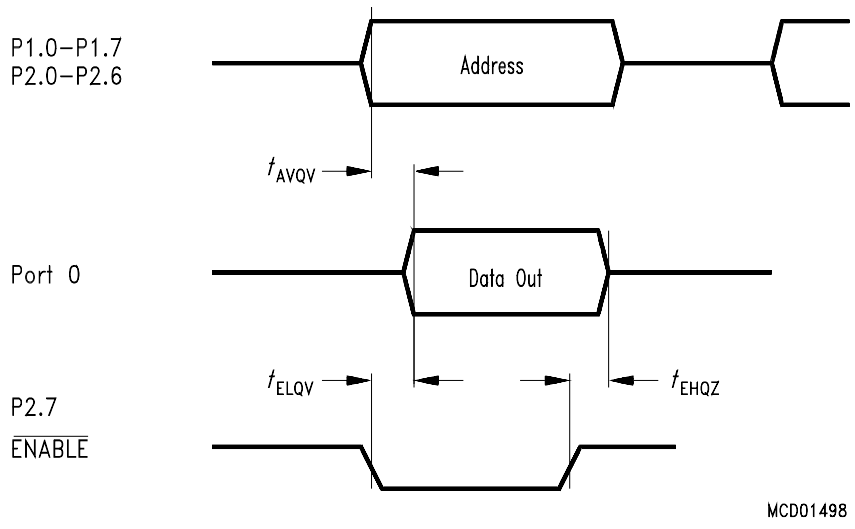
ROM Verification Characteristics

T_A = 25°C ± 5°C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	

ROM Verification Mode 1 (Standard Verify Mode for not Read Protected ROM)

Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after ENABLE	t_{EHOZ}	0	48 t_{CLCL}	ns
Oscillator frequency	1/t_{CLCL}	4	6	MHz

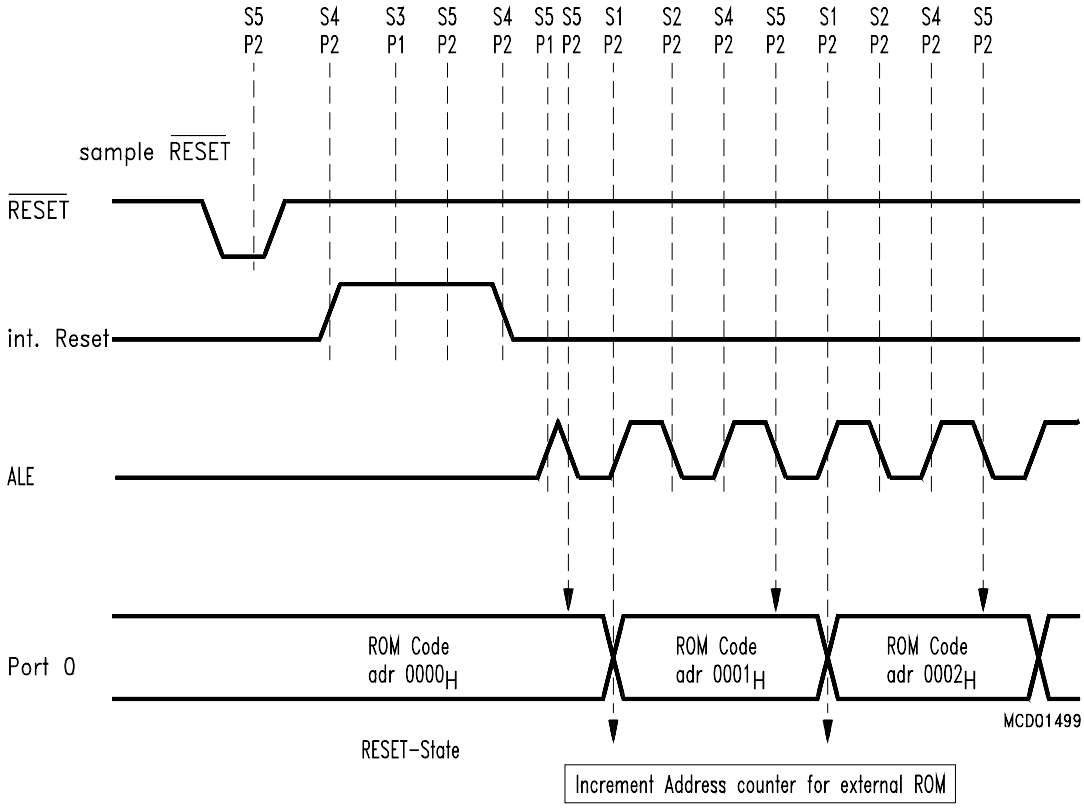


Address: P1.0–P1.7=A0–A7
P2.0–P2.6=A8–A14
Data: P0.0–0.7=D0–D7

Inputs $\overline{PSEN}$ = V_{SS}
ALE,$\overline{EA}$ = V_{IH}
$\overline{RESET}$ = V_{IL}

ROM Verification Mode 1

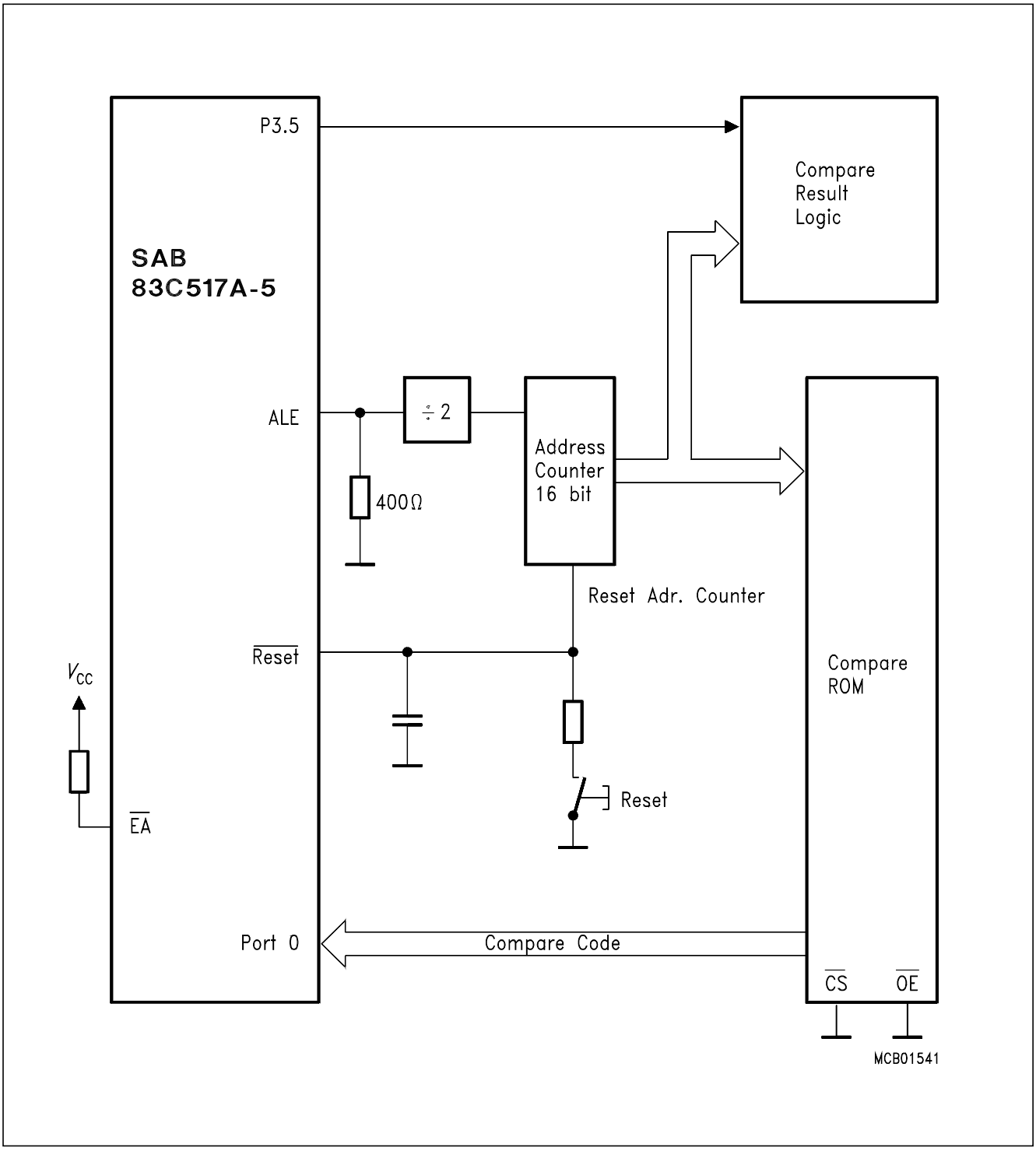
ROM Verification Mode 2 (New Verify Mode for Protected and not Protected ROM)



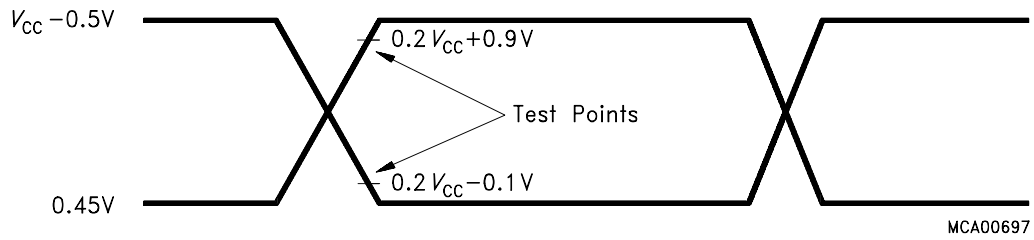
Inputs $\overline{EA}= V_{IH}$
ALE forced to low level by a weak pull down resistor (approx.400Ω),
during RESET activ ROM-Code: Port 0=D0-D7

Outputs Port 3.5 shows all 1024 cycles low level for one cycle
when compared ROM-Code was not alright

ROM Verification Mode 2

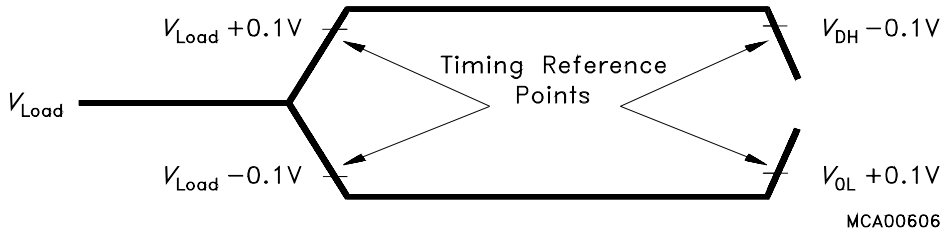


Application Circuitry for Verifying the Internal ROM



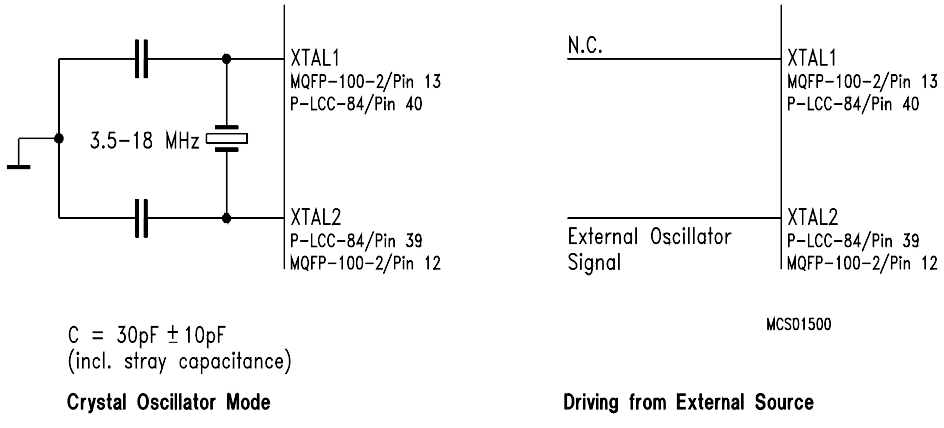
AC Inputs during testing are driven at V_{CC} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Input, Output Waveforms



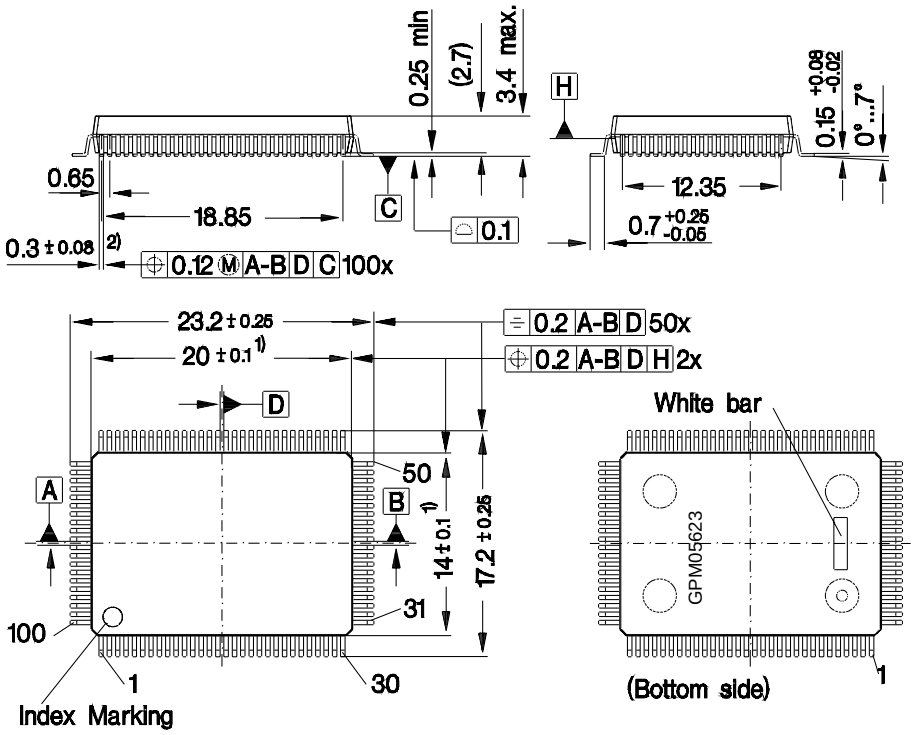
For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

AC Testing: Float Waveforms



Recommended Oscillator Circuits

Plastic Package, P-MQFP-100-2 (SMD)
(Plastic Metric Quad Flat Package)



2) Does not include dambar protrusion of 0.08 max. per side
1) Does not include plastic or metal protrusion of 0.25 max. per side

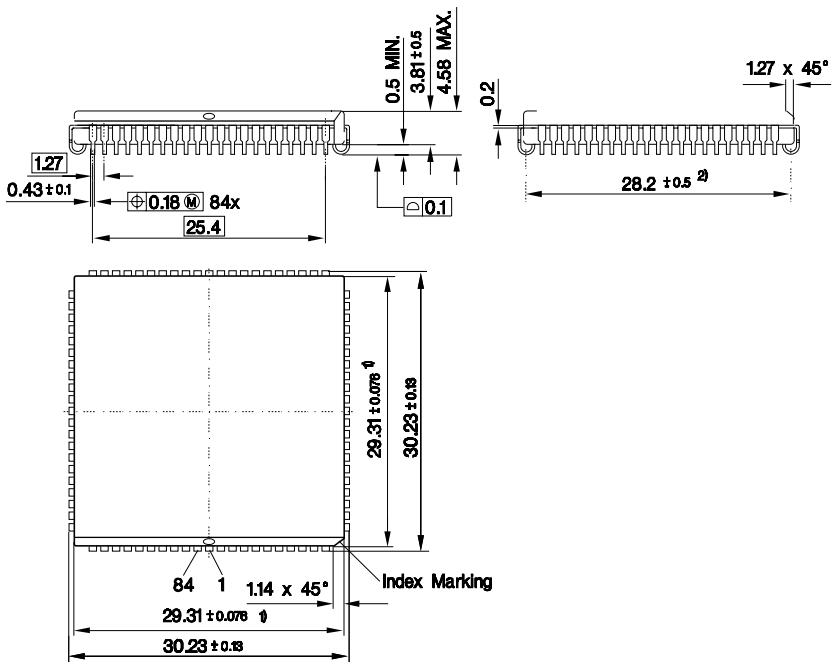
Figure 1
P-MQFP-100-2 Package Outlines

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-LCC-84-2 (SMD)
(Plastic Leaded Chip Carrier)



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Dimension from center to center

Figure 2
P-LCC-84-2 Package Outlines

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm