

Low Quiescent Current, Programmable-Delay Supervisory Circuit

FEATURES

- Power-On Reset Generator with Adjustable Delay Time: 1.25ms to 10s
- Very Low Quiescent Current: 2.4 μ A typ
- High Threshold Accuracy: 0.5% typ
- Fixed Threshold Voltages for Standard Voltage Rails from 0.9V to 5V and Adjustable Voltage Down to 0.4V Are Available
- Manual Reset (MR) Input
- Open-Drain RESET Output
- Temperature Range: –40°C to +125°C
- Small SOT23 and 2mm × 2mm QFN Packages

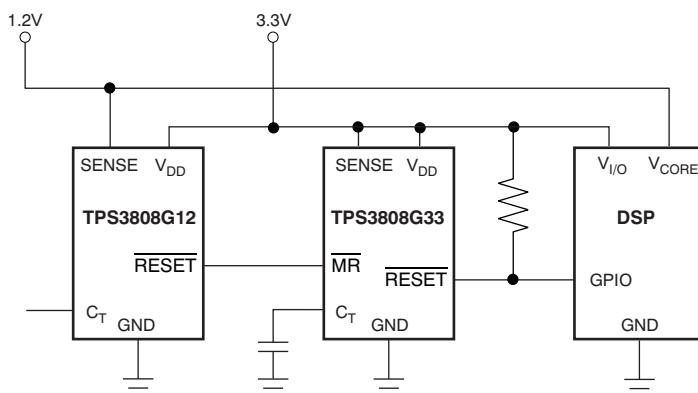
APPLICATIONS

- DSP or Microcontroller Applications
- Notebook/Desktop Computers
- PDAs/Hand-Held Products
- Portable/Battery-Powered Products
- FPGA/ASIC Applications

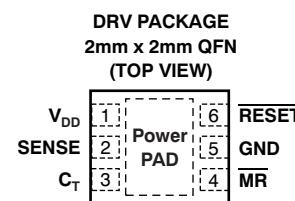
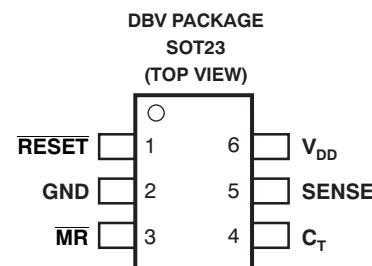
DESCRIPTION

The TPS3808xxx family of microprocessor supervisory circuits monitor system voltages from 0.4V to 5.0V, asserting an open-drain RESET signal when the SENSE voltage drops below a preset threshold or when the manual reset (MR) pin drops to a logic low. The RESET output remains low for the user-adjustable delay time after the SENSE voltage and manual reset (MR) return above the respective thresholds.

The TPS3808 uses a precision reference to achieve 0.5% threshold accuracy for $V_{IT} \leq 3.3V$. The reset delay time can be set to 20ms by disconnecting the C_T pin, 300ms by connecting the C_T pin to V_{DD} using a resistor, or can be user-adjusted between 1.25ms and 10s by connecting the C_T pin to an external capacitor. The TPS3808 has a very low typical quiescent current of 2.4 μ A so it is well-suited to battery-powered applications. It is available in a small SOT23 and an ultra-small 2mm × 2mm QFN PowerPAD™ package, and is fully specified over a temperature range of –40°C to +125°C (T_J).



Typical Application Circuit



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	NOMINAL SUPPLY VOLTAGE ⁽²⁾	THRESHOLD VOLTAGE (V _{IT})
TPS3808G01	Adjustable	0.405V
TPS3808G09	0.9V	0.84V
TPS3808G12	1.2V	1.12V
TPS3808G125	1.25V	1.16V
TPS3808G15	1.5V	1.40V
TPS3808G18	1.8V	1.67V
TPS3808G19	1.9V	1.77V
TPS3808G25	2.5V	2.33V
TPS3808G30	3.0V	2.79V
TPS3808G33	3.3V	3.07V
TPS3808G50	5.0V	4.65V

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Custom threshold voltages from 0.82V to 3.3V, 4.4V to 5.0V are available through the use of factory EEPROM programming. Minimum order quantities apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating junction temperature range, unless otherwise noted.

	TPS3808	UNIT
Input voltage range, V _{DD}	−0.3 to 7.0	V
C _T voltage range, V _{CT}	−0.3 to V _{DD} + 0.3	V
Other voltage ranges: V _{RESET} , V _{MR} , V _{SENSE}	−0.3 to 7	V
RESET pin current	5	mA
Operating junction temperature range, T _J ⁽²⁾	−40 to +150	°C
Storage temperature range, T _{STG}	−65 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the [Electrical Characteristics](#) is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) As a result of the low dissipated power in this device, it is assumed that T_J = T_A.

ELECTRICAL CHARACTERISTICS

$1.7V \leq V_{DD} \leq 6.5V$, $R_{LRESET} = 100k\Omega$, $C_{LRESET} = 50pF$, over operating temperature range ($T_J = -40^{\circ}C$ to $+125^{\circ}C$), unless otherwise noted. Typical values are at $T_J = +25^{\circ}C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{DD}	Input supply range	$-40^{\circ}C < T_J < +125^{\circ}C$	1.7	6.5		V	
		$0^{\circ}C < T_J < +85^{\circ}C$	1.65	6.5			
I_{DD}	Supply current (current into V_{DD} pin)	$V_{DD} = 3.3V$, \overline{RESET} not asserted MR, \overline{RESET} , C_T open		2.4	5.0	μA	
		$V_{DD} = 6.5V$, \overline{RESET} not asserted MR, \overline{RESET} , C_T open		2.7	6.0	μA	
V_{OL}	Low-level output voltage	$1.3V \leq V_{DD} < 1.8V$, $I_{OL} = 0.4mA$		0.3		V	
		$1.8V \leq V_{DD} \leq 6.5V$, $I_{OL} = 1.0mA$		0.4		V	
Power-up reset voltage ⁽¹⁾		V_{OL} (max) = 0.2V, $I_{RESET} = 15\mu A$		0.8		V	
V_{IT}	Negative-going input threshold accuracy	TPS3808G01		-2.0	± 1.0	+2.0	
		$V_{IT} \leq 3.3V$		-1.5	± 0.5	+1.5	
		$3.3V < V_{IT} \leq 5.0V$		-2.0	± 1.0	+2.0	
		$V_{IT} \leq 3.3V$	$-40^{\circ}C < T_J < +85^{\circ}C$	-1.25	± 0.5	+1.25	
		$3.3V < V_{IT} \leq 5.0V$	$-40^{\circ}C < T_J < +85^{\circ}C$	-1.5	± 0.5	+1.5	
V_{HYS}	Hysteresis on V_{IT} pin	TPS3808G01		1.5	3.0		
		Fixed versions	$-40^{\circ}C < T_J < +85^{\circ}C$	1.0	2.0	$\%V_{IT}$	
				1.0	2.5		
R_{MR}	\overline{MR} Internal pull-up resistance		70	90		$k\Omega$	
I_{SENSE}	Input current at SENSE pin	TPS3808G01	$V_{SENSE} = V_{IT}$	-25	25	nA	
		Fixed versions	$V_{SENSE} = 6.5V$		1.7	μA	
I_{OH}	\overline{RESET} leakage current		$V_{RESET} = 6.5V$, \overline{RESET} not asserted		300	nA	
C_{IN}	Input capacitance, any pin	C_T pin	$V_{IN} = 0V$ to V_{DD}		5	pF	
		Other pins	$V_{IN} = 0V$ to $6.5V$		5		
V_{IL}	\overline{MR} logic low input			0	$0.3 V_{DD}$	V	
V_{IH}	\overline{MR} logic high input			$0.7 V_{DD}$	V_{DD}		
t_w	Input pulse width to \overline{RESET}	SENSE	$V_{IH} = 1.05V_{IT}$, $V_{IL} = 0.95V_{IT}$		20	μs	
		MR	$V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$		0.001		
t_d	\overline{RESET} delay time	$C_T = \text{Open}$	See Timing Diagram	12	20	28	ms
		$C_T = V_{DD}$		180	300	420	ms
		$C_T = 100pF$		0.75	1.25	1.75	ms
		$C_T = 180nF$		0.7	1.2	1.7	s
t_{pHL}	Propagation delay	\overline{MR} to \overline{RESET}	$V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$		150		ns
	High to low level \overline{RESET} delay	SENSE to \overline{RESET}	$V_{IH} = 1.05V_{IT}$, $V_{IL} = 0.95V_{IT}$		20		μs
θ_{JA}	Thermal resistance, junction-to-ambient				290		$^{\circ}C/W$

(1) The lowest supply voltage (V_{DD}) at which \overline{RESET} becomes active. $T_{rise(VDD)} \geq 15\mu s/V$.

FUNCTIONAL BLOCK DIAGRAMS

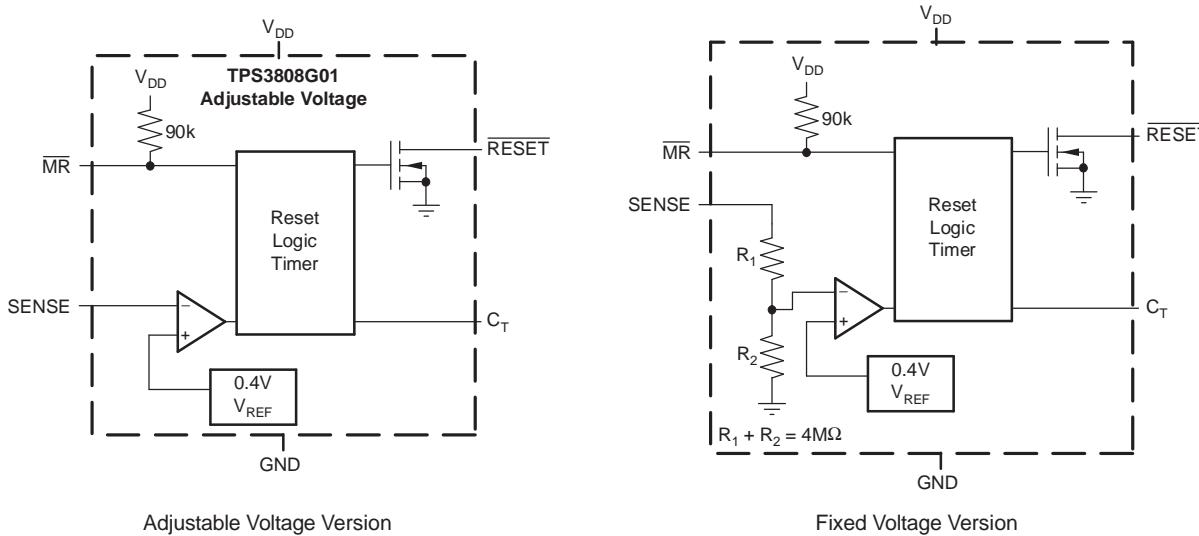


Figure 1. Adjustable and Fixed Voltage Versions

PIN ASSIGNMENTS

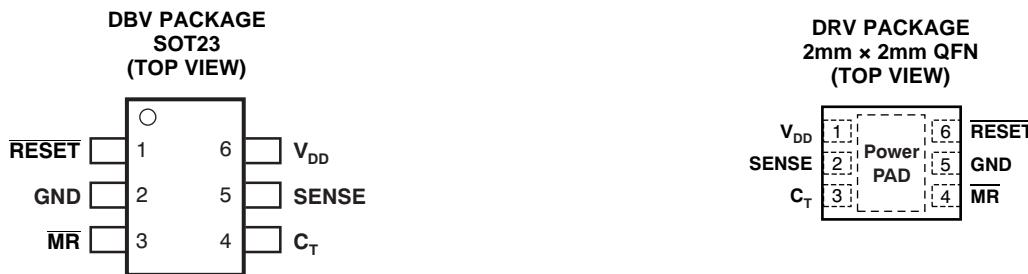


Table 1. TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	SOT23 (DBV) PIN NO.	
RESET	1	RESET is an open-drain output that is driven to a low impedance state when RESET is asserted (either the SENSE input is lower than the threshold voltage (V_{IT}) or the MR pin is set to a logic low). RESET will remain low (asserted) for the reset period after both SENSE is above V_{IT} and MR is set to a logic high. A pull-up resistor from 10kΩ to 1MΩ should be used on this pin, and allows the reset pin to attain voltages higher than V_{DD} .
GND	2	Ground
MR	3	Driving the manual reset pin (MR) low asserts RESET. MR is internally tied to V_{DD} by a 90kΩ pull-up resistor.
CT	4	Reset period programming pin. Connecting this pin to V_{DD} through a 40kΩ to 200kΩ resistor or leaving it open results in fixed delay times (see Electrical Characteristics). Connecting this pin to a ground referenced capacitor $\geq 100\text{pF}$ gives a user-programmable delay time. See the Selecting the Reset Delay Time section for more information.
SENSE	5	This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage V_{IT} , then RESET is asserted.
V_{DD}	6	Supply voltage. It is good analog design practice to place a $0.1\mu\text{F}$ ceramic capacitor close to this pin.
PowerPAD		PowerPAD. Connect to ground plane to enhance thermal performance of package.

TIMING DIAGRAM

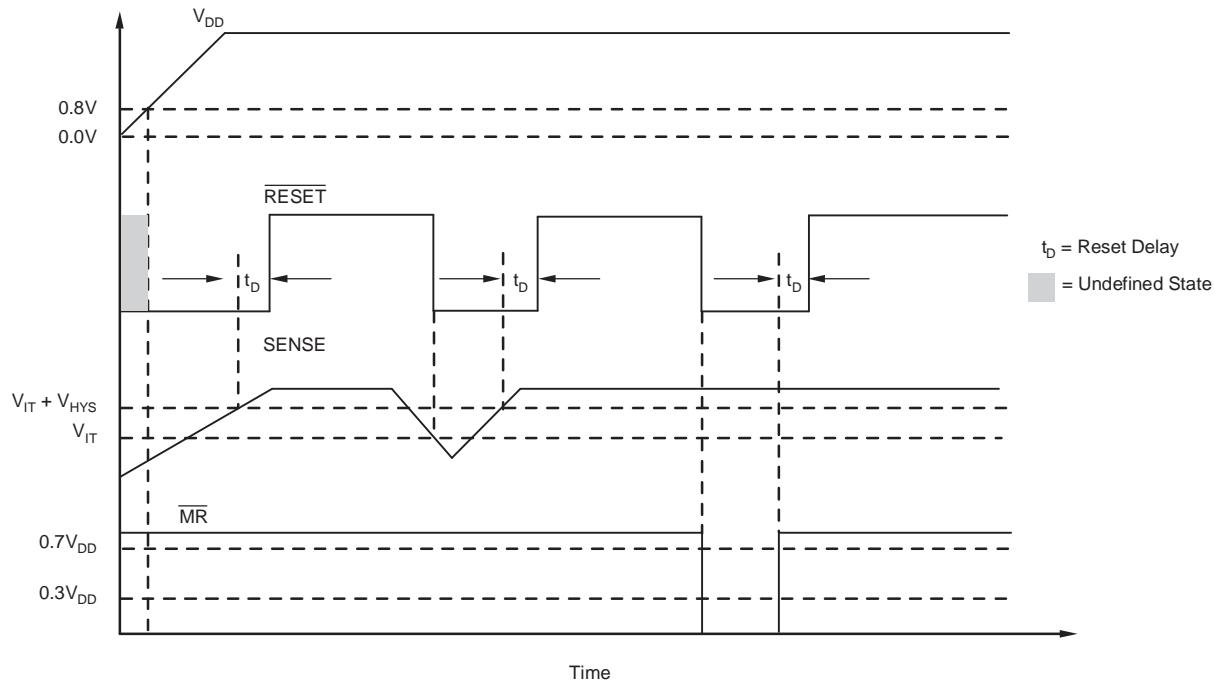


Figure 2. TPS3808 Timing Diagram Showing \overline{MR} and \overline{SENSE} Reset Timing

TRUTH TABLE

\overline{MR}	$\overline{SENSE} > V_{IT}$	\overline{RESET}
L	0	L
L	1	L
H	0	L
H	1	H

TYPICAL CHARACTERISTICS

At $T_J = +25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, $R_{RESET} = 100\text{k}\Omega$, and $C_{RESET} = 50\text{pF}$, unless otherwise noted.

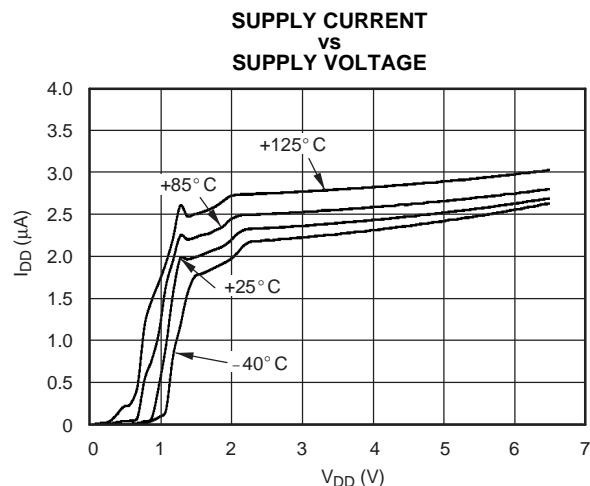


Figure 3.

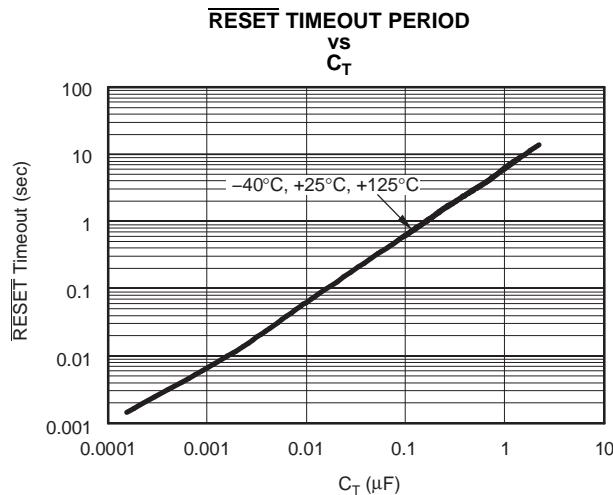


Figure 4.

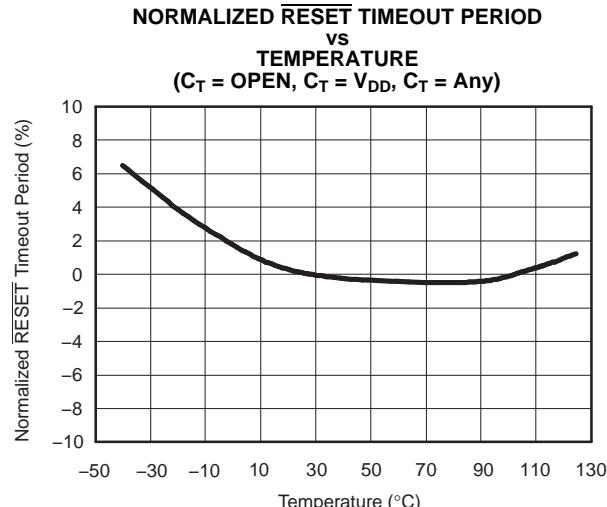


Figure 5.

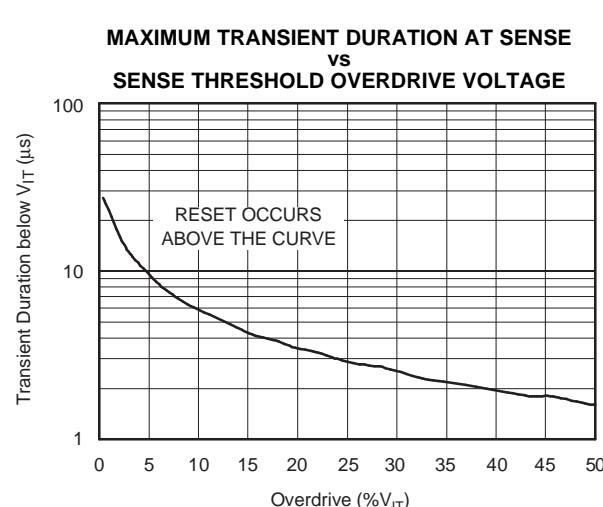


Figure 6.

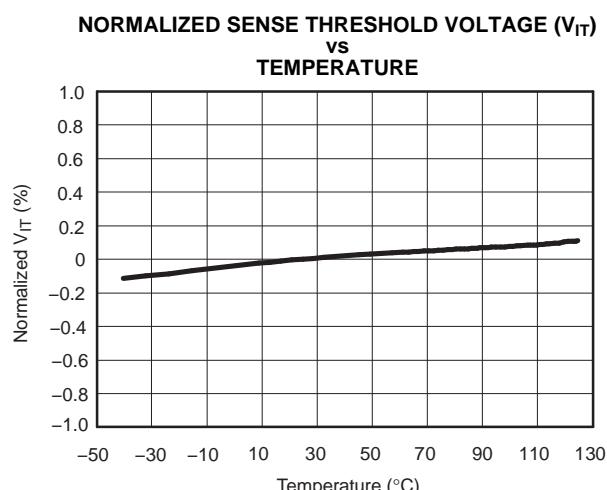


Figure 7.

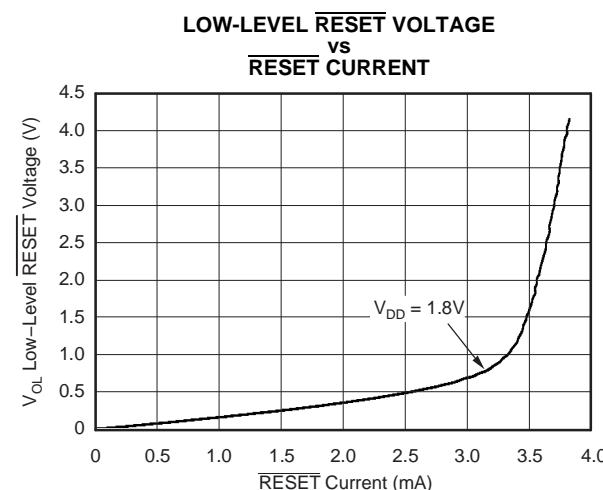


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At $T_J = +25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, $R_{LRESET} = 100\text{k}\Omega$, and $C_{LRESET} = 50\text{pF}$, unless otherwise noted.

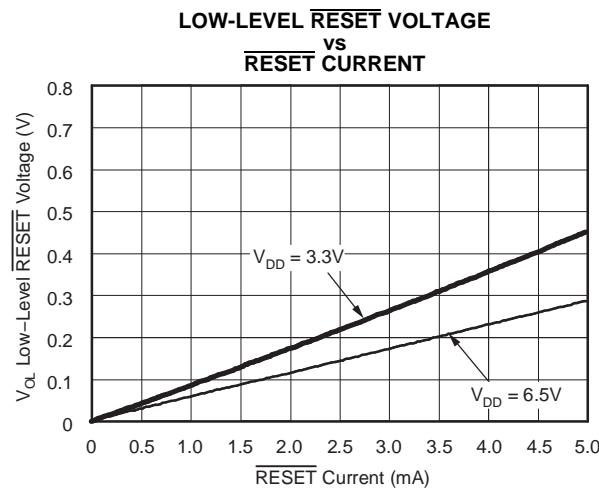


Figure 9.

DEVICE OPERATION

The TPS3808 microprocessor supervisory product family is designed to assert a RESET signal when either the SENSE pin voltage drops below V_{IT} or the manual reset (MR) is driven low. The RESET output remains asserted for a user-adjustable time after both the manual reset (MR) and SENSE voltages return above the respective thresholds. A broad range of voltage threshold and reset delay time adjustments are available, allowing these devices to be used in a wide array of applications. Reset threshold voltages can be factory-set from 0.82V to 3.3V or from 4.4V to 5.0V, while the TPS3808G01 can be set to any voltage above 0.405V using an external resistor divider. Two preset delay times are also user-selectable: connecting the C_T pin to V_{DD} results in a 300ms reset delay, while leaving the C_T pin open yields a 20ms reset delay. In addition, connecting a capacitor between C_T and GND allows the designer to select any reset delay period from 1.25ms to 10s.

RESET OUTPUT

A typical application of the TPS3808G25 used with the OMAP1510 processor is shown in [Figure 10](#). The open-drain RESET output is typically connected to the RESET input of a microprocessor. A pull-up resistor must be used to hold this line high when RESET is not asserted. The RESET output is undefined for voltage below 0.8V, but this is normally not a problem since most microprocessors do not function below this voltage. RESET remains high (unasserted) as long as SENSE is above its threshold (V_{IT}) and the manual reset (MR) is logic high. If either SENSE falls below V_{IT} or MR is driven low, RESET is asserted, driving the RESET pin to a low impedance.

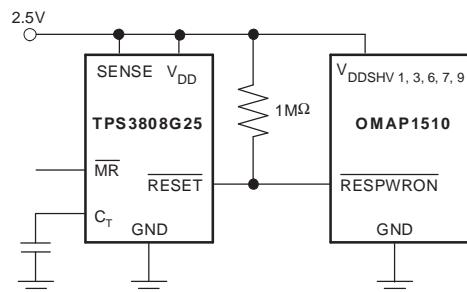


Figure 10. Typical Application of the TPS3808 with an OMAP Processor

Once MR is again logic high and SENSE is above $V_{IT} + V_{HYS}$ (the threshold hysteresis), a delay circuit is enabled which holds RESET low for a specified reset delay period. Once the reset delay has expired, the RESET pin goes to a high impedance state. The pull-up resistor from the open-drain RESET to the

supply line can be used to allow the reset signal for the microprocessor to have a voltage higher than V_{DD} (up to 6.5V). The pull-up resistor should be no smaller than $10k\Omega$ as a result of the finite impedance of the RESET line.

SENSE INPUT

The SENSE input provides a terminal at which any system voltage can be monitored. If the voltage on this pin drops below V_{IT} , then RESET is asserted. The comparator has a built-in hysteresis to ensure smooth RESET assertions and de-assertions. It is good analog design practice to put a $1nF$ to $10nF$ bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics.

The TPS3808G01 can be used to monitor any voltage rail down to 0.405V using the circuit shown in [Figure 11](#).

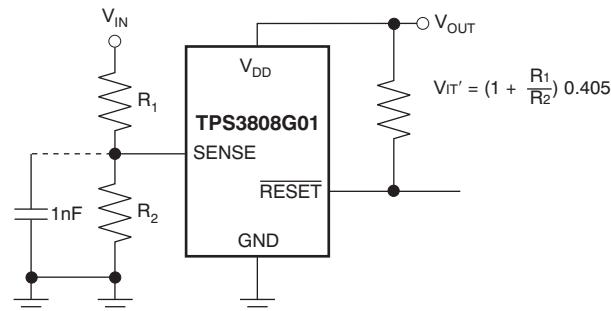


Figure 11. Using the TPS3808G01 to Monitor a User-Defined Threshold Voltage

MANUAL RESET (MR) INPUT

The manual reset (MR) input allows a processor or other logic circuits to initiate a reset. A logic low (0.3V_{DD}) on MR causes RESET to assert. After MR returns to a logic high and SENSE is above its reset threshold, RESET is de-asserted after the user defined reset delay expires. Note that MR is internally tied to V_{DD} using a $90k\Omega$ resistor so this pin can be left unconnected if MR will not be used.

See [Figure 12](#) for how MR can be used to monitor multiple system voltages. Note that if the logic signal driving MR does not go fully to V_{DD} , there will be some additional current draw into V_{DD} as a result of the internal pull-up resistor on MR. To minimize current draw, a logic-level FET can be used as illustrated in [Figure 13](#).

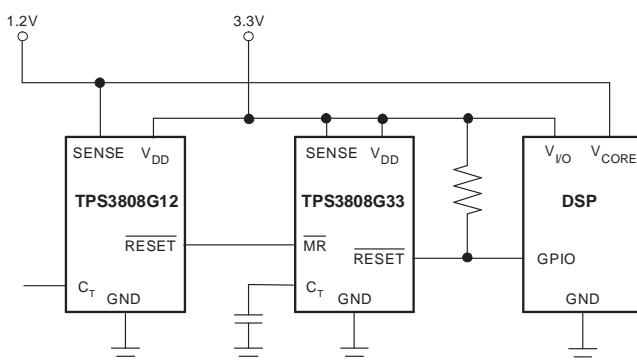


Figure 12. Using MR to Monitor Multiple System Voltages

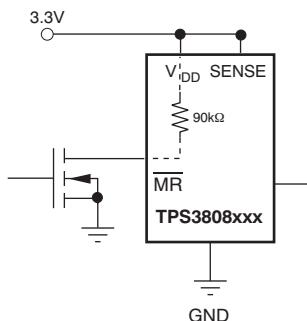


Figure 13. Using an External MOSFET to Minimize I_{DD} When MR Signal Does Not Go to V_{DD}

SELECTING THE RESET DELAY TIME

The TPS3808 has three options for setting the $\overline{\text{RESET}}$ delay time as shown in Figure 14. Figure 14a shows the configuration for a fixed 300ms typical delay time by tying C_T to V_{DD} ; a resistor from 40kΩ to 200kΩ must be used. Supply current is not affected

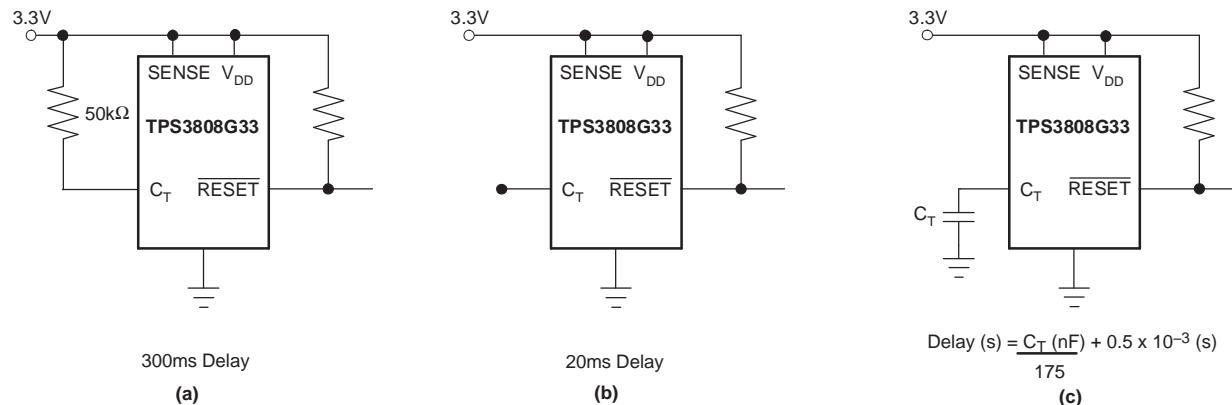


Figure 14. Configuration Used to Set the $\overline{\text{RESET}}$ Delay Time

by the choice of resistor. Figure 14b shows a fixed 20ms delay time by leaving the C_T pin open. Figure 14c shows a ground referenced capacitor connected to C_T for a user-defined program time between 1.25ms and 10s.

The capacitor C_T should be $\geq 100\text{pF}$ nominal value in order for the TPS3808xxx to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using the following equation:

$$C_T (\text{nF}) = [t_D (\text{s}) - 0.5 \times 10^{-3} (\text{s})] \times 175 \quad (1)$$

The reset delay time is determined by the time it takes an on-chip precision 220nA current source to charge the external capacitor to 1.23V. When a $\overline{\text{RESET}}$ is asserted the capacitor is discharged. When the $\overline{\text{RESET}}$ conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.23V, $\overline{\text{RESET}}$ is de-asserted. Note that a low leakage type capacitor such as a ceramic should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

IMMUNITY TO SENSE PIN VOLTAGE TRANSIENTS

The TPS3808 is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients is dependent on threshold overdrive, as shown in the *Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage* graph (Figure 6) in the *Typical Characteristics* section.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TPS3808G01DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G01DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G01DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G01DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G01DRVVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G01DRVVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G01DRVVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G01DRVVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G09DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G09DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G09DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G09DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G125DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G125DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G125DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G125DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G12DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TPS3808G12DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G12DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G12DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G12DRVVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G12DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G12DRVVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G12DRVVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G15DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G15DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G15DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G15DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G15DRVVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G15DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G15DRVVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G15DRVVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G18DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G18DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G18DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TPS3808G18DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G18DRV	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G18DRV	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G19DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G19DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G19DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G19DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G25DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G25DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G25DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G25DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G25DRV	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G25DRV	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G25DRV	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G25DRV	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G30DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G30DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G30DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TPS3808G30DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G30DRV	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G30DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G30DRV	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G30DRV	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G33DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G33DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G33DBV	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G33DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G50DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G50DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G50DBV	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3808G50DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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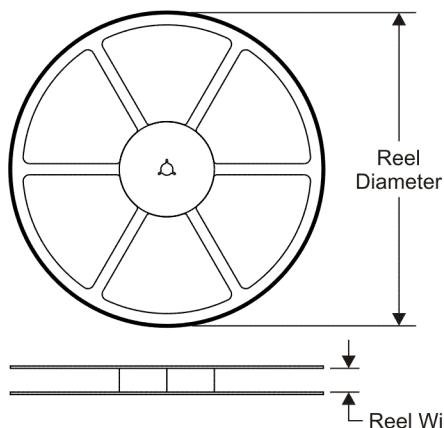
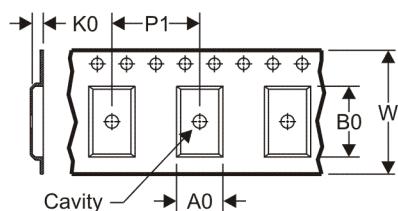
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3808G01, TPS3808G12, TPS3808G125, TPS3808G18, TPS3808G30, TPS3808G33, TPS3808G50 :

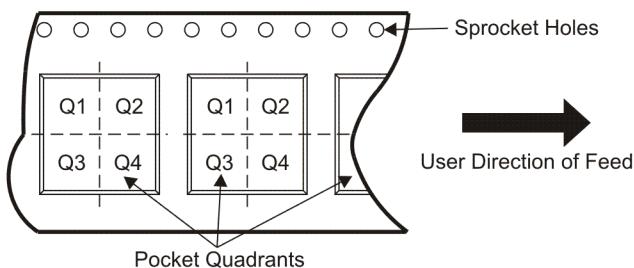
- Automotive: [TPS3808G01-Q1](#), [TPS3808G12-Q1](#), [TPS3808G125-Q1](#), [TPS3808G18-Q1](#), [TPS3808G30-Q1](#), [TPS3808G33-Q1](#), [TPS3808G50-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


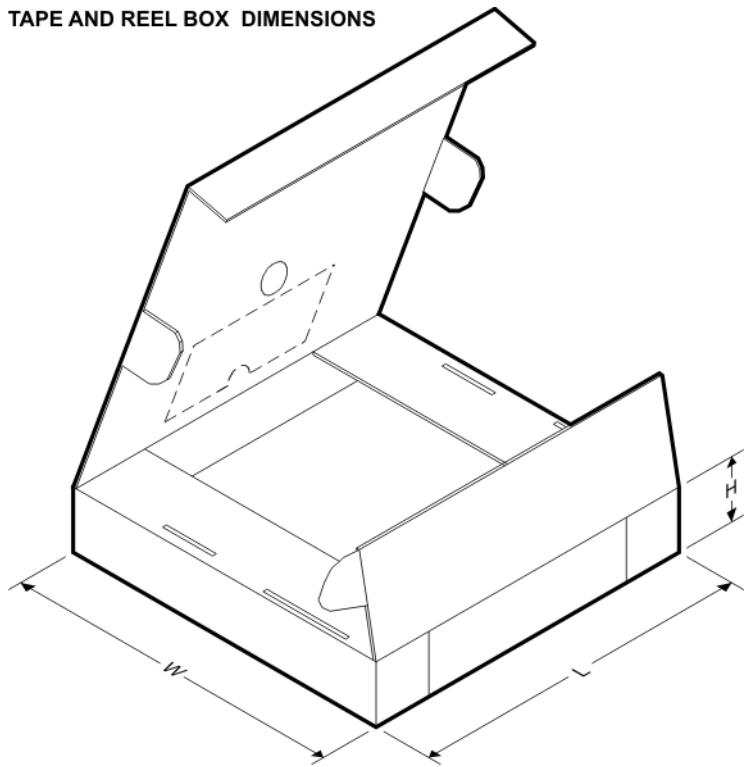
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3808G01DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G01DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G01DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G01DRVVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G01DRVVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G09DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G09DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G125DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G125DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G12DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G12DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G12DRVVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G12DRVVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G15DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G15DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G15DRVVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G15DRVVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G18DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3808G18DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G18DRV	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G18DRV	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G19DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G19DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G25DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G25DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G25DRV	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G25DRV	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G30DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G30DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G30DRV	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G30DRV	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G33DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G33DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G50DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G50DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

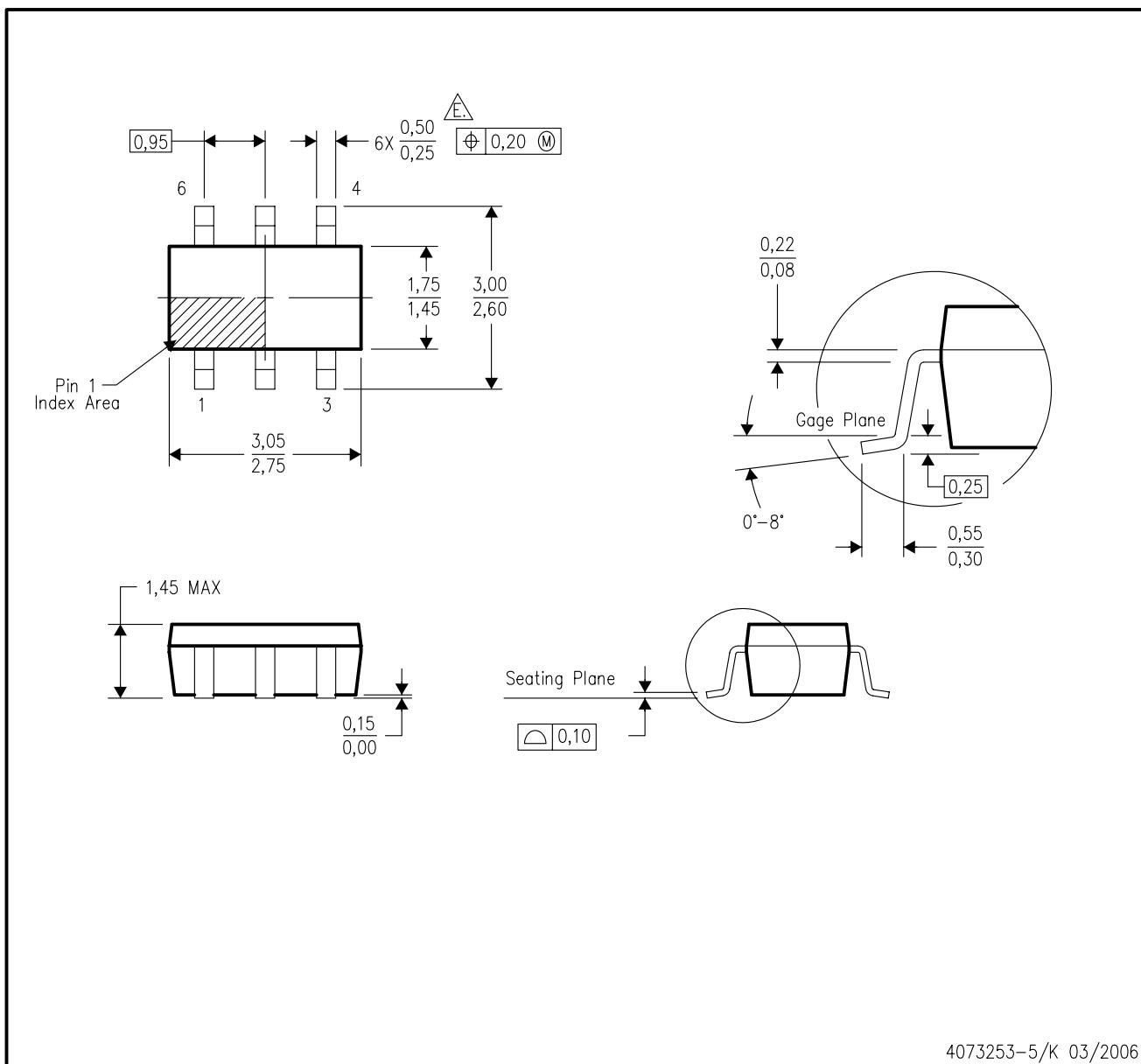
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3808G01DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3808G01DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G01DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3808G01DRVVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS3808G01DRVVT	SON	DRV	6	250	203.0	203.0	35.0
TPS3808G09DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G09DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3808G125DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3808G125DBVT	SOT-23	DBV	6	250	203.0	203.0	35.0
TPS3808G12DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G12DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3808G12DRVVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS3808G12DRVVT	SON	DRV	6	250	203.0	203.0	35.0
TPS3808G15DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3808G15DBVT	SOT-23	DBV	6	250	203.0	203.0	35.0
TPS3808G15DRVVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS3808G15DRVVT	SON	DRV	6	250	203.0	203.0	35.0
TPS3808G18DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G18DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3808G18DRVVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS3808G18DRVVT	SON	DRV	6	250	203.0	203.0	35.0
TPS3808G19DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3808G19DBVT	SOT-23	DBV	6	250	203.0	203.0	35.0
TPS3808G25DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G25DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3808G25DRVVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS3808G25DRVVT	SON	DRV	6	250	203.0	203.0	35.0
TPS3808G30DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G30DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3808G30DRVVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS3808G30DRVVT	SON	DRV	6	250	203.0	203.0	35.0
TPS3808G33DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G33DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3808G50DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G50DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-5/K 03/2006

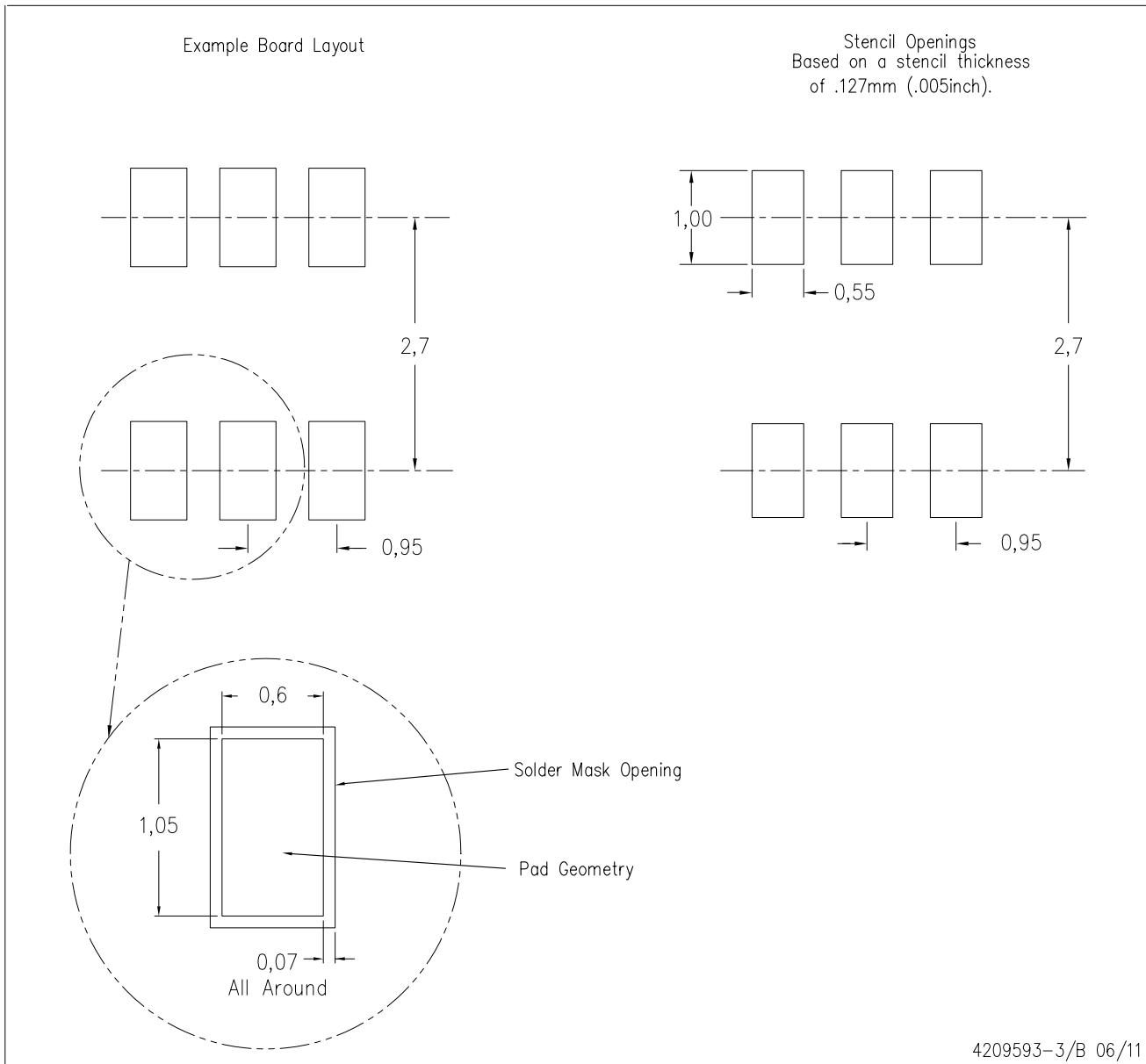
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.

 Falls within JEDEC MO-178 Variation AB, except minimum lead width.

LAND PATTERN DATA

DBV (R-PDSO-G6)



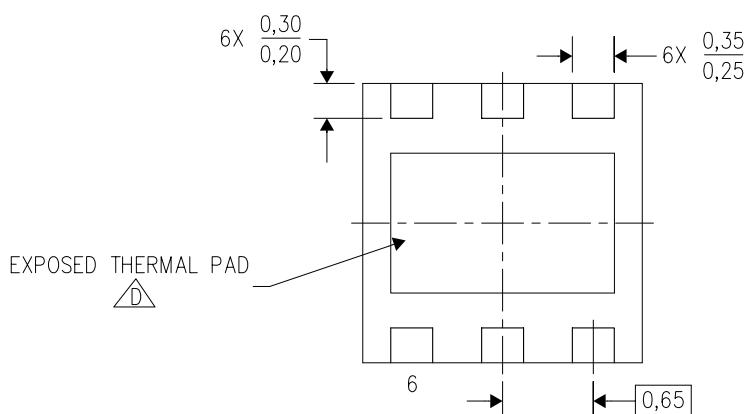
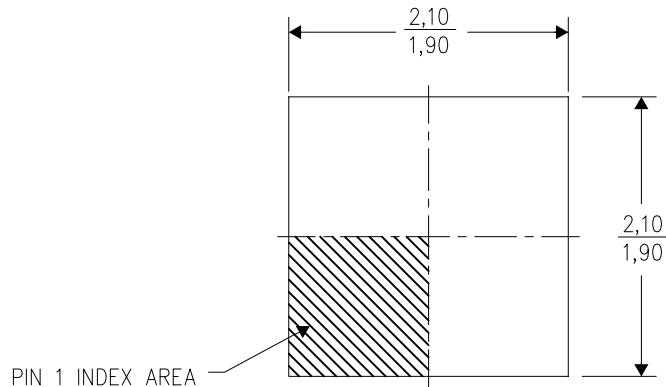
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

MECHANICAL DATA

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4206925/E 10/10

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Small Outline No-Lead (SON) package configuration.

 The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

DRV (S-PWSON-N6)

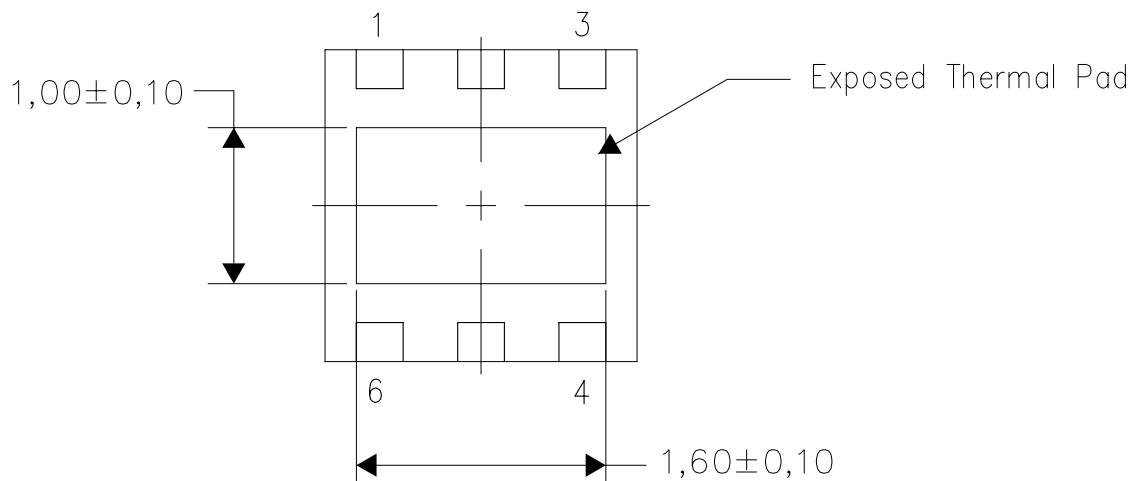
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

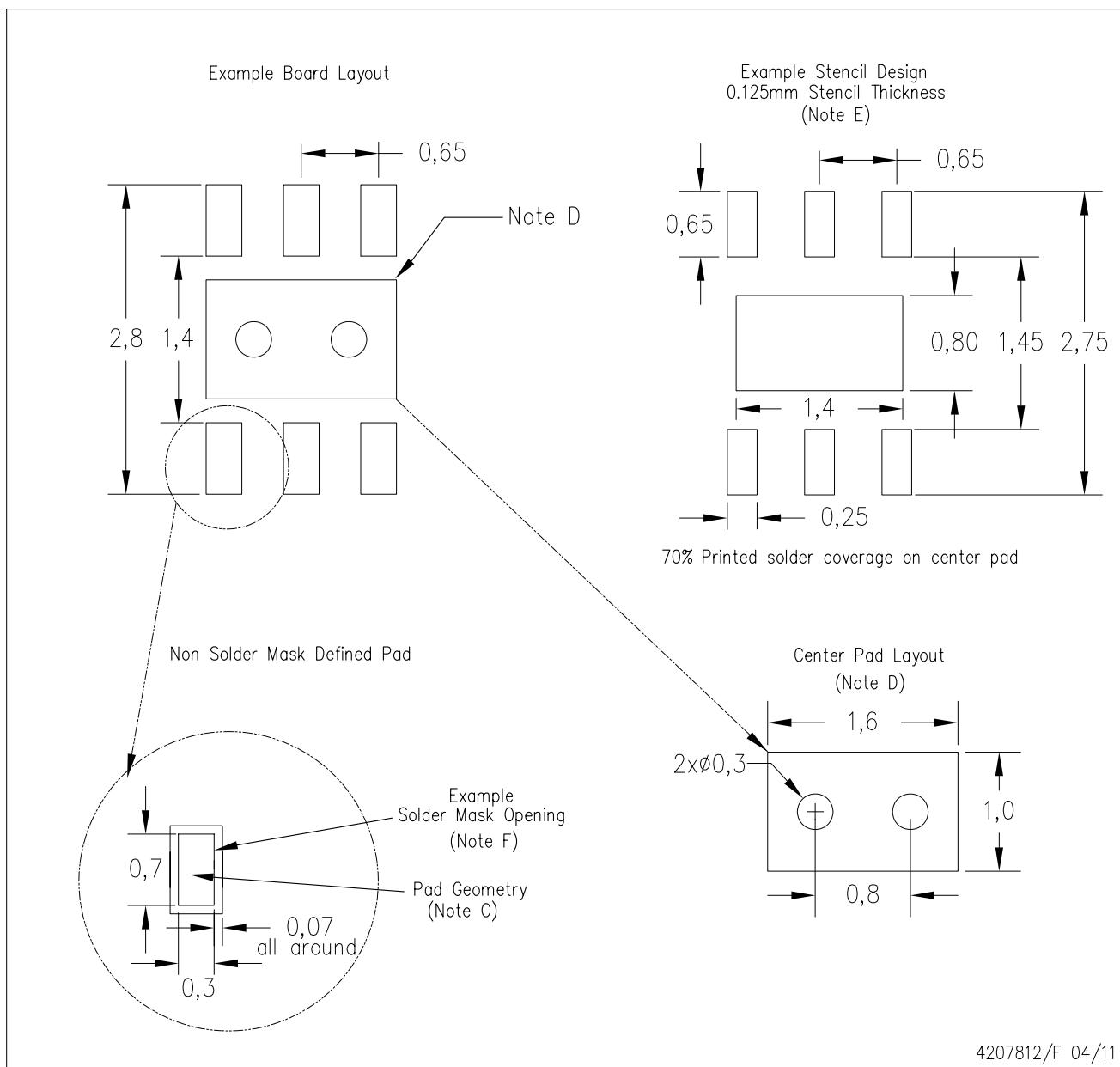
Exposed Thermal Pad Dimensions

4206926/K 04/11

NOTE: A. All linear dimensions are in millimeters

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for solder mask tolerances.

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