

DESCRIPTION

The HI-8585 and HI-8586 are CMOS integrated circuits designed to directly drive the ARINC 429 bus in an 8 pin package. Two logic inputs control a differential voltage between the output pins producing a +10 volt One, a -10 volt Zero, and a 0 volt Null.

The CMOS/TTL control inputs are translated to ARINC specified amplitudes using on board zeners. A logic input is provided to control the slope of the differential output signal. Timing is set by on-chip resistor and capacitor and tested to be within ARINC requirements.

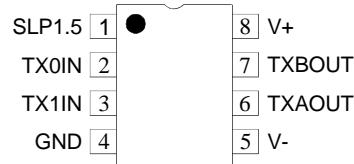
The HI-8585 has 37.5 ohms in series with each line driver output. The HI-8586 provides the option to bypass most of the output resistance so that series protection circuits can add their resistances.

The HI-8585 or the HI-8586 along with the HI-8588 line receiver offer the smallest options available to get on and off the ARINC bus.

FEATURES

- Direct ARINC 429 line driver interface in a small package
- On-chip zener to set output levels
- On-chip line driver slope control and selection by logic input
- Low current 12 to 15 volt supplies
- CMOS / TTL logic pins
- Plastic and ceramic package options - surface mount and DIP
- Thermally enhanced SOIC packages
- Mil processing available

PIN CONFIGURATION



SUPPLY VOLTAGES

V+ = 12V to 15V
 V- = -12V to -15V

FUNCTION TABLE

TX1IN	TX0IN	SLP1.5	TXAOUT	TXBOUT	SLOPE
0	0	X	0V	0V	N/A
0	1	0	-5V	5V	10µs
0	1	1	-5V	5V	1.5µs
1	0	0	5V	-5V	10µs
1	0	1	5V	-5V	1.5µs
1	1	X	0V	0V	N/A

PIN DESCRIPTION TABLE

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	SLP1.5	LOGIC INPUT	CMOS OR TTL, V+IS OK
2	TX0IN	LOGIC INPUT	CMOS OR TTL
3	TX1IN	LOGIC INPUT	CMOS OR TTL
4	GND	POWER	GROUND
5	V-	POWER	-12 TO -15 VOLTS
6	TXAOUT	LOGIC OUTPUT	LINE DRIVER TERMINAL A
7	TXBOUT	LOGIC OUTPUT	LINE DRIVER TERMINAL B
8	V+	POWER	+12 TO +15 VOLTS

FUNCTIONAL DESCRIPTION

Figure 1 is a block diagram of the line driver. The +5V and -5V levels are generated internally using on-chip zeners. Currents for slope control are set by zener voltages across on-chip resistors.

The TX0IN and TX1IN inputs receive logic signals from a control transmitter chip such as the HI-6010, HI-3282 or HI-8282. TXAOUT and TXBOUT hold each side of the ARINC bus at Ground until one of the inputs becomes a One. If for example TX1IN goes high, a charging path is enabled to 5V on an "A" side internal capacitor while the "B" side is enabled to -5V. The charging current is selected by the SLP1.5 pin. If the SLP1.5 pin is high, the capacitor is nominally charged from 10% to 90% in 1.5 μ s. If SLP1.5 is low, the rise and fall times are 10 μ s.

A unity gain buffer receives the internally generated slopes and differentially drives the ARINC line. Current is limited by the series output resistors at each pin. There are no fuses at the outputs of the HI-8585 as exists on the HI-8382.

The HI-8585 has 37.5 ohms in series with each output. The HI-8586 has 10 ohms in series. The HI-8586 is for applications where more series resistance is added externally, typically for lightning protection devices.

Both the HI-8585 and HI-8586 are built using high-speed CMOS technology. Care should be taken to ensure the V+ and V- supplies are locally decoupled and that the input waveforms are free from negative voltage spikes which may upset the chip's internal slope control circuitry.

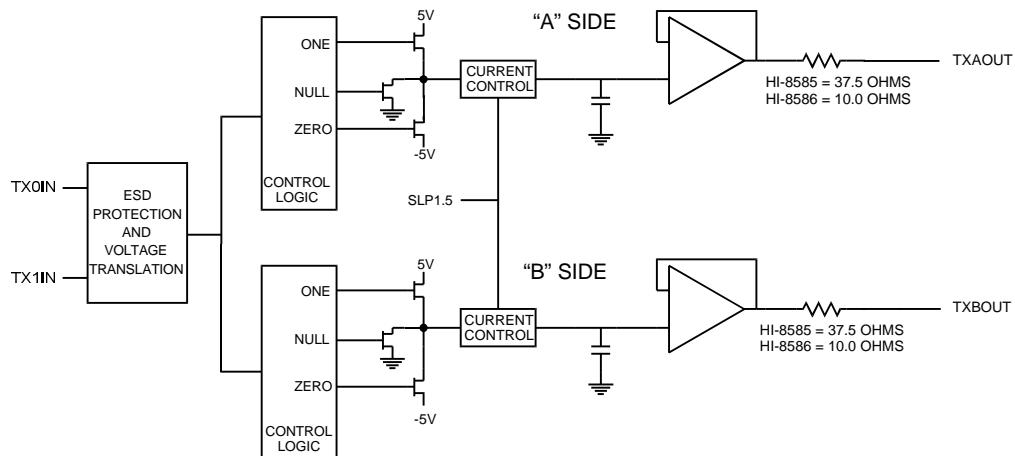


FIGURE 1 - LINE DRIVER BLOCK DIAGRAM

APPLICATION INFORMATION

Figure 2 shows a possible application of the HI-8585/86 interfacing an ARINC transmit channel from the HI-6010.

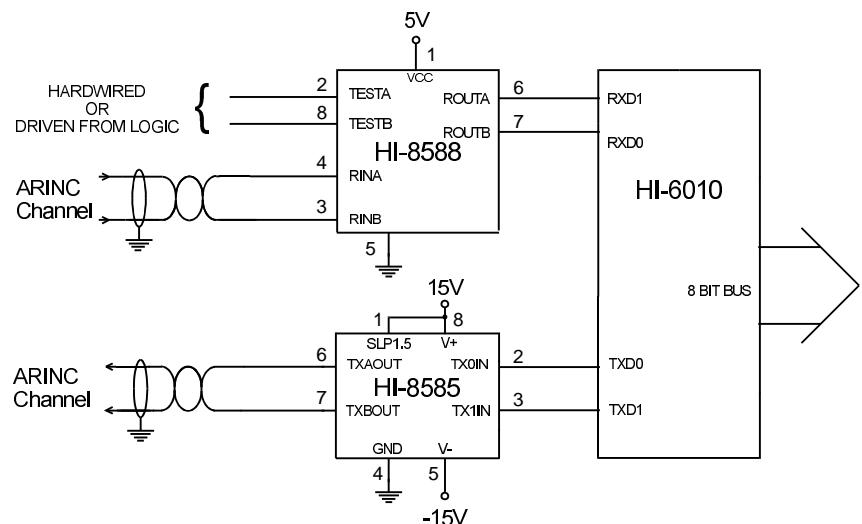


FIGURE 2 - APPLICATION DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground

Supply voltages	
V+.....	20V
V-.....	-20V
DC current per input pin.....	+10mA
Power dissipation at 25°C	
plastic DIL.....	1.0W, derate 10mW/°C
ceramic DIL.....	0.5W, derate 7mW/°C
Solder Temperature	275°C for 10 sec
Storage Temperature.....	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltages	
V+.....	+12V ± 5% or +15V ±10%
V-.....	-12V ± 5% or -15V ±10%

Temperature Range	
Industrial Screening.....	-40°C to +85°C
Hi-Temp Screening.....	-55°C to +125°C
Military Screening.....	-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

V+ = +12V to +15V, V- = -12V to -15V, T_A = Operating Temperature Range (unless otherwise stated)

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage (TX1IN, TX0IN, SLP1.5) high low	V _{IH} V _{IL}		2.1 -	- -	V+ 0.5	volts volts
Input current (TX1IN, TX0IN, SLP1.5) source sink	I _{IH} I _{IL}	V _{IN} = 0V V _{IN} = 5V	- -	- -	0.1 0.1	µA µA
ARINC output voltage (Differential) one zero null	V _{DIFF1} V _{DIFF0} V _{DIFFN}	no load; TXAOUT - TXBOUT no load; TXAOUT - TXBOUT no load; TXAOUT - TXBOUT	9.00 -11.00 -0.50	10.00 -10.00 0	11.00 -9.00 0.50	volts volts volts
ARINC output voltage (Ref. to GND) one or zero null	V _{DOUT} V _{NOUT}	no load & magnitude at pin no load	4.50 -0.25	5.00 0	5.50 0.25	volts volts
Operating supply current V+ V-	I _{DD} I _{EE}	SLP1.5 = V+ TX1IN & TX0IN = 0V: no load TX0IN & TX1IN = 0V: no load	- -14.0	6.0 -6.0	14.0 -	mA mA
ARINC output impedance HI-8585 HI-8586	Z _{OUT}	Note1	- -	37.5 10	- -	ohms ohms

NOTE :

1. The output resistance is checked by measuring the momentary short circuit current at each ARINC output pin.

AC ELECTRICAL CHARACTERISTICS

V₊ = 15.0V, V₋ = -15V, T_A = Operating Temperature Range (unless otherwise stated)

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Line Driver propagation delay Output high to low Output low to high	t_{phlx} t_{plhx}	defined in Figure 3, no load	-	500	-	ns
Line Driver transition times Output high to low Output low to high	t_{fx} t_{rx}	pin 1 = logic 1 pin 1 = logic 1	1.0 1.0	1.5 1.5	2.0 2.0	μ s μ s
Input capacitance (1) logic	C_{IN}		-	-	10	pF

Notes:

1. Guaranteed but not tested

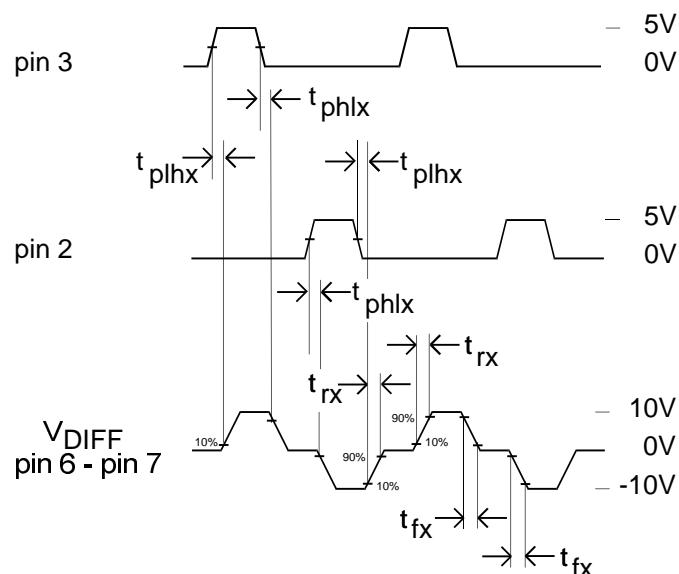


FIGURE 3 - LINE DRIVER TIMING

PACKAGE THERMAL CHARACTERISTICS

MAXIMUM ARINC LOAD⁹

PACKAGE STYLE ¹	ARINC 429 DATA RATE	SUPPLY CURRENT (mA) ²			JUNCTION TEMP, T _j (°C)		
		T _a = 25°C	T _a = 85°C	T _a = 125°C	T _a = 25°C	T _a = 85°C	T _a = 125°C
8 Lead Plastic DIP	Low Speed ³	16.8	17.2	16.9	58	116	157
	High Speed ⁴	27.3	26.7	25.9	75	132	169
8 Lead Plastic ESOIC ⁵	Low Speed	17.4	17.5	16.9	68	126	166
	High Speed	27.6	27.1	25.9	97	147	186
8 Lead Plastic ESOIC ⁶	Low Speed	17.1	17.2	16.7	52	110	151
	High Speed	27.3	27.1	26.2	57	112	157

TXAOUT and TXBOUT Shorted to Ground^{7, 8, 9}

PACKAGE STYLE ¹	ARINC 429 DATA RATE	SUPPLY CURRENT (mA) ²			JUNCTION TEMP, T _j (°C)		
		T _a = 25°C	T _a = 85°C	T _a = 125°C	T _a = 25°C	T _a = 85°C	T _a = 125°C
8 Lead Plastic DIP	Low Speed ³	53.6	50.7	52.2	131	181	217
	High Speed ⁴	46.9	38.7	42.5	135	181	219
8 Lead Plastic ESOIC ⁵	Low Speed	46.4	47.6	68.1	167	191	221
	High Speed	42.1	43.8	67.1	177	212	223
8 Lead Plastic ESOIC ⁶	Low Speed	48.5	45.6	46.1	112	161	186
	High Speed	46.8	41.1	40.5	116	168	197

Notes:

1. All data taken in still air on devices soldered to single layer copper PCB (3" X 4.5" X .062").
2. At 100% duty cycle, 15V power supplies. For 12V power supplies multiply all tabulated values by 0.8.
3. Low Speed: Data Rate = 12.5 Kbps, Load: R = 400 Ohms, C = 30 nF.
4. High Speed: Data Rate = 100 Kbps, Load: R = 400 Ohms, C = 10 nF. Data not presented for C = 30 nF as this is considered unrealistic for high speed operation.
5. 8 Lead Plastic ESOIC (Thermally enhanced SOIC with built in heat sink). Heat sink not soldered to the PCB.
6. 8 Lead Plastic ESOIC (Thermally enhanced SOIC with built in heat sink). Heat sink soldered to the PCB.
7. Similar results would be obtained with TXAOUT shorted to TXBOUT.
8. For applications requiring survival with continuous short circuit, operation above T_j = 175°C is not recommended.
9. Data will vary depending on air flow and the method of heat sinking employed.

HEAT SINK - ESOIC PACKAGES

An 8-pin thermally enhanced SOIC package is used for the HI-8585/HI-8586 products. The ESOIC package includes a metal heat sink located on the bottom surface of the device. This heat sink should be soldered down to the printed circuit board for optimum thermal dissipation. The

heat sink is electrically isolated from the chip and can be soldered to any ground or power plane. However, since the chip's substrate is at V+, connecting the heat sink to this power plane is recommended to avoid coupling noise into the circuit.

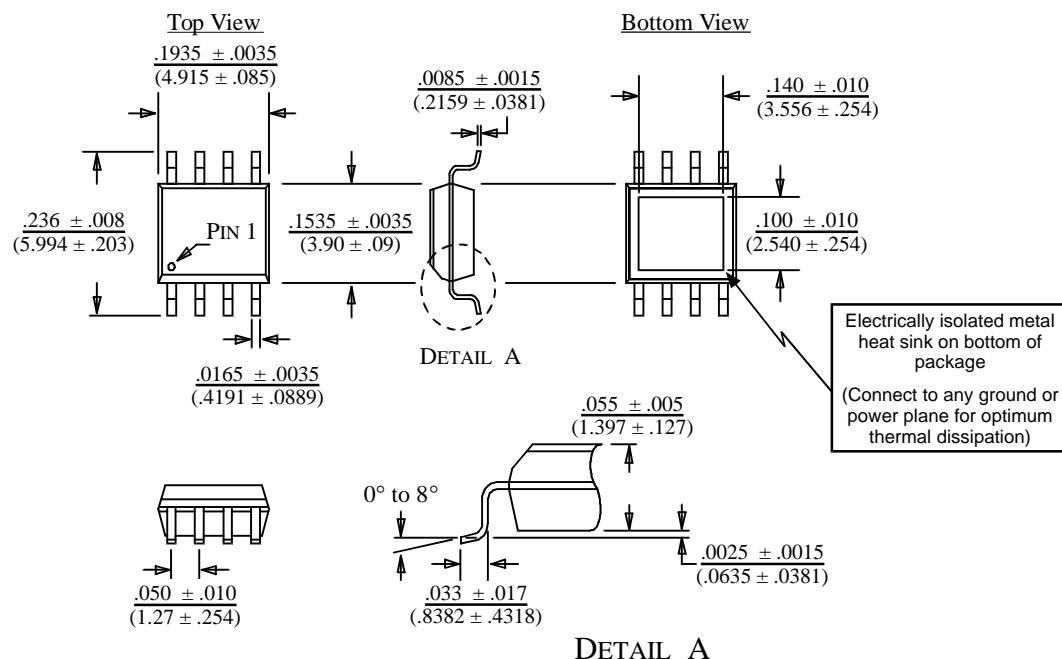
ORDERING INFORMATION

PART NUMBER	PACKAGE DESCRIPTION	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
HI-8585PDI	8 PIN PLASTIC DIP	-40°C TO +85°C	I	NO	SOLDER
HI-8585PDT	8 PIN PLASTIC DIP	-55°C TO +125°C	T	NO	SOLDER
HI-8585PSI	8 PIN PLASTIC ESOIC - NB	-40°C TO +85°C	I	NO	SOLDER
HI-8585PST	8 PIN PLASTIC ESOIC - NB	-55°C TO +125°C	T	NO	SOLDER
HI-8585CDI	8 PIN CERAMIC SIDE BRAZED DIP	-40°C TO +85°C	I	NO	GOLD
HI-8585CDT	8 PIN CERAMIC SIDE BRAZED DIP	-55°C TO +125°C	T	NO	GOLD
HI-8585CDM	8 PIN CERAMIC SIDE BRAZED DIP	-55°C TO +125°C	M	YES	SOLDER
HI-8585CRI	8 PIN CERDIP	-40°C TO +85°C	I	NO	SOLDER
HI-8585CRT	8 PIN CERDIP	-55°C TO +125°C	T	NO	SOLDER
HI-8585CRM	8 PIN CERDIP	-55°C TO +125°C	M	YES	SOLDER
HI-8586PDI	8 PIN PLASTIC DIP	-40°C TO +85°C	I	NO	SOLDER
HI-8586PDT	8 PIN PLASTIC DIP	-55°C TO +125°C	T	NO	SOLDER
HI-8586PSI	8 PIN PLASTIC ESOIC - NB	-40°C TO +85°C	I	NO	SOLDER
HI-8586PST	8 PIN PLASTIC ESOIC - NB	-55°C TO +125°C	T	NO	SOLDER
HI-8586CDI	8 PIN CERAMIC SIDE BRAZED DIP	-40°C TO +85°C	I	NO	GOLD
HI-8586CDT	8 PIN CERAMIC SIDE BRAZED DIP	-55°C TO +125°C	T	NO	GOLD
HI-8586CDM	8 PIN CERAMIC SIDE BRAZED DIP	-55°C TO +125°C	M	YES	SOLDER
HI-8586CRI	8 PIN CERDIP	-40°C TO +85°C	I	NO	SOLDER
HI-8586CRT	8 PIN CERDIP	-55°C TO +125°C	T	NO	SOLDER
HI-8586CRM	8 PIN CERDIP	-55°C TO +125°C	M	YES	SOLDER

Legend: ESOIC - Thermally Enhanced Small Outline Package (SOIC w/built-in heat sink)
 NB - Narrow Body

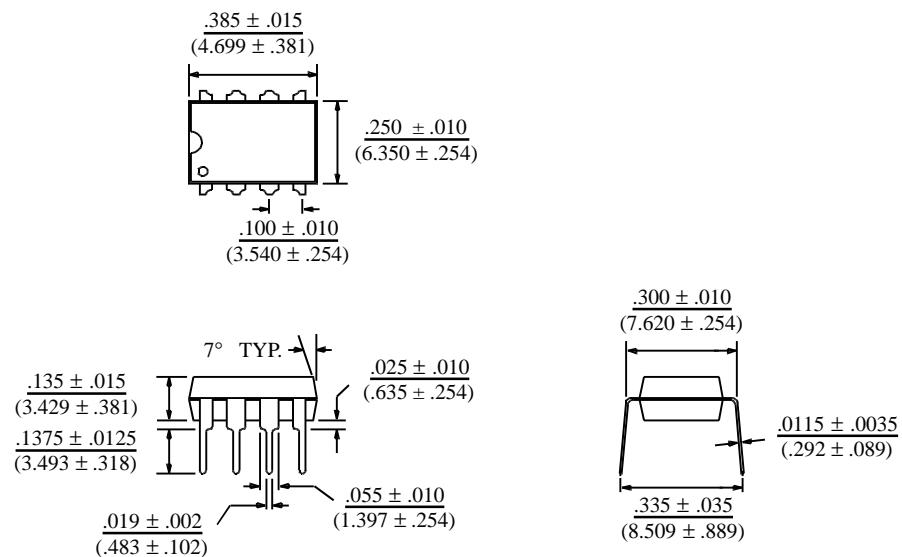
8-PIN PLASTIC SMALL OUTLINE (ESOIC) - NB
(Narrow Body, Thermally Enhanced)

Package Type: 8HNE



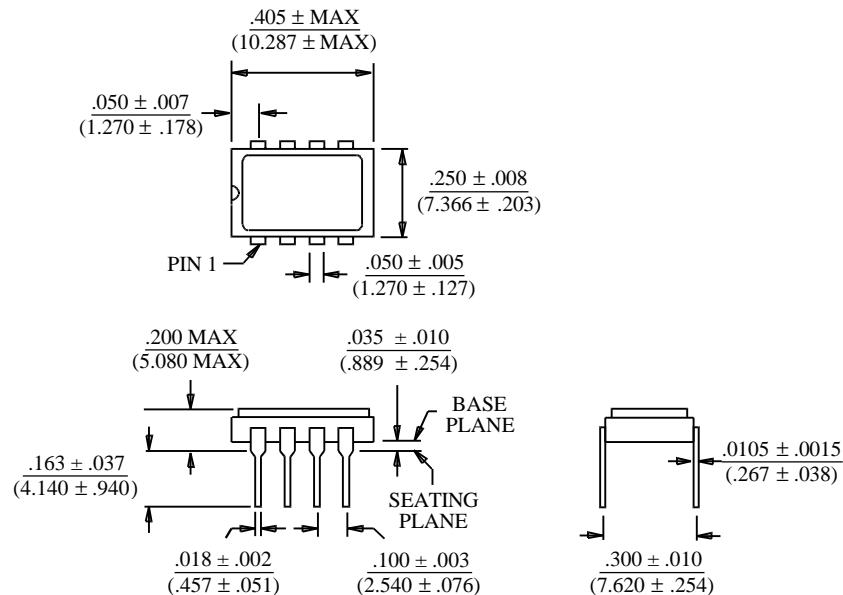
8-PIN PLASTIC DIP

Package Type: 8P



8-PIN CERAMIC SIDE-BRAZED DIP

Package Type: 8C



8-PIN CERDIP

Package Type: 8D

