Micro Linear

ML6622

High-Speed Data Quantizer

GENERAL DESCRIPTION

The ML6622 high-speed data quantizer (post-amplifier) is a low noise, wide-band, BiCMOS monolithic IC designed for high-speed signal recovery applications, such as FDDI, Fast Ethernet, and ATM. An internal DC restoration feedback loop nulls any offset voltage produced in the input stage. The limiting amplifier contributes to a high level of sensitivity and a minimum of duty cycle distortion.

The output of the data path is a high-speed comparator with ECL outputs. An enable pin gates the comparator on or off in response to the input signal level or a system control signal.

The Link Detect circuit provides an Assert-Deassert function with a user-selectable threshold voltage. This circuit monitors the input signal and provides an ECL High output within 100ms of signal acquisition and an ECL Low output within 350ms of signal loss. The ECL discriminator output can be used to disable the comparator when the signal is below the user-selected threshold. LINKLED drives an LED for a visible indication of the link status.

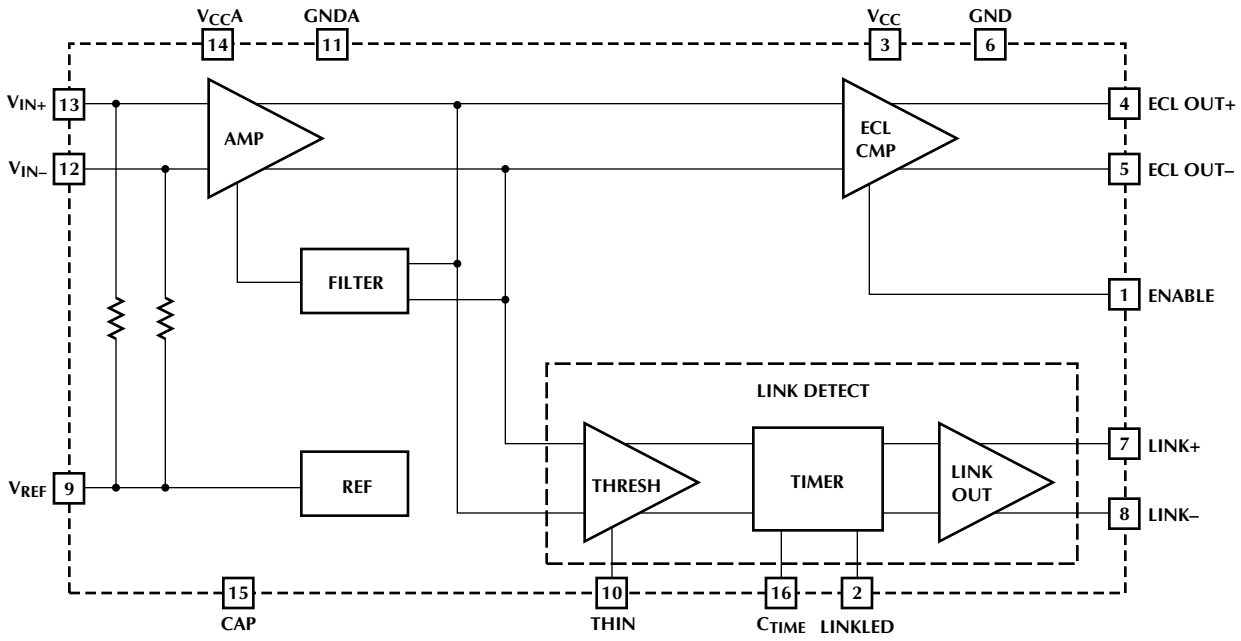
FEATURES

- 200 MHz bandwidth
- Low noise design
- Adjustable Link Detect function
- Low power design: 35mA typical
- Used with the ML6633 LED driver

APPLICATIONS

- FDDI
- Fast Ethernet, 100BASE-FX
- ATM (SONET), 155Mbps
- Fibre Channel, 133 or 266Mbps
- Proprietary high-speed fiber optic data links

BLOCK DIAGRAM



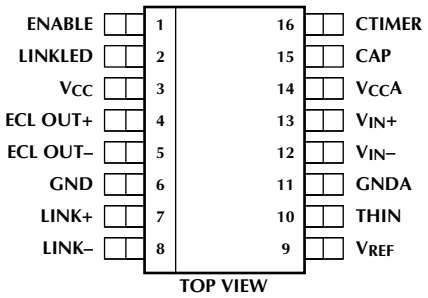
PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	ENABLE	ECL input active low. When this input is tied to LINKLED the ECL comparator output is automatically enabled and disabled by the Link Detect circuit. This input can be tied to GND for continuous enable. When the ECL Comparator is disabled, ECL OUT– goes low and ECL OUT+ goes high.
2	LINKLED	Link Detect Status output. LINKLED is an open collector active low signal. It will be active low when the input signal applied to V_{IN+},$V_{IN–}$ exceeds the programmed threshold level at the THIN pin. Capable of driving a 20mA LED indicator.
3	V_{CC}	Positive Power Supply. +5 volts
4 5	ECL OUT+ ECL OUT–	Positive and Negative ECL Comparator outputs. 1mA internal pull downs are incorporated.
6	GND	Ground connection. Used for less noise sensitive nodes.
7	LINK+	Positive ECL Link Detect output. Active high when the input signal exceeds the programmed Link Detect threshold. 1mA internal pull down current sources.
8	LINK –	Negative ECL Link Detect output. Active low when the input signal exceeds the programmed Link Detect threshold. 1mA internal pull down current sources.
9	V_{REF}	A 2.5V reference with respect to GND.

NAME	PIN #	FUNCTION
10	THIN	Threshold Input. A voltage applied to this input pin sets the minimum amplitude of the input signal required to cause the link detect to activate. In most cases this can be tied to V_{REF}.
11	GNDA	Ground connection for noise sensitive circuits in the chip; the input amplifier, DC restoration loop, part of the Comparator and part of the link detect circuit. In some system designs, it may be advantageous to separate GND and GNDA.
12	$V_{IN–}$	This input pin should be capacitively coupled to the input source or to V_{CC}A.
13	V_{IN+}	This input pin should be capacitively coupled to the input source or to V_{CC}A.
14	V_{CC}A	Positive power supply V_{CC} for noise sensitive circuits as mentioned in GNDA. +5 volts.
15	CAP	A capacitor is tied from this pin to V_{REF}. This capacitor sets the lower frequency rejection and helps remove internal DC offset. This capacitor should be 10 times larger than the input capacitors.
16	C_{TIMER}	A capacitor from this pin to ground determines the Link Detect response time. To Meet FDDI specifications this capacitor should be 2,000pF. This capacitor can be removed for faster response time.

PIN CONNECTION

ML6622
16-Pin Narrow SOIC (S16N)



ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} ..... GND –0.3V to 6V
$V_{CC}A$ ..... GND –0.3V to 6V
Inputs/Outputs ..... GND – 0.3V to V_{CC} + 0.3
Junction Temperature ..... 150°C

Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 260°C
Thermal Resistance ..... 100°C/W

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{CC} = V_{CC} = 5V \pm 10\%$, T_A = Operating Temperature Range. (Note 1)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{CC}	V_{CC} Supply Current	No load on ECL outputs			35	50	mA
V_{REF}	Reference Voltage			2.30	2.47	2.57	V
IV_{REF}	V_{REF} Output Current			–1	3	+5	mA
V_{IN}	Input Signal Range			3.5		1600	mV_{P-P}
V_{TH} ADJ Range	External Voltage at THIN to set V_{TH}			0.5		V_{REF}	V
EN	Input-referred Voltage Noise	100 MHz BW			25		μV_{RMS}
R_{IN}	Input Resistance	V_{IN}+, V_{IN}–		500	770	1500	Ω
I_{THIN}	Input Bias Current of THIN			–100		+100	µA
V_{OL}-V_{CC}	ECL Output Voltage-Low	Through 50Ω to V_{CC} –2V		–1.810	–1.730	–1.620	V
V_{OH}-V_{CC}	ECL Output Voltage-High	Through 50Ω to V_{CC} –2V	C Suffix	–1.025	–0.963	–0.800	V
			I Suffix	–1.025	–0.963	–0.780	V
t_r	Data Output Rise Time			0.5		1.3	ns
t_f	Data Output Fall Time			0.5		1.3	ns
Link Detect							
AS_Max	Assert Time (off to on)	C_{TIME} = 2000pF		0		100	µs
ANS_Max	Deassert Time (on to off)	C_{TIME} = 2000pF		0		350	µs
V_{TH}	Input threshold Hysteresis	THIN = V_{REF} Assert		8 1.5	10 1.7	12 2	mV dB
BW	Bandwidth 1-3dB				200		MHz
VIPW	Minimum Input Pulse Width				5		ns
DCD	Duty Cycle Distortion Peak-to-peak	Data rate = 155Mb/s 50% duty cycle input			0.5		ns
DDJ	Data Dependent Jitter Peak-to-peak	FDDI – 56 Data Pattern V_{IN} = 60mV, Data rate = 125Mb/s			1.2		ns

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case conditions.

FUNCTIONAL DESCRIPTION

The ML6622 high speed data quantizer accepts a low level analog signal from a pin diode and transimpedance amp front end and converts it into digital ECL levels for subsequent digital processing. The input signal, from a transimpedance amplifier, is immediately amplified by a two-stage video amplifier. The output of this amplifier feeds two parallel paths.

The data path is comprised of a high speed comparator that outputs PECL differential data on the ECL OUT± pins. The Link Detection path monitors the magnitude of the amplified input signal, compares it to a user-settable threshold, and provides the result of the comparison as a PECL differential output on the Link± pins. The timer following the threshold block is used to set the Link Detect output acquire and deacquire time using a capacitor.

AMPLIFIER

The amplifier is a two stage video amplifier with a gain of approximately 55V/V. Maximum sensitivity is achieved through the use of the DC restoration feedback loop and AC coupling the input. The AC coupling input capacitors, in conjunction with the input impedance of the amplifier, establish a high pass filter with the lower 3dB point determined by the input resistance and the input coupling capacitors. This cap also adds a secondary pole to the offset loop.

Since the amplifier has a differential input, two AC capacitors of equal value are required. If the signal driving the input is single ended, the other coupling capacitor should be tied to V_{CC}.

A low-pass filter in the offset loop is created with the capacitor on pin 15 (CAP). The lower 3dB point controlled by a capacitor tied from the CAP pin to V_{REF} as shown in the application circuit. For stability reasons the value of the capacitor on the CAP pin should be 10 times larger than the input coupling capacitors. The 3dB point is given by the following equation:

$$F_{3dB} = \frac{1}{2\pi \times 100k \times C}$$

Although the input is AC coupled, the offset voltage within the amplifier will be present at the amplifier's output. The removal of the dc offset in the amplifier helps the circuit respond to small input voltages, and reduces duty-cycle distortion. In order to reduce this error, a negative feedback loop nulls the offset voltage. An external capacitor connected to the CAP pin is used to store the offset voltage. This voltage is compared to V_{REF} and a difference current proportional to the result is applied to the negative side of the input stage of the AMP circuit block thereby nulling the DC offset.

COMPARATOR

A high speed ECL comparator with PECL outputs is used for the quantization function. The comparator has an Enable input pin which takes an ECL level. This Enable pin is normally driven by LINKLED, which causes the output to be enabled when the link is up and disabled when the link is down. When ENABLE is low the comparator is operational. When ENABLE is high the comparator is disabled causing ECL OUT– to go low and ECL OUT+ to go high. The ENABLE pin can be tied to ground to keep the comparator permanently enabled.

LINK DETECT CIRCUIT

The Link Detection Circuit is used to accurately measure the input amplitude to determine whether it is large enough to reliably recover the input signal. Once the Bit Error Rate (BER) for the ML6622 receive circuit is determined, the link detect threshold can be set so that the Link Detect Circuit will shut off before the error rate exceeds the link requirement.

The Link Detection Circuit consists of three functional blocks; Thresh, Timer, and Link Out. Thresh detects the output of Amp and compares it to a programmable threshold input THIN. As long as the input amptitude is greater than the programmable threshold input, the Link Detect output remains active.

When the peak input drops below THIN, Thresh's output changes state and Timer delays the Link Out state change for a programmable amount of time. When using the default C_{TIME} capacitance of 2000pF, the deassert time and the assert time values conform to the ANSI X3.166-1990 PMD standard for FDDI.

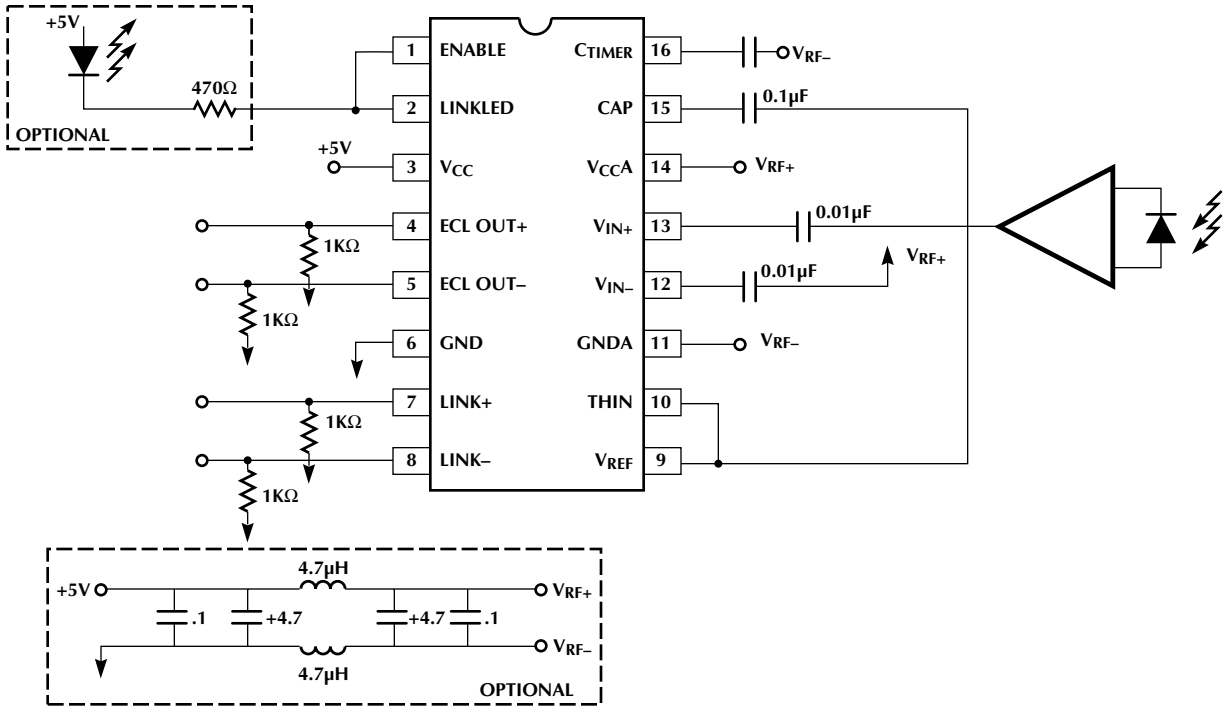
To improve stability, the Link Detect circuit includes 1.7dB of hysteresis.

The V_{REF} output can be tied directly to THIN to set the Link Detect threshold. For greater sensitivities, V_{REF} can be divided down before applied to THIN. The formula for the threshold on the thin pin is as follows:

$$\text{Threshold(Assert)} = \frac{V_{THIN}}{500}$$

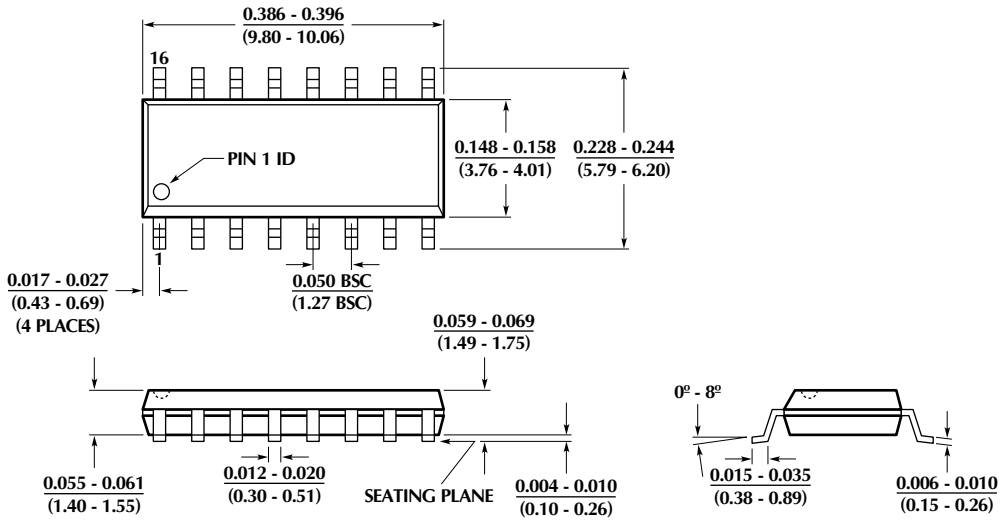
$$\text{Threshold(Deassert)} = \frac{V_{THIN}}{750}$$

APPLICATION CIRCUIT



PHYSICAL DIMENSIONS inches (millimeters)

Package: S16N
16-Pin Narrow SOIC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6622CS	0° to 70°C	16-Pin Narrow SOIC (S16N)
ML6622IS	–40° to 85°C	16-Pin Narrow SOIC (S16N)

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When sending e-mail, be sure to include the Micro Linear part number and whether you want a price quote or a sample in the subject line.

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