THS7530 High-Speed, Fully Differential, Continuously Variable Gain Amplifier

1 Features

- Low Noise: $V_n = 1.1\ nV/\sqrt{Hz}$, Noise Figure = 9 dB
- Low Distortion:
  - $HD_2 = –65$ dBc, $HD_3 = –61$ dBc at 32 MHz
  - $IMD_3 = –62$ dBc, $OIP_3 = 21$ dBm at 70 MHz
- 300-MHz Bandwidth
- Continuously Variable Gain Range: 11.6 dB to 46.5 dB
- Gain Slope: 38.8 dB/V
- Fully Differential Input and Output
- Output Common-Mode Voltage Control
- Output Voltage Limiting

2 Applications

- Time Gain Amplifiers in Ultra Sound, Sonar, and Radar
- Automatic Gain Control in Communication and Video
- System Gain Calibration in Communications
- Variable Gain in Instrumentation

3 Description

The THS7530 device is fabricated using Texas Instruments' state-of-the-art BiCom III SiGe complementary bipolar process. The THS7530 device is a DC-coupled, wide bandwidth amplifier with voltage-controlled gain. The amplifier has high-impedance differential inputs and low-impedance differential outputs with high-bandwidth gain control, output common-mode control, and output voltage clamping.

Signal-channel performance is exceptional with 300-MHz bandwidth, and third harmonic distortion of –61 dBc at 32 MHz with $1\text{-}V_{PP}$ output into 400 Ω.

Gain control is linear in dB with 0 V to 0.9 V varying the gain from 11.6 dB to 46.5 dB with 38.8-dB/V gain slope.

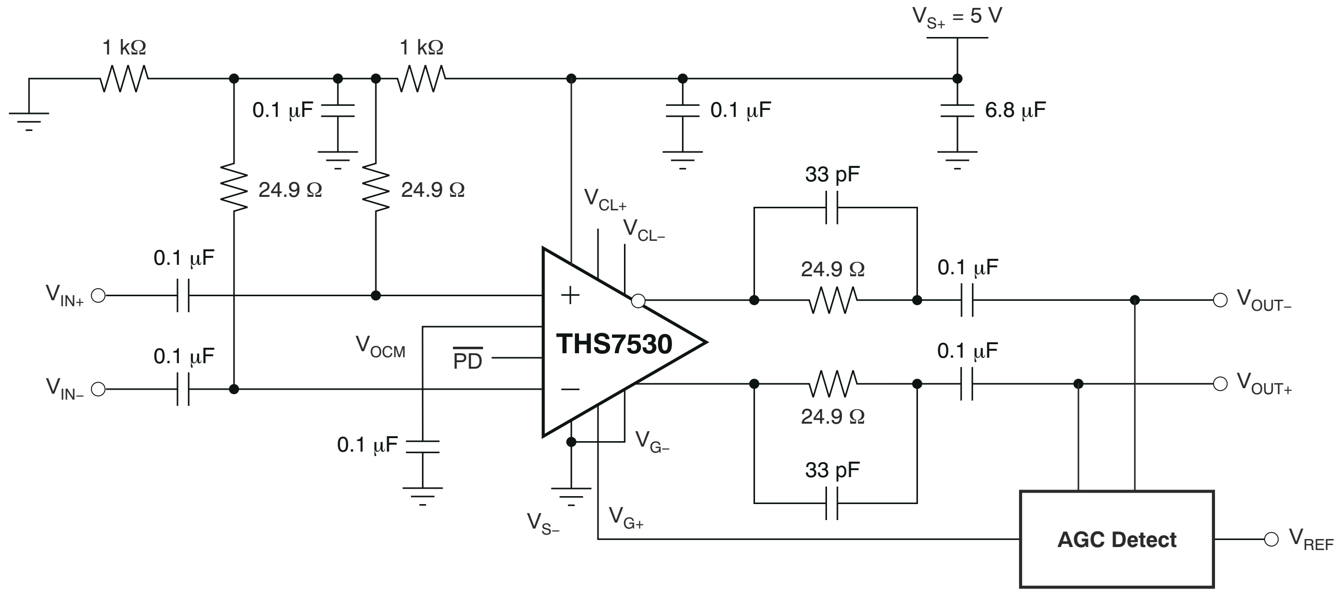
Output voltage limiting is provided to limit the output voltage swing and to prevent saturating following stages.

The device is characterized for operation over the industrial temperature range, –40°C to +85°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS7530	HTSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Circuit

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2015) to Revision E (August 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision C (February 2010) to Revision D (July 2015)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision B (February 2006) to Revision C (February 2010)	Page
• Corrected polarity indication on input and output in front-page figure	1
• Deleted *lead temperature* specification from Absolute Maximum Ratings table	4
• Corrected Figure 7-2	11
• Changed Figure 9-2 and Figure 9-3 to correct problem with output polarity indication	14
• Changed Figure 9-4 and Figure 9-5 to correct problem with output polarity indication	14

5 Pin Configuration and Functions

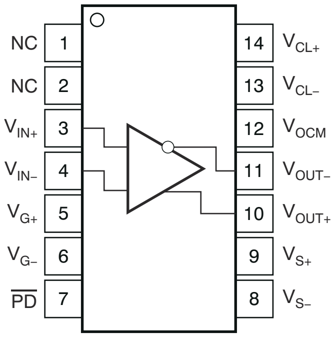


Figure 5-1. PWP Package 14-Pin HTSSOP With PowerPAD™ Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
NC	1 2	—	No internal connection
$\overline{PD}$	7	—	Power down, $\overline{PD}$ = logic low puts the device into low power mode; $\overline{PD}$ = logic high or open for normal operation
$V_{CL–}$	13	I	Output negative clamp voltage input
V_{CL+}	14	I	Output positive clamp voltage input
V_{G-}	6	I	Gain setting negative input
V_{G+}	5	I	Gain setting positive input
$V_{IN–}$	4	I	Inverting amplifier input
V_{IN+}	3	I	Noninverting amplifier input
V_{OCM}	12	I	Output common-mode voltage input
$V_{OUT–}$	11	O	Inverted amplifier output
V_{OUT+}	10	O	Noninverted amplifier output
$V_{S–}$	8	I	Negative amplifier power-supply input
V_{S+}	9	I	Positive amplifier power-supply input

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
$V_{S+} – V_{S–}$	Supply voltage		5.5	V
V_I	Input voltage		$±V_S$	V
I_O	Output current		65	mA
V_{ID}	Differential input voltage		±4	V
	Continuous power dissipation	See *Section 6.4*		
T_J	Maximum junction temperature		150	°C
	Maximum junction temperature for long term stability(2)		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
$[V_{S–}$ to $V_{S+}]$	Supply voltage		4.5	5	5.5	V
	Input common mode voltage	$[V_{S–}$ to $V_{S+}] = 5$ V		2.5		V
	Output common mode voltage	$[V_{S–}$ to $V_{S+}] = 5$ V		2.5		V
T_A	Operating free-air temperature		–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		THS7530	UNIT
		PWP (HTSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: Main Amplifier

V_{S+} = 5 V, V_{S-} = 0 V, V_{OCM} = 2.5 V, V_{ICM} = 2.5 V, V_{G-} = 0 V, V_{G+} = 1 V (maximum gain), T_A = 25°C, AC performance measured using the AC test circuit shown in Figure 7-1 (unless otherwise noted). DC performance is measured using the DC test circuit shown in Figure 7-2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE					
Small-signal bandwidth	All gains, P_{IN} = –45 dBm		300		MHz
Slew rate(1)	1-V_{PP} Step, 25% to 75%, minimum gain		1250		V/µs
Settling time to 1%(1)	1-V_{PP} Step, minimum gain		11		ns
Harmonic distortion, 2nd harmonic	f = 32 MHz, $V_{O(PP)}$ = 1 V, $R_{L(diff)}$= 400 Ω		–65		dBc
Harmonic distortion, 3rd harmonic	f = 32 MHz, $V_{O(PP)}$ = 1 V, $R_{L(diff)}$= 400 Ω		–61		dBc
Third-order intermodulation distortion	P_O = –10 dBm each tone, f_C= 70 MHz, 200-kHz tone spacing		–62		dBc
Third-order output intercept point	f_C= 70 MHz, 200-kHz tone spacing		21		dBm
Noise figure (with input termination)	Source impedance: 50 Ω		9		dB
Total input voltage noise	f > 100 kHz		1.1		$\text{nV}/\sqrt{\text{Hz}}$
DC PERFORMANCE—INPUTS					
Input bias current	T_A = 25°C		20	39	µA
	T_A = –40°C to +85°C			40	
Input bias current offset			<150		pA
Minimum input voltage	Minimum gain, T_A = 25°C		1.5	1.6	V
	Minimum gain, T_A = –40°C to +85°C			1.7	
Maximum input voltage	Minimum gain, T_A = 25°C	3.35	3.5		V
	Minimum gain, T_A = –40°C to +85°C	3.2			
Common-mode rejection ratio	T_A = 25°C	56	114		dB
	T_A = –40°C to +85°C	44			
Differential input impedance			8.5 || 3		kΩ || pF
DC PERFORMANCE—OUTPUTS					
Output offset voltage	All gains, T_A = 25°C		±100	±340	mV
	All gains, T_A = –40°C to +85°C			±480	
Maximum output voltage high	T_A = 25°C	3.275	3.5		V
	T_A = –40°C to +85°C	3.25			
Minimum output voltage low	T_A = 25°C		1.5	1.7	V
	T_A = –40°C to +85°C			1.8	
Output current	T_A = 25°C	±16	±37		mA
	T_A = –40°C to +85°C	±16			
Output impedance			15		Ω
OUTPUT COMMON-MODE VOLTAGE CONTROL					
Small-signal bandwidth			32		MHz
Gain			1		V/V
Common-mode offset voltage	T_A = 25°C		4.5	12	mV
	T_A = –40°C to +85°C			13.8	
Minimum input voltage			1.75		V
Maximum input voltage			3.25		V
Input impedance			25 || 1		kΩ || pF
Default voltage, with no connect			2.5		V
Input bias current			<1		µA
GAIN CONTROL					
Gain control differential voltage range	V_{G+}		0 to 1		V
Minus gain control voltage	V_{G-} – V_{S-}		–0.6 to 0.8		V
Minimum gain	V_{G+} = 0 V		11.6		dB

6.5 Electrical Characteristics: Main Amplifier (continued)

V_{S+} = 5 V, $V_{S–}$ = 0 V, V_{OCM} = 2.5 V, V_{ICM} = 2.5 V, V_{G-} = 0 V, V_{G+} = 1 V (maximum gain), T_A = 25°C, AC performance measured using the AC test circuit shown in Figure 7-1 (unless otherwise noted). DC performance is measured using the DC test circuit shown in Figure 7-2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum gain	V_{G+} = 0.9 V		46.5		dB
Gain slope	V_{G+} = 0 V to 0.9 V		38.8		dB/V
Gain slope variation	V_{G+} = 0 V to 0.9 V		±1.5		dB/V
Gain error	V_{G+} = 0 V to 0.15 V		±4		dB
	V_{G+} = 0.15 V to 0.9 V		±2.25		
Gain control input bias current			<1		μA
Gain control input resistance			40		kΩ
Gain control bandwidth	Small signal –3 dB		15		MHz
VOLTAGE CLAMPING					
Output voltages ($V_{OUT±}$) relative to clamp voltages ($V_{CL±}$)	Device In voltage limiting mode, T_A = 25°C		±25	±38	mV
	Device In voltage limiting mode, T_A = –40°C to +85°C			±60	
Clamp voltage ($V_{CL±}$) input resistance	Device in voltage limiting mode		3.3		kΩ
Clamp voltage ($V_{CL±}$) limits			$V_{S–}$ to V_{S+}		V
POWER SUPPLY					
Specified operating voltage	T_A = 25°C		5	5.5	V
	T_A = –40°C to +85°C			5.5	
Maximum quiescent current	T_A = 25°C		40	48	mA
	T_A = –40°C to +85°C			49	
Power supply rejection (±PSRR)	T_A = 25°C	70	77		dB
	T_A = –40°C to +85°C	45			
POWER DOWN					
Enable voltage threshold	TTL low = shut down, T_A = 25°C		1.4		V
	TTL low = shut down, T_A = –40°C to +85°C	1			
Disable voltage threshold	TTL high = normal operation, T_A = 25°C		1.4		V
	TTL high = normal operation, T_A = –40°C to +85°C			1.65	
Power-down quiescent current	T_A = 25°C		0.35	0.4	mA
	T_A = –40°C to +85°C			0.45	
Input current high	T_A = 25°C		±9	±16	μA
	T_A = –40°C to +85°C			±19	
Input current low	T_A = 25°C		±109	±116	μA
	T_A = –40°C to +85°C			±119	
Input impedance			50 || 1		kΩ || pF
Turnon time delay	Measured to 50% quiescent current		820		ns
Turnoff time delay	Measured to 50% quiescent current		500		ns
Forward isolation in power down			80		dB
Input resistance in power down			> 1		MΩ
Output resistance in power down			16		kΩ

(1) Slew rate and settling time measured at amplifier output.

6.6 Package Thermal Data

PACKAGE	PCB	T_A = 25°C POWER RATING[1]
PWP (14-pin)[2]	See *Section 11*.	3 W

[1] This data was taken using 2 oz trace and copper pad that is soldered directly to a 3 in × 3 in PCB.

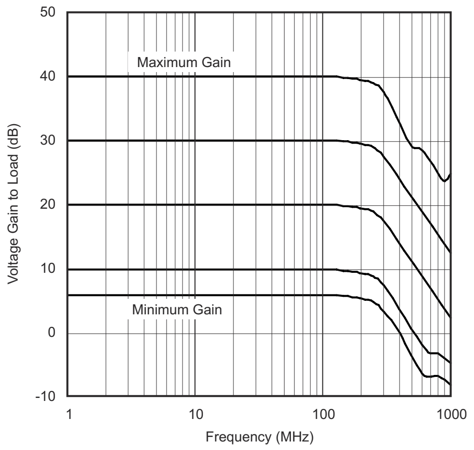
[2] The THS7530 incorporates a PowerPAD on the underside of the chip. The PowerpAD acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about using the PowerPAD thermally enhanced package.

6.7 Typical Characteristics

Measured using the AC test circuit shown in Figure 7-1 (unless otherwise noted).

Table 6-1. Table Of Graphs

		FIGURE
Voltage Gain to Load	vs Frequency (Input at 45 dBm)	Figure 6-1
Gain and Gain Error	vs V_{G+}	Figure 6-2
Noise Figure	vs Frequency	Figure 6-3
Output Intercept Point	vs Frequency	Figure 6-4
1-dB Compression Point	vs Frequency	Figure 6-5
Total Input Voltage Noise	vs Frequency	Figure 6-6
Intermodulation Distortion	vs Frequency	Figure 6-7
Harmonic Distortion	vs Frequency	Figure 6-8
S-Parameters	vs Frequency	Figure 9-7
Differential Input Impedance of Main Amplifier	vs Frequency	Figure 9-8
Differential Output Impedance of Main Amplifier	vs Frequency	Figure 6-9
V_{G+} Input Impedance	vs Frequency	Figure 6-10
V_{OCM} Input Impedance	vs Frequency	Figure 6-11
Common-Mode Rejection Ratio	vs Frequency	Figure 6-12
Step Response: 2 V_{PP}	vs Time	Figure 6-13
Step Response: Rising Edge	vs Time	Figure 6-14
Step Response: Falling Edge	vs Time	Figure 6-15



Gain is taken at load. Add 6 dB to refer to amplifier output

P_{IN} = –45 dBm

Figure 6-1. Voltage Gain to Load vs Frequency

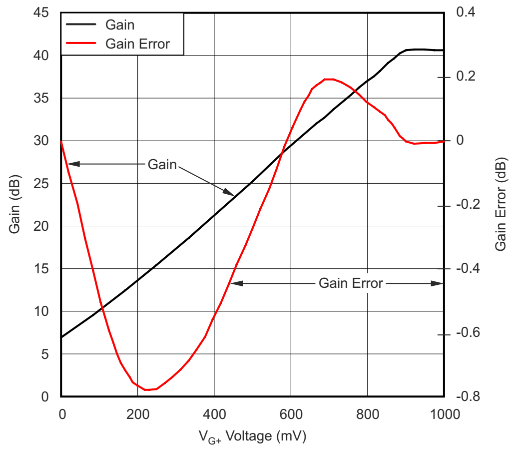
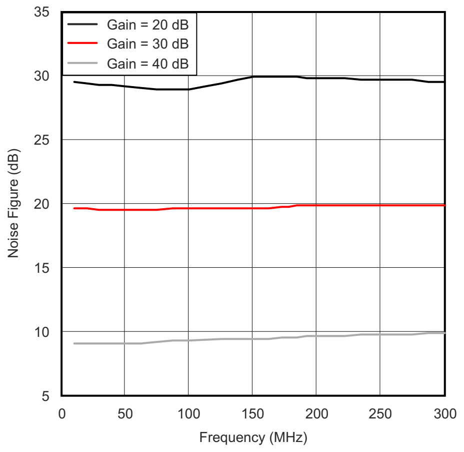
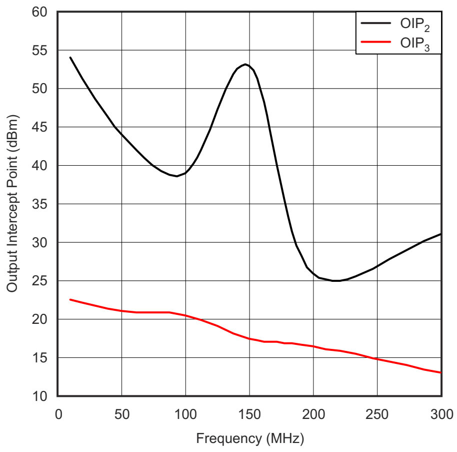


Figure 6-2. Gain and Gain Error vs V_{G+}



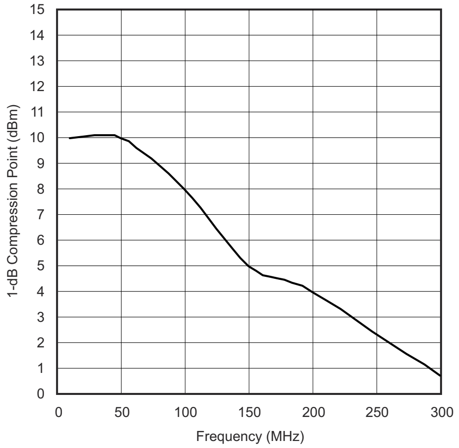
Terminated input

Figure 6-3. Noise Figure vs Frequency



Taken at load. Add 3 dB to refer to amplifier output.

Figure 6-4. Output Intercept Point vs Frequency



Taken at load. Add 3 dB to refer to amplifier output.

Figure 6-5. 1-dB Compression Point vs Frequency

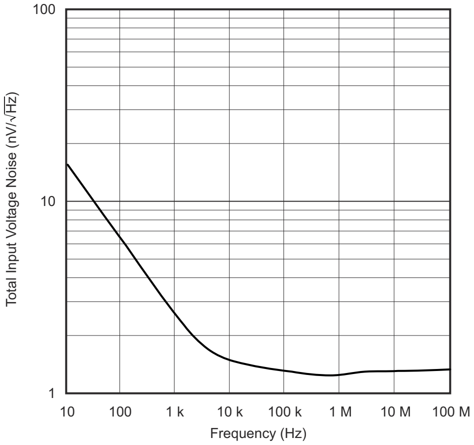
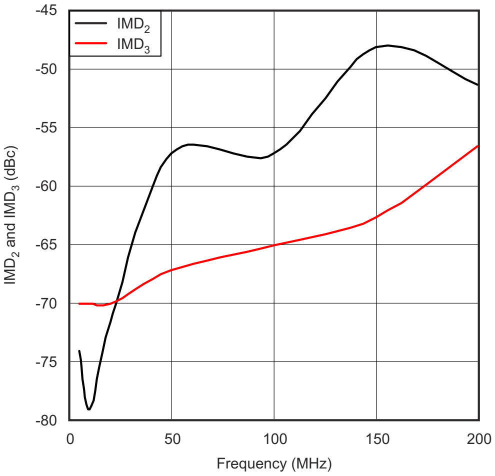
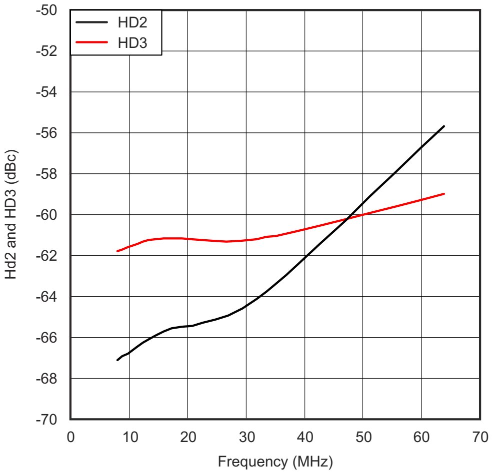


Figure 6-6. Total Input Voltage Noise vs Frequency



V_{G+} = 1 V V_O = 1 V_{PP} (composite) R_L = 400 Ω

Figure 6-7. Intermodulation Distortion vs Frequency



V_{G+} = 1 V V_O = 1 V_{PP} R_L = 400 Ω

Figure 6-8. Harmonic Distortion vs Frequency

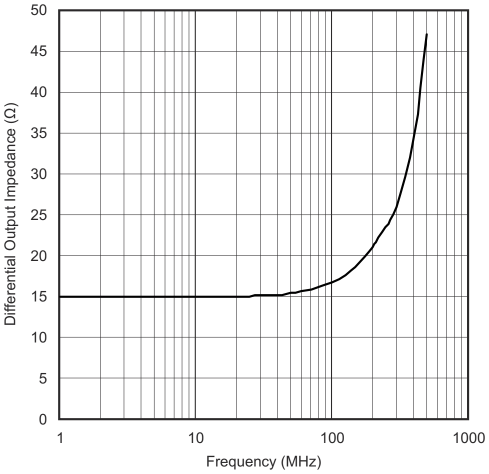


Figure 6-9. Differential Output Impedance of Main Amplifier vs Frequency

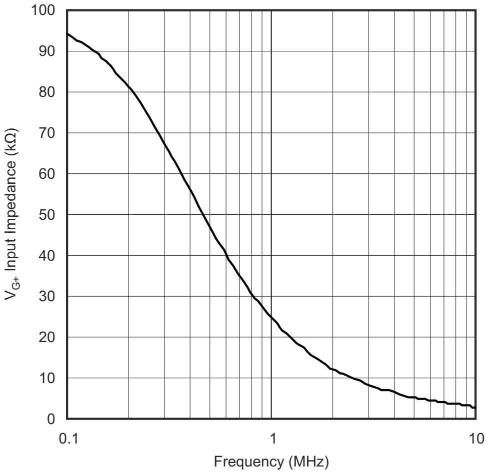


Figure 6-10. V_{G+} Input Impedance vs Frequency

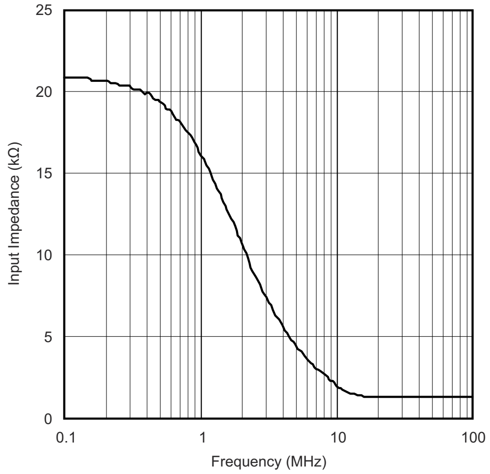


Figure 6-11. V_{OCM} Input Impedance vs Frequency

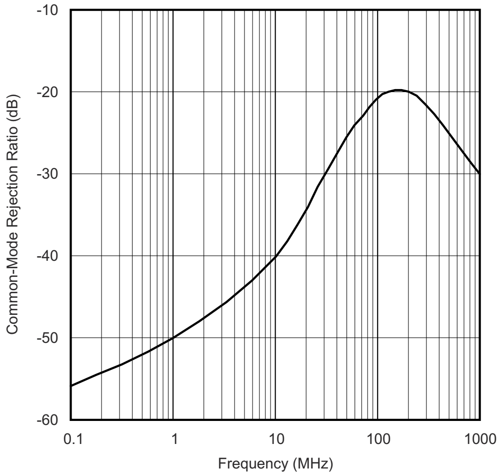
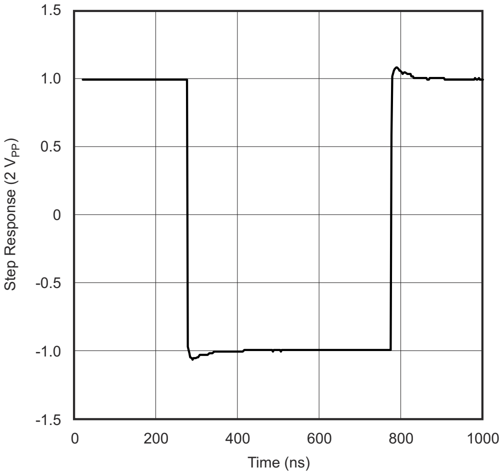
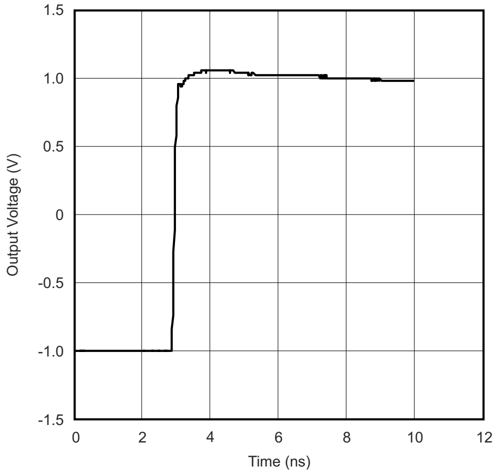


Figure 6-12. Common-Mode Rejection Ratio vs Frequency



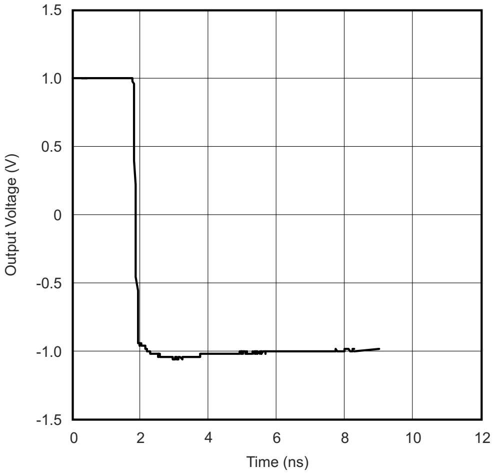
R_L = 400 Ω At amplifier output and minimum gain

Figure 6-13. Step Response



R_L = 400 Ω At amplifier output and minimum gain

Figure 6-14. Step Response: Rising Edge



R_L = 400 Ω At amplifier output and minimum gain

Figure 6-15. Step Response: Falling Edge

7 Parameter Measurement Information

7.1 Test Circuits

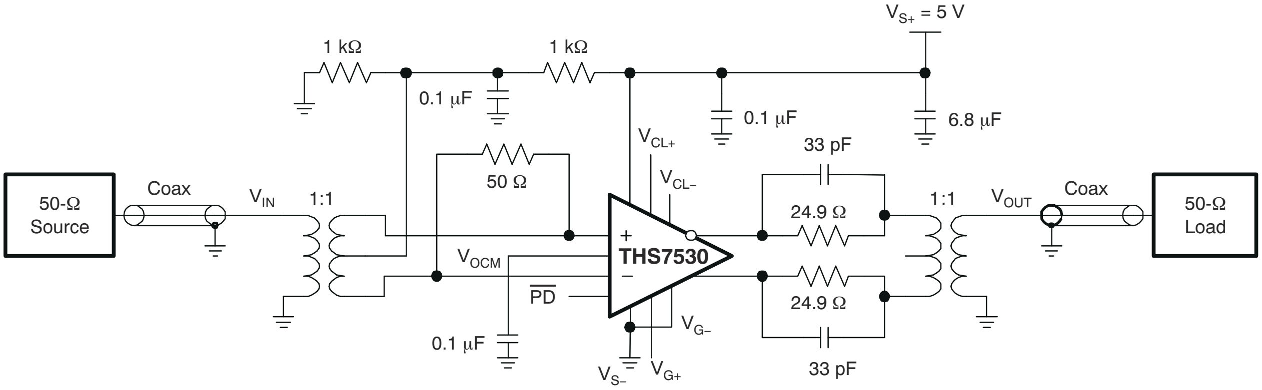


Figure 7-1. AC Test Circuit

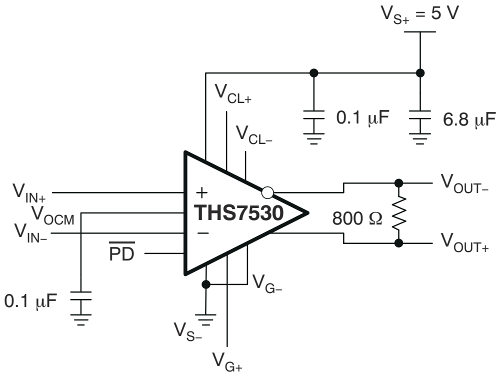


Figure 7-2. DC Test Circuit

8 Detailed Description

8.1 Overview

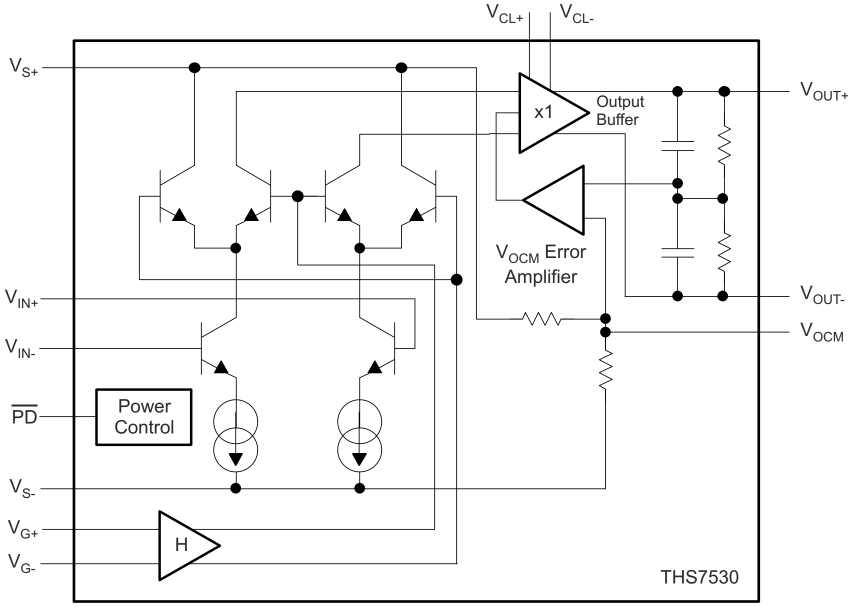
The THS7530 device is a fully-differential amplifier with 300-MHz bandwidth and with continually-variable gain from 11.6 dB to 46.5 dB. This amplifier together with an automatic gain control (AGC) circuit will precisely established a desired amplitude at its output.

The input architecture is a modified Gilbert cell. The output from the Gilbert cell is converted to a voltage and buffered to the output as a fully-differential signal. A summing node between the outputs is used to compare the output common-mode voltage to the V_{OCM} input. The V_{OCM} error amplifier then servos the output common-mode voltage to maintain it equal to the V_{OCM} input. Left unterminated, V_{OCM} is set to midsupply by internal resistors.

The gain control input is conditioned to give linear-in-dB gain control (block H). The gain control input is a differential signal from 0 V to 0.9 V which varies the gain from 11.6 dB to 46.5 dB.

V_{CL+} and V_{CL-} provide inputs that limit the output voltage swing of the amplifier.

8.2 Functional Block Diagram



8.3 Feature Description

The main features of the THS7530 device are continually-variable gain control, common-mode voltage control, output voltage clamps, and power-down mode.

8.3.1 Continually-Variable Gain Control

The amplifier gain in dB is a linear function of the gain control voltage, which has a range of 0 V to 0.9 V. The slope of the gain control input is 38.8 dB/V with a gain range of 11.6 dB to 46.5 dB, which is 3.8 to 211.3 V/V, respectively. The bandwidth of the gain control is 15 MHz, typically.

The gain control is a differential input to reduce noise due to ground bounce, coupling, and so forth. The negative gain-control input V_{G-} can be below the negative supply by as much as 600 mV.

8.3.2 Common-Mode Voltage Control

The common-mode voltage control sets the common-mode voltage of the differential output. The gain of the control voltage is 1 V/V with a range of 1.75 V to 3.25 V above the negative supply. If unconnected, the common-mode voltage control is at mid-supply, typically 2.5 V above the negative supply. The bandwidth of the common-mode voltage control is an impressive 32 MHz.

8.3.3 Output Voltage Clamps

Separate inputs, V_{CL-} and V_{CL+}, establish the minimum and maximum output voltages, respectively. The typical error of the output voltage compared to the clamp voltage is only 25 mV. This feature can be used to avoid saturating the inputs of a receiving device, thereby precluding long recovery times in the signal path.

8.3.4 Power-Down Mode

To minimize power consumption when idle, the THS7530 device has an active-low power-down control that reduces the quiescent current from 40 mA to 350 µA. The turnon delay is only 820 ns.

When in power-down mode, the THS7530 device has a 80-dB forward isolation to allow other devices to drive the same signal path with minimal interference from the idle THS7530 device.

8.4 Device Functional Modes

The THS7530 device has two functional modes: full-power mode and power-down mode. The power-down mode reduces the quiescent current of the device to 350 µA from a typical value of 40 mA.

With a turnon time of only 820 ns and a turnoff time of 500 ns, the power-down mode can be used to greatly reduce the average power consumption of the device without sacrificing system performance.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The THS7530 device is designed to work in a wide variety of applications requiring continuously variable gain and a fully-differential signal path. The common-mode voltage control and the output voltage clamps enable the THS7530 device to drive a diverse array of receiving circuits.

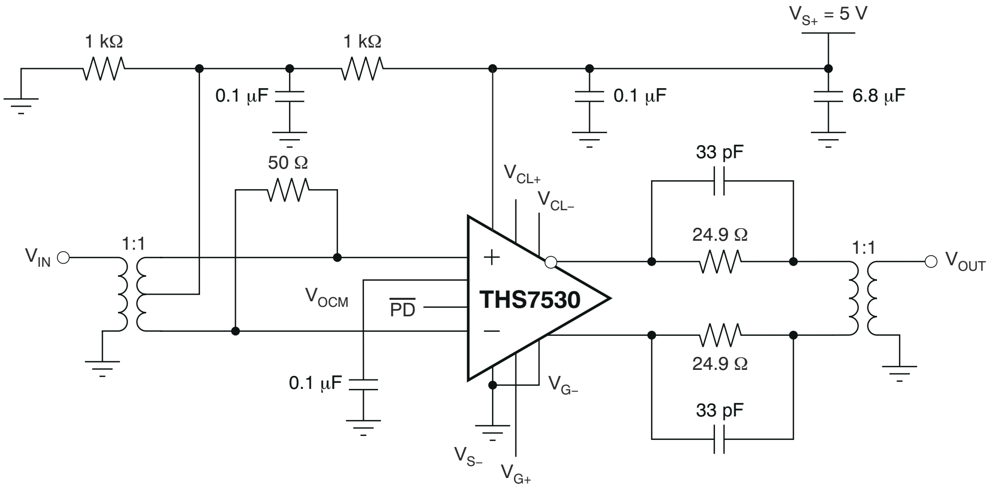


Figure 9-1. EVM Schematic: Designed for Use With Typical 50-Ω RF Test Equipment

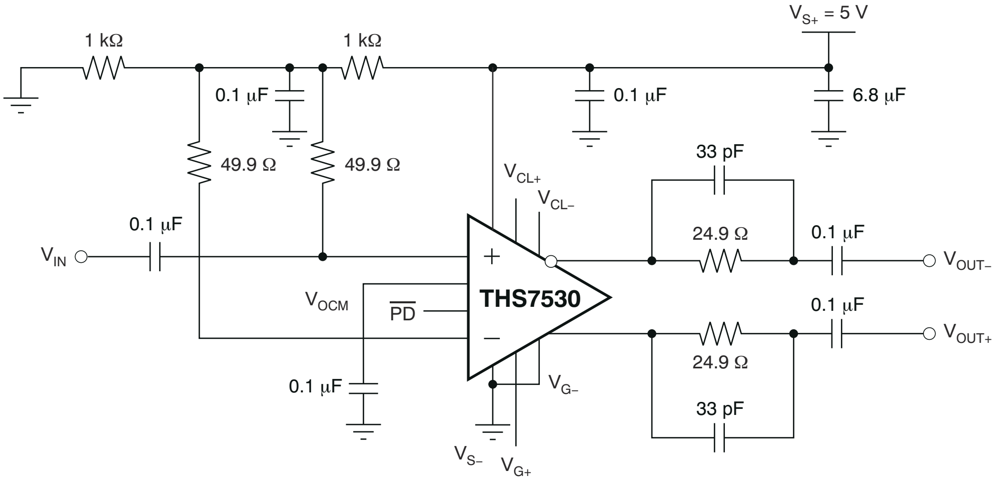


Figure 9-2. AC-Coupled Single-Ended Input With AC-Coupled Differential Output

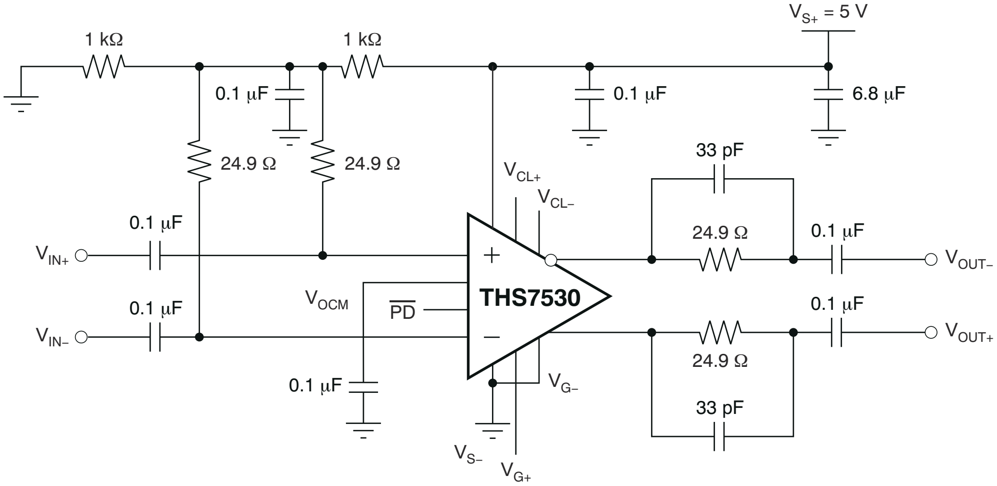


Figure 9-3. AC-Coupled Differential Input With AC-Coupled Differential Output

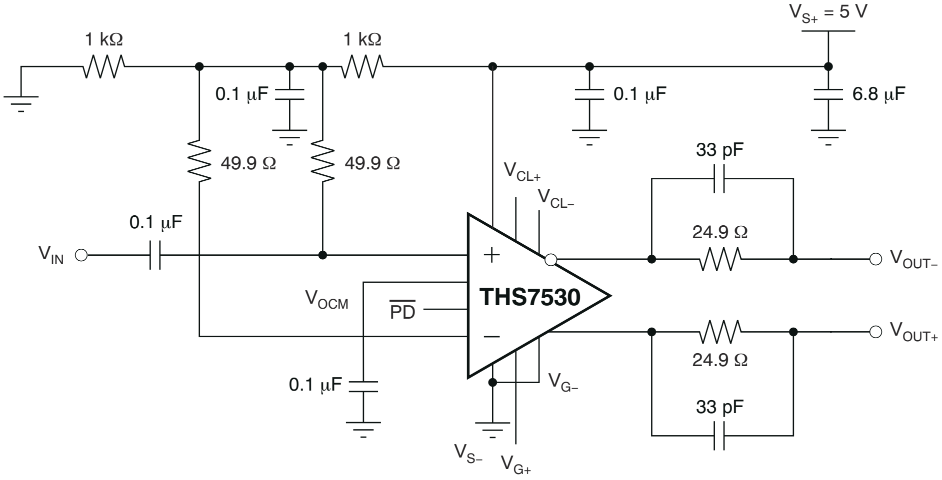


Figure 9-4. DC-Coupled Single-Ended Input With DC-Coupled Differential Output

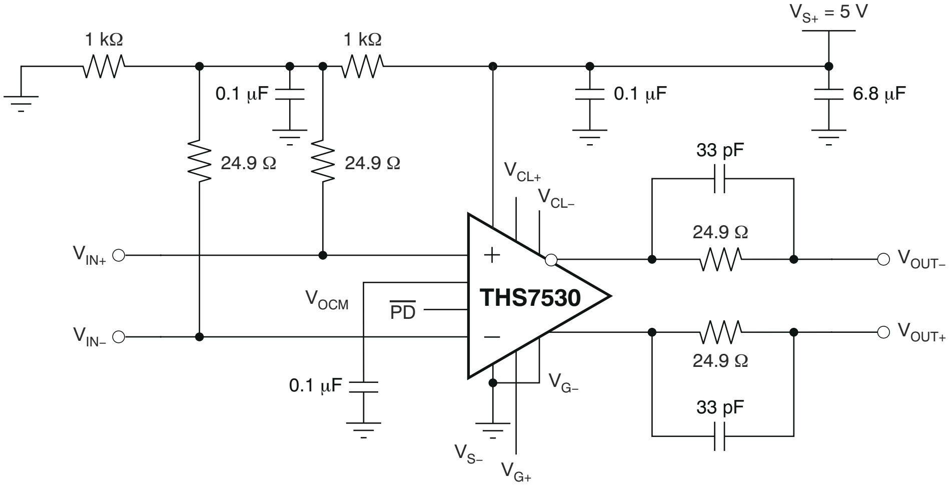


Figure 9-5. DC-Coupled Differential Input With DC-Coupled Differential Output

9.2 Typical Application

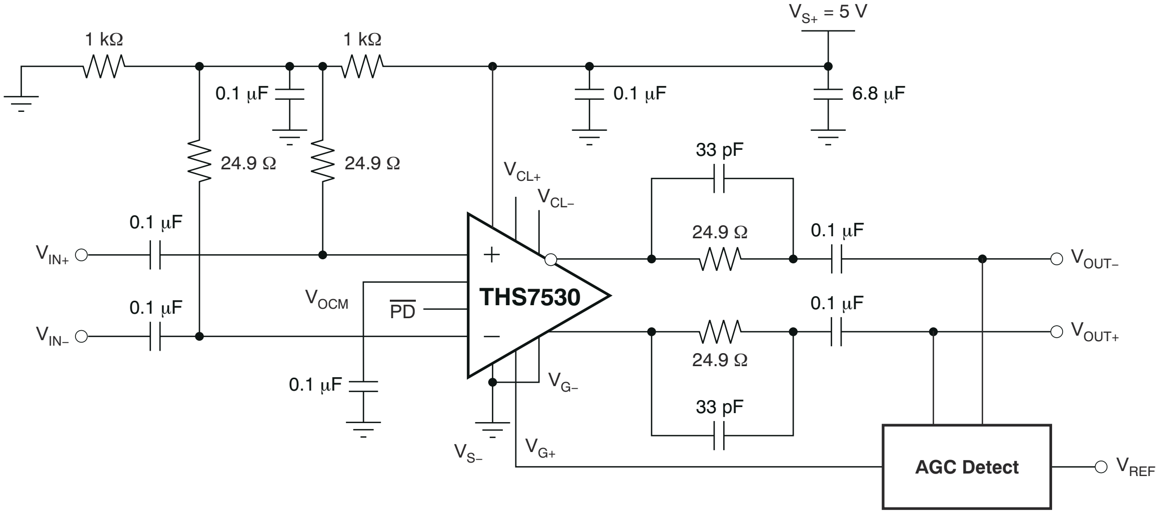


Figure 9-6. Typical Application Circuit

9.2.1 Design Requirements

A typical application circuit is shown in *Figure 9-6*. Two noteworthy aspects of this circuit are the customer's automatic gain control (AGC) circuit and the THS7530 input bias circuit.

The proper design of the AGC circuit is essential for the THS7530 device to operate properly in the customer's application. The method of detecting the amplitude of the differential output of the THS7530 device and creating the gain-control voltage, V_{G+}, from the detected amplitude and the reference amplitude, V_{ref}, are application-specific and beyond the scope of this document. The bandwidth of the amplitude of the THS7530 amplitude control is 15 MHz, which allows for rapid corrections of amplitude errors but which also allows noise from DC to 15 MHz to create an amplitude error. The trade-off between rapid amplitude correction and amplitude modulation due to noise is an important design consideration.

The input bias currents of the differential inputs of the THS7530 device are typically 20 µA. When the differential inputs are AC-coupled, the bias currents must be supplied as shown in *Figure 9-6*. In this circuit, the DC bias voltage is mid-supply and the AC differential input impedance is 50 Ω. The 0.1-µF capacitor between the two 24.9-Ω resistors creates an AC ground for the driving circuit.

9.2.2 Detailed Design Procedure

The THS7530 device is designed for nominal 5-V power supply from V_{S+} to $V_{S–}$.

The amplifier has fully differential inputs, V_{IN+} and $V_{IN–}$, and fully differential outputs, V_{OUT+} and $V_{OUT–}$ The inputs are high impedance and outputs are low impedance. External resistors are recommended for impedance matching and termination purposes.

The inputs and outputs can be DC-coupled, but for best performance, the input and output common-mode voltage should be maintained at the midpoint between the two supply pins. The output common-mode voltage is controlled by the voltage applied to V_{OCM}. Left unterminated, V_{OCM} is set to midsupply by internal resistors. A 0.1-µF bypass capacitor should be placed between V_{OCM} and ground to reduce common-mode noise. The input common-mode voltage defaults to midrail when left unconnected. For voltages other than midrail, V_{OCM}must be biased by external means. V_{IN+} and $V_{IN–}$ both require a nominal 30-µA bias current for proper operation. Therefore, ensure equal input impedance at each input to avoid generating an offset voltage that varies with gain.

Voltage applied from $V_{G–}$ to V_{G+} controls the gain of the part with 38.8-dB/V gain slope. The input can be differential or single ended. $V_{G–}$ must be maintained within –0.6 V and 0.8 V of $V_{S–}$for proper operation. The negative gain input should typically be tied directly to the negative power supply.

V_{CL+} and $V_{CL–}$ are inputs that limit the output voltage swing of the amplifier. The voltages applied set an absolute limit on the voltages at the output. Input voltages at V_{CL+} and $V_{CL–}$ clamp the output, ensuring that neither output exceeds those values.

The power-down input is a TTL compatible input, referenced to the negative supply voltage. A logic low puts the THS7530 device in power-saving mode. In power-down mode the part consumes less than 1-mA current, the output goes high impedance, and a high amount of isolation is maintained between the input and output.

Power-supply bypass capacitors are required for proper operation. A 6.8-μF tantalum bulk capacitor is recommended if the amplifier is located far from the power supply and may be shared among other devices. A ceramic 0.1-μF capacitor is recommended within 0.1-in of the device power pin. The ceramic capacitors should be located on the same layer as the amplifier to eliminate the use of vias between the capacitors and the power pin.

Table 9-1. THS7530EVM Bill of Materials

ITEM NO.	DESCRIPTION	SIZE	REFERENCE DESIGNATOR	QTY	PART NUMBER
1	Bead, ferrite, 3 A, 80 Ω	1206	FB1	1	(Steward) HI1206N800R–00
2	Capacitor, tantalum, 6.8 mF, 35 V, 10%	D	C2	1	(AVX) TAJD685K035R
3	Capacitor, ceramic, 0.1 mF, X7R, 16V	508	C1	1	(AVX) 0508YC104KAT2A
5	Capacitor, ceramic, 0.1 mF, X7R, 50 V	805	C3, C7, C12, C13, C14, C15, C16, C17	8	(AVX) 08055C104KAT2A
6	Diode, Schottky, 20 V, 0.5 A	SOD-123	D1	1	(Diodes Inc.) B0520LW–7
7	Resistor, 10 Ω, 1/8 W, 1%	805	R24, R25, R26	3	(PHYCOMP) 9C08052A10R0FKHFT
8	Resistor, 24.9 Ω, 1/8 W, 1%	805	R9, R15	2	(PHYCOMP) 9C08052A24R9FKHFT
9	Resistor, 1 kΩ, 1.8W, 1%	805	R7, R12	2	(PHYCOMP) 9C08052A1001FKHFT
10	Resistor, 3.92 kΩ , 1/8 W, 1%	805	R1	1	(PHYCOMP) 9C08052A3921FKHFT
11	Resistor, 0 Ω, 1/4 W	1206	C4, C5	2	(PHYCOMP) 9C12063A0R00JLHFT
12	Resistor, 49.9 Ω, 1/4 W, 1%	1206	R4	1	(PHYCOMP) 9C12063A49R9FKRFT
13	Pot., ceramic, 1/4 inch square, 1 kΩ		R2	1	(Bourns) 3362P–1–102
14	Pot., ceramic, 1/4 inch square, 10 kΩ		R21, R22, R23	3	(Bourns) 3362P–1–103
15	IC, TLV2371	SOT-23	U2, U3, U4	3	(TI) TLV2371IDBVT
16	Transformer, 1:1	CD542	T1, T2	2	(Mini-Circuits) ADT1-1WT
17	Connector, edge, SMA PCB Jack		J3, J4	2	(Johnson) 142–0701–801
18	Jack, banana receptacle, 0.25-in diameter hole		J1, J2	2	(HH Smith) 101
19	Header, 0.1-in Ctrs, 0.025-in square pins	2 POS.	JP1	1	(Sullins) PZC36SAAN
20	Shunts		JP1	1	(Sullins) SSC02SYAN
21	Test point, black		TP2, TP3, TP4	3	(Keystone) 5001
22	Test points, red		TP1, TP8, TP9, TP10	4	(Keystone) 5000
23	Standoff, 4–40 Hex, 0.625-in Length			4	(Keystone) 1804
24	Screw, Phillips, 4–40, .250-in			4	SHR–0440–016–SN
25	IC, THS7530		U1	1	(TI) THS7530PWP
26	Board, printed circuit			1	(TI) EDGE # 6441987

9.2.3 Application Curves

Figure 9-7 and Figure 9-8 highlight the input characteristics of the THS7530 device that should be used to design the circuit driving the THS7530 device.

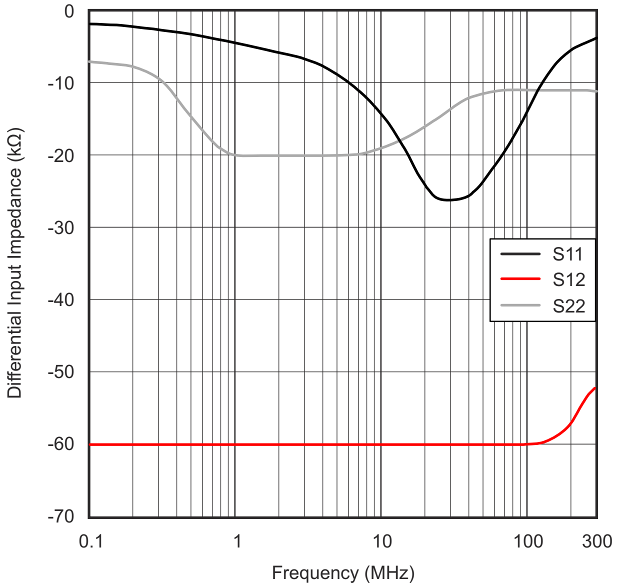


Figure 9-7. S-Parameters vs Frequency

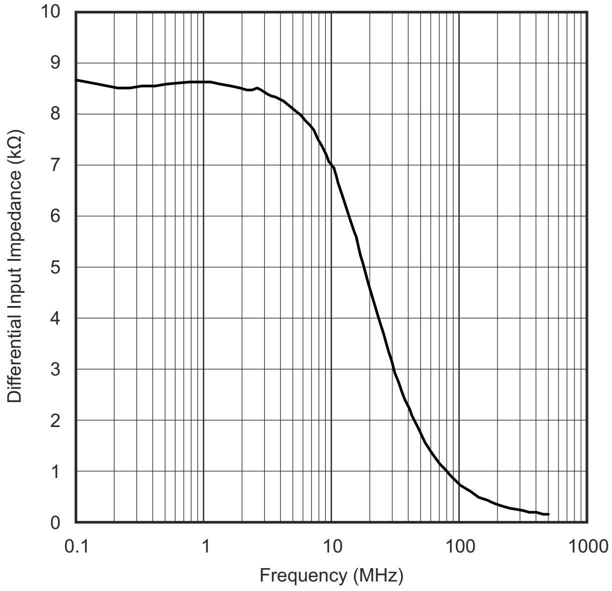


Figure 9-8. Differential Input Impedance of Main Amplifier vs Frequency

10 Power Supply Recommendations

The THS7530 device is principally intended to operate with a nominal single-supply voltage of 5 V. Supply voltage tolerances of ±10% are supported. The absolute maximum supply is 5.5 V.

Supply decoupling is required, as described in *Section 9*.

Split (or bipolar) supplies can be used with the THS7530 device, as long as the total value across the device remains less than 5.5 V (absolute maximum).

11 Layout

11.1 Layout Guidelines

The THS7530 device is available in a thermally-enhanced PowerPAD™ package. Figure 11-1 shows the recommended number of vias and thermal land size recommended for best performance. Thermal vias connect the thermal land to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow. The experiments conducted jointly with Solectron Texas indicate that a via drill diameter of 0.33 mm (13 mils, or .013 in) or smaller works well when 1-ounce copper is plated at the surface of the board and simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a dimension equal to the via diameter + 0.1 mm minimum. This prevents the solder from being wicked through the thermal via and potentially creating a solder void in the region between the package bottom and the thermal land on the surface of the PCB.

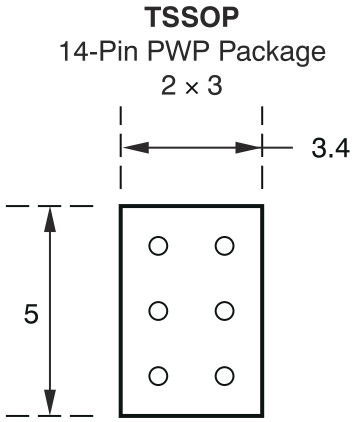


Figure 11-1. Recommended Thermal Land Size and Thermal Via Patterns (Dimensions in mm)

See TI's Technical Brief titled, *PowerPAD™ Thermally Enhanced Package* (SLMA002) for a detailed discussion of the PowerPAD™ package, its dimensions, and recommended use.

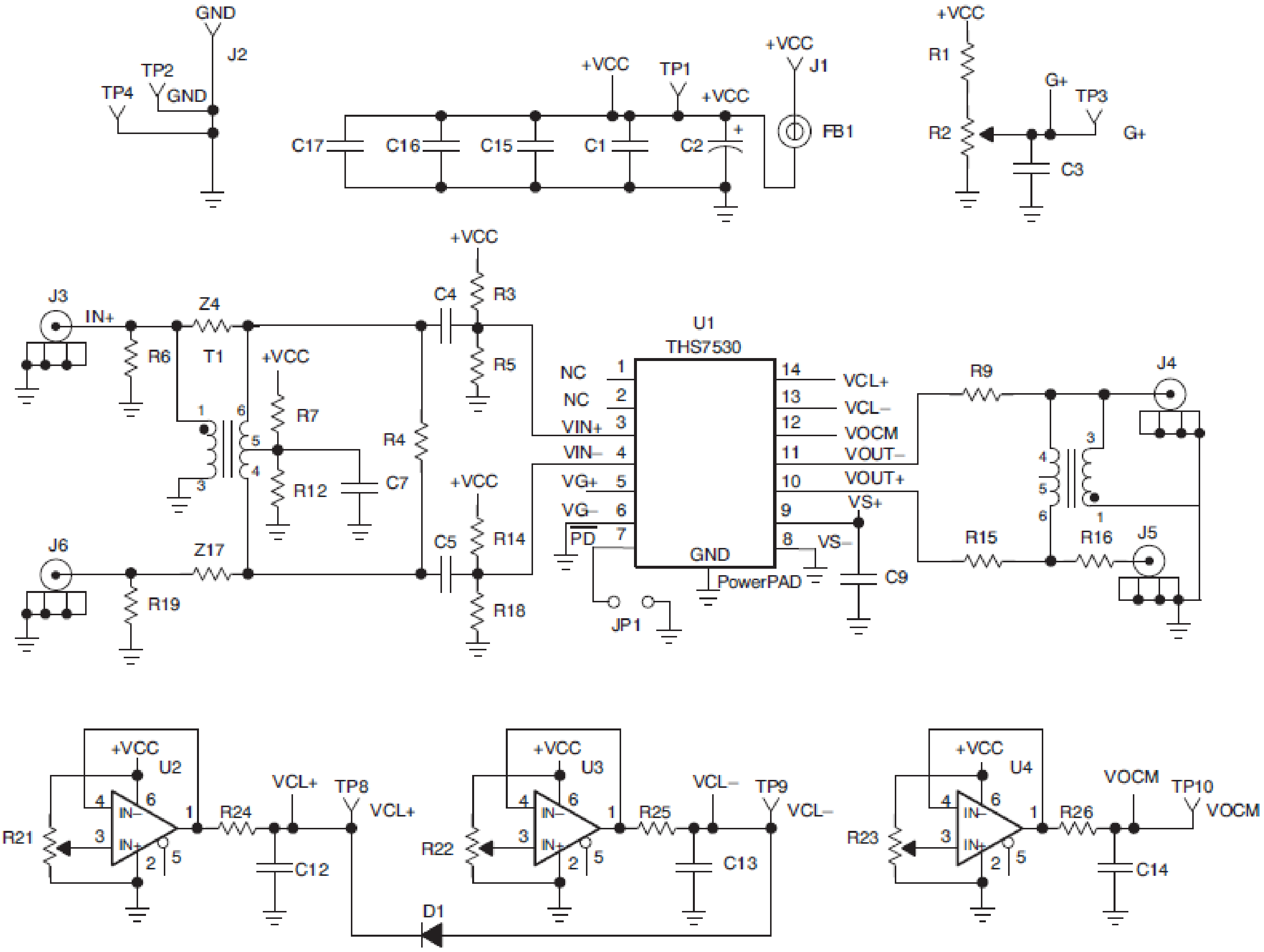
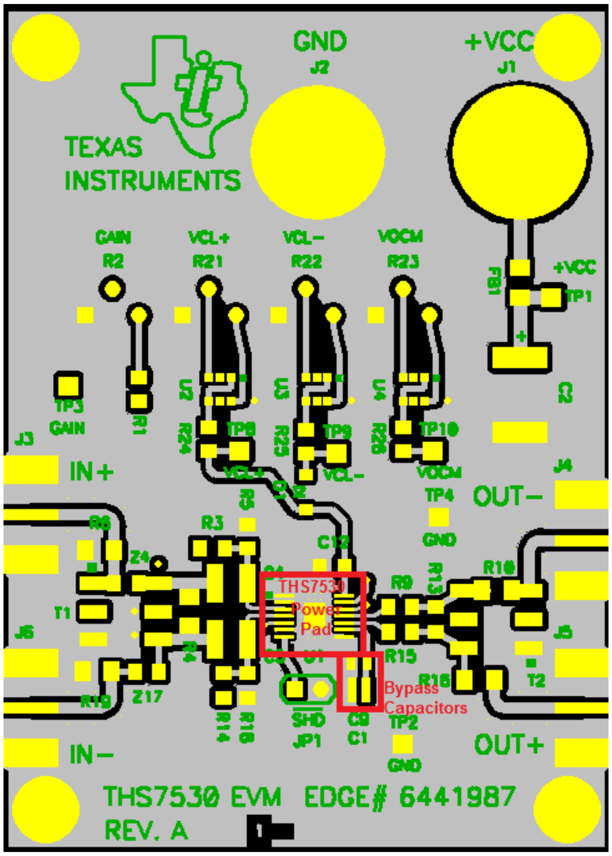


Figure 11-2. EVM Schematic

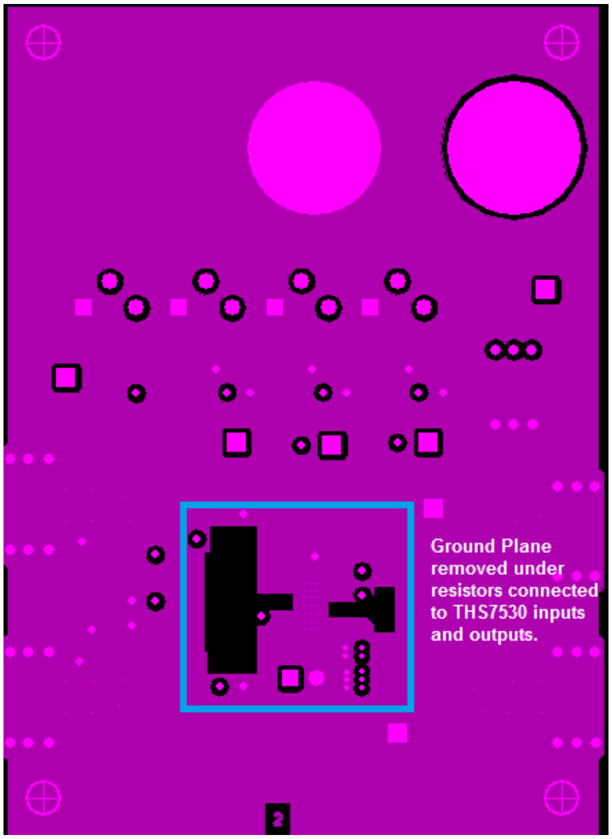
11.2 Layout Examples



THS7530 Power Pad

Bypass Capacitors

Figure 11-3. Layout Diagram (Top)



Ground Plane removed under resistors connected to THS7530 inputs and outputs.

Figure 11-4. Layout Diagram (Ground)

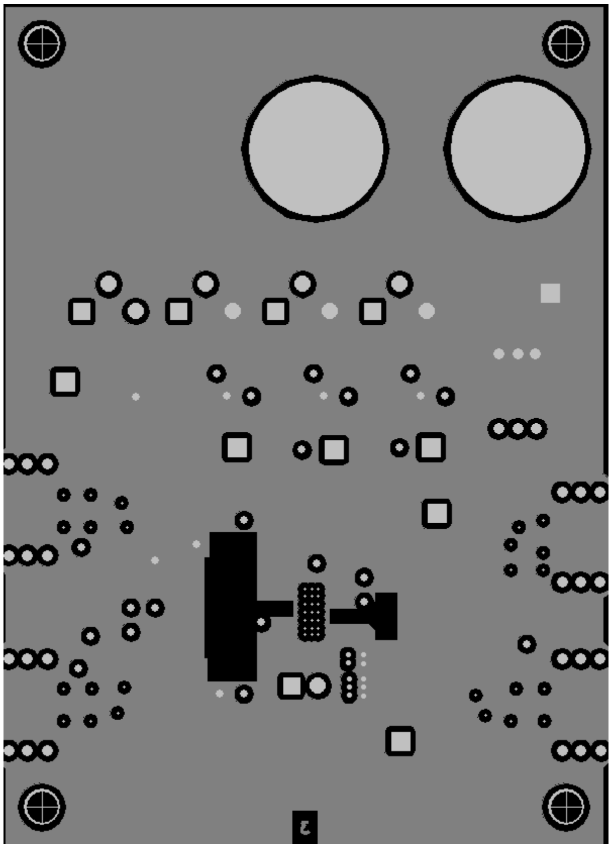


Figure 11-5. Layout Diagram (Power)

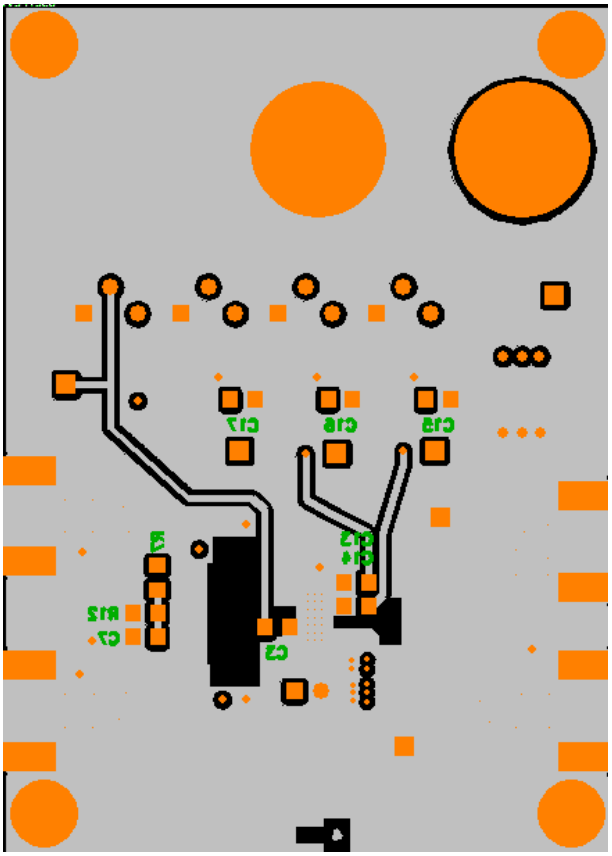


Figure 11-6. Layout Diagram (Bottom)

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Development Support

For the THS7530 PSpice Model, see SLOJ139.

For the THS7530 TINA-TI Spice Model, see SLAM020.

For the THS7530 TINA-TI Reference Design, see SLAC091.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- *THS7530 EVM Users Guide*, SLOU161
- *Noise Analysis for High-Speed Op Amps*, SBOA066
- *TI's Analog Signal Chain Guide*, SLYB174
- *PowerPAD™ Thermally Enhanced Package*, SLMA002
- *PowerPAD™ Made Easy*, SLMA004

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS7530PWP	Active	Production	HTSSOP (PWP) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7530
THS7530PWP.B	Active	Production	HTSSOP (PWP) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7530
THS7530PWPR	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7530
THS7530PWPR.B	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7530

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF THS7530 :

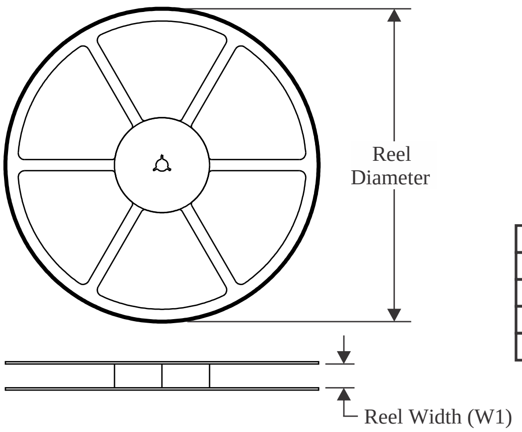
- Automotive : THS7530-Q1

NOTE: Qualified Version Definitions:

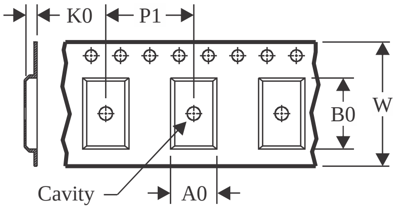
  - Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

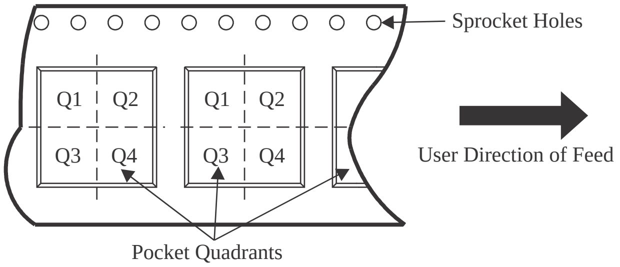


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

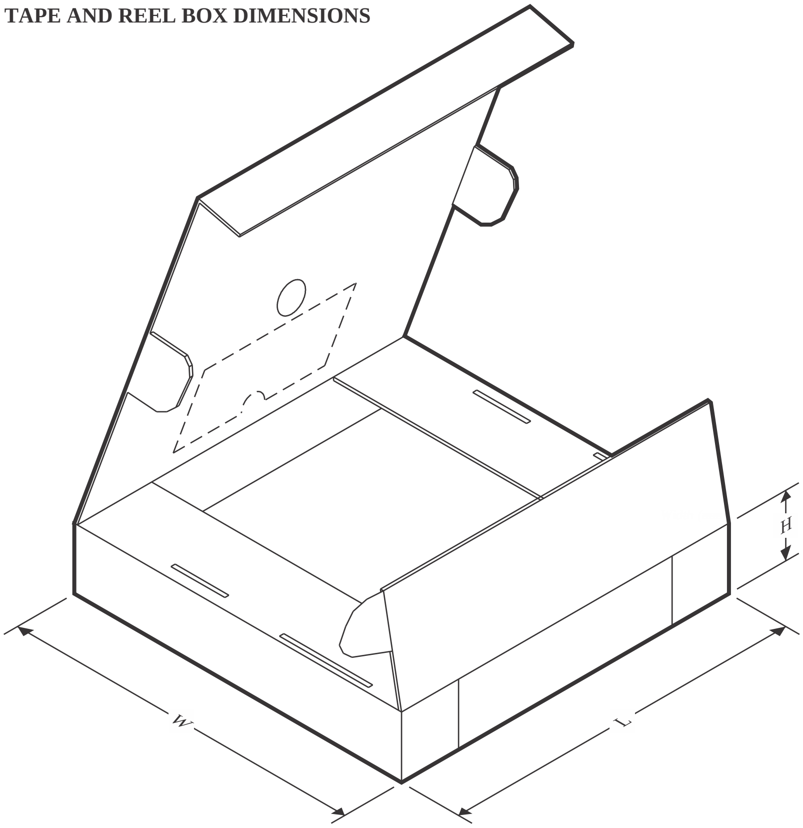
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7530PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

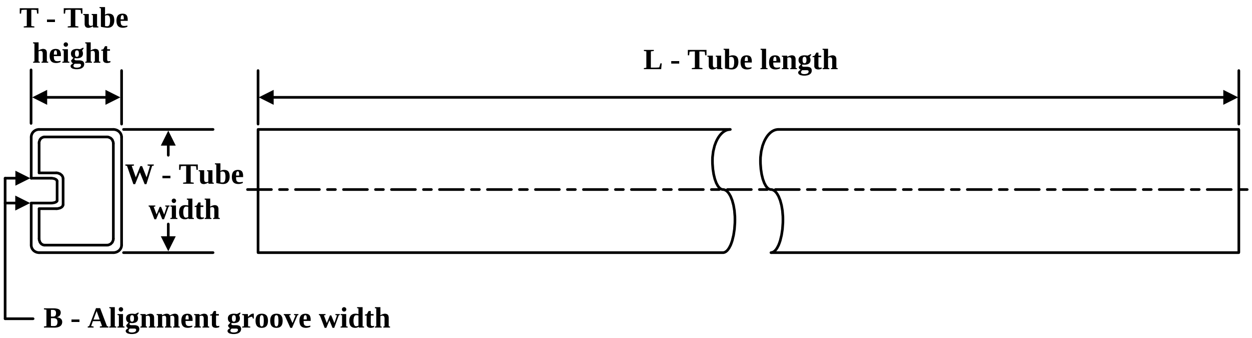
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7530PWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS7530PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5
THS7530PWP.B	PWP	HTSSOP	14	90	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

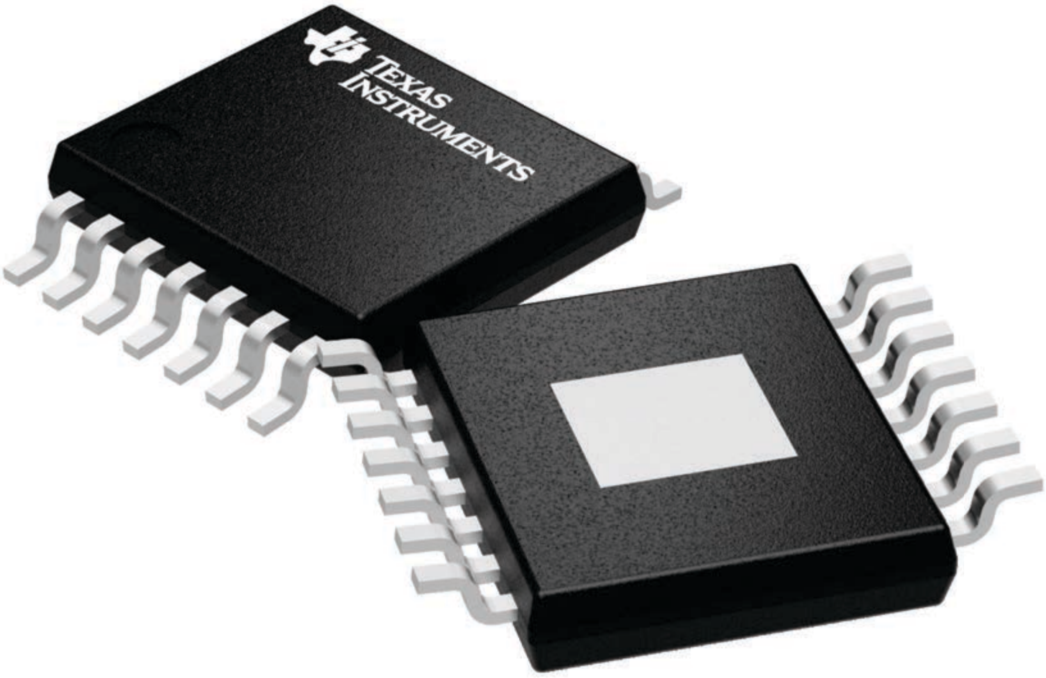
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

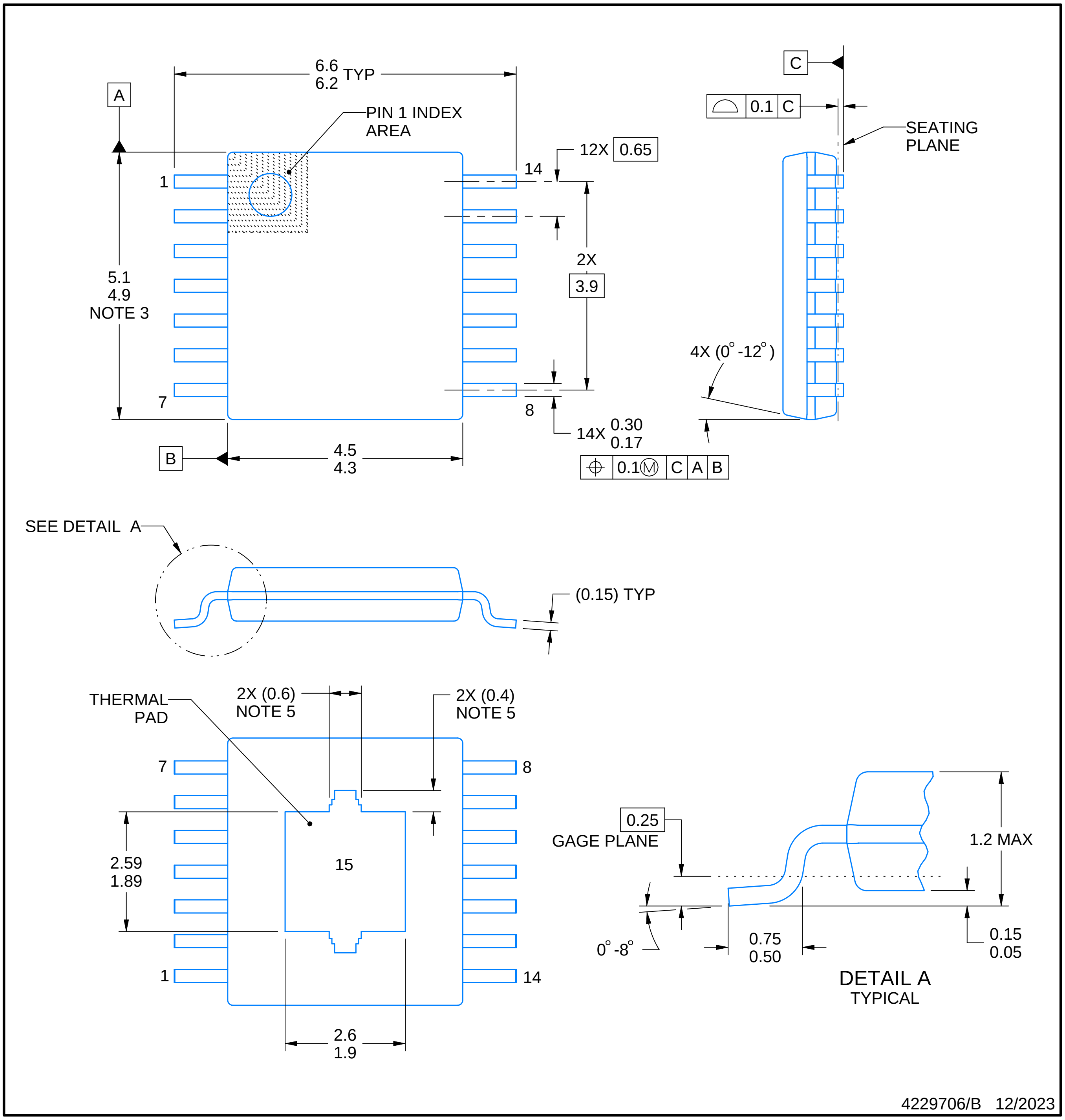


PACKAGE OUTLINE

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

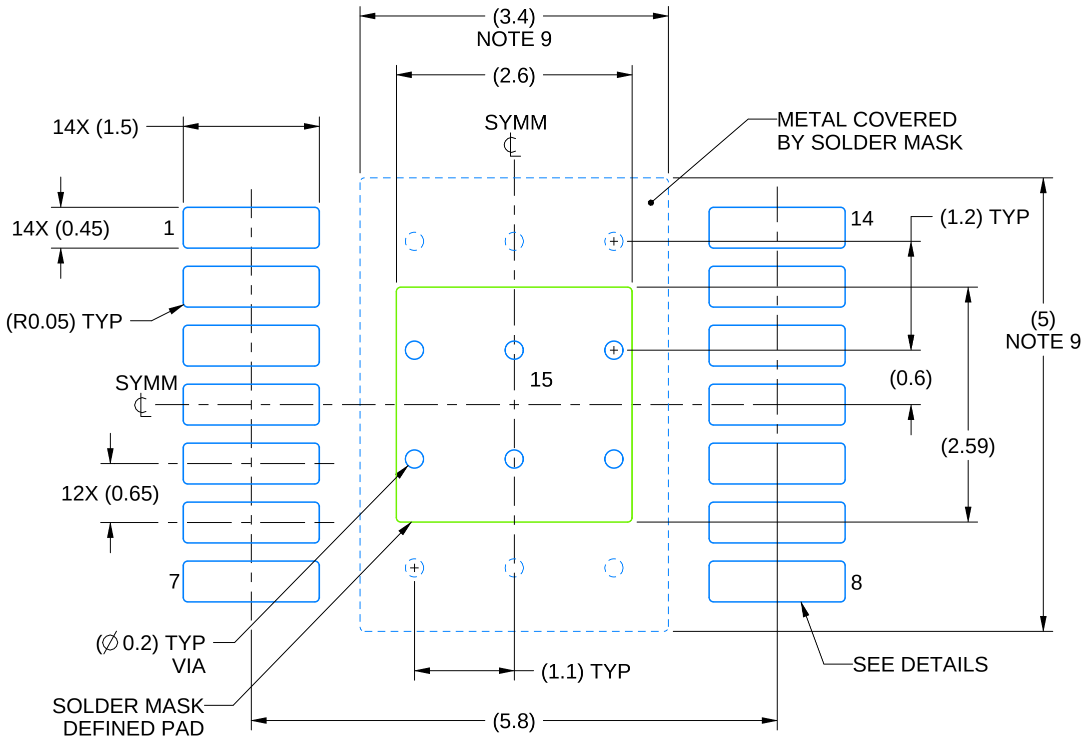
SMALL OUTLINE PACKAGE



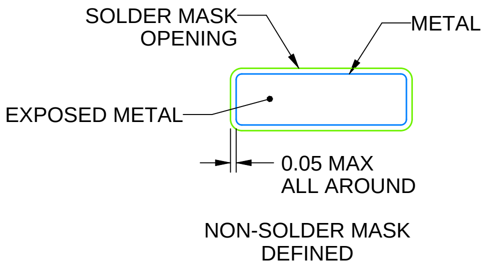
PowerPAD is a trademark of Texas Instruments.

NOTES:

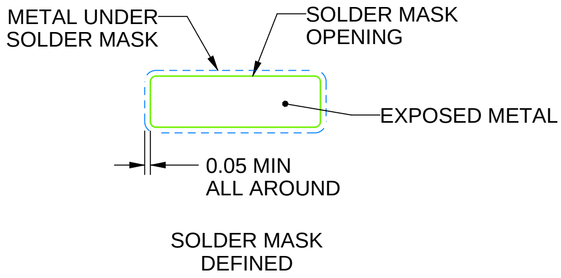
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



NON-SOLDER MASK
DEFINED

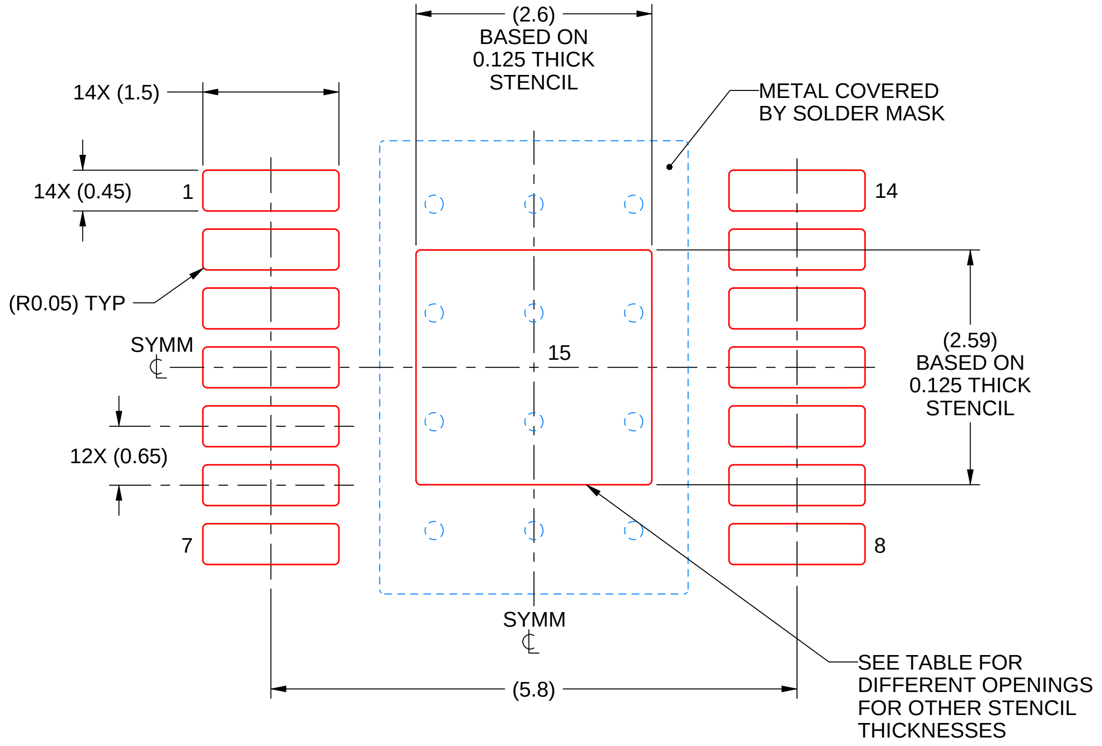


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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