



Z86E61/E63

CMOS Z8® 16K/32K EPROM MICROCONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller
- 40-Pin DIP, 44-Pin PLCC Style Packages
- 4.5V to 5.5V Operating Range
- Clock Speeds: 16 and 20 MHz
- Low Power Consumption: 275 mW (max)
- Fast Instruction Pointer: 1.0 ms @ 12 MHz
- Two Standby Modes: STOP and HALT
- 32 Input/Output Lines
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- High Voltage Protection on High Voltage Inputs
- RAM and EPROM Protect
- EPROM: 16 Kbytes Z86E61
32 Kbytes Z86E63
- 256 Bytes Register File
 - 236 Bytes of General-Purpose RAM
 - 16 Bytes of Control and Status Registers
 - 4 Bytes for Ports
- Two Programmable 8-Bit Counter/Timers Each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Eight Different Sources
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive

GENERAL DESCRIPTION

The Z86E61/E63 microcontrollers are members of the Z8® single-chip microcontroller family with 16K/32 Kbytes of EPROM and 236 bytes of general-purpose RAM. Offered in 40-pin DIP or 44-pin PLCC package styles, these devices are pin-compatible EPROM versions of the Z86C61/63. The ROMless pin option is available on the 44-pin versions only.

With 4 Kbytes of ROM and 236 bytes of general-purpose RAM, the Z86E61/E63 offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

For applications demanding powerful I/O capabilities, the Z86E61/E63 offers 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

The Z86E61/E63 can address both external memory and preprogrammed ROM, making it well suited for high-volume applications or where code flexibility is required.

PIN DESCRIPTION

Standard Mode

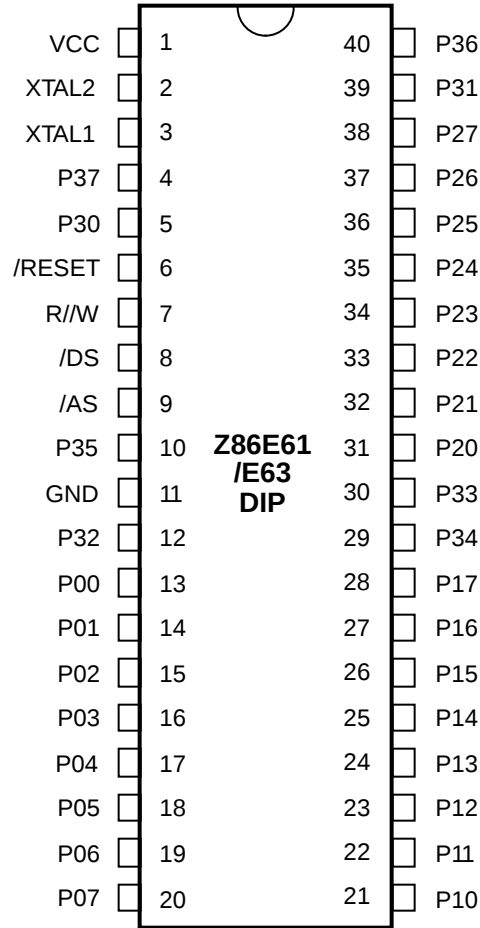


Table 1. 40-Pin DIP Pin Identification

Standard Mode			
Pin #	Symbol	Function	Direction
1	V _{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	/RESET	Reset	Input
7	R/W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3, Pin 5	Output
11	GND	Ground	Input
12	P32	Port 3, Pin 2	Input
13-20	P07-P00	Port 0, Pins 0, 1, 2, 3, 4, 5, 6, 7	In/Output
21-28	P17-P10	Port 1, Pins 0, 1, 2, 3, 4, 5, 6, 7	In/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P27-P20	Port 2, Pins 0, 1, 2, 3, 4, 5, 6, 7	In/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

Figure 2. 40-Pin DIP Pin Configuration

PIN DESCRIPTION (Continued)

Standard Mode

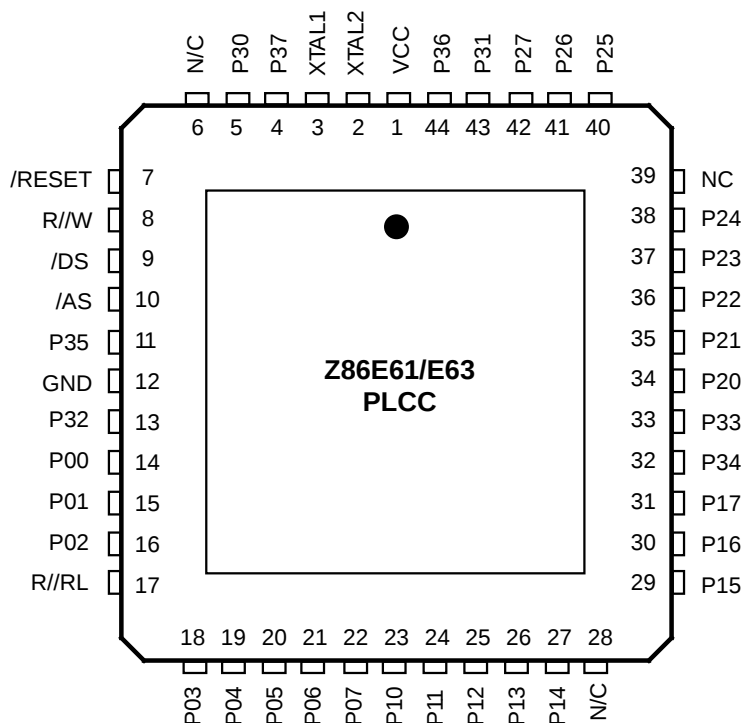


Figure 3. 44-Pin PLCC Pin Configuration

Table 2. 44-Pin PLCC Pin Identification

Standard Mode				Standard Mode			
Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	V _{CC}	Power Supply	Input	14-16	P02-P00	Port 0, Pins 0,1,2	In/Output
2	XTAL2	Crystal, Osc. Clock	Output	17	R//RL	ROM/ROMless control	Input
3	XTAL1	Crystal, Osc. Clock	Input	18-22	P07-P03	Port 0, Pins 3,4,5,6,7	In/Output
4	P37	Port 3, Pin 7	Output	23-27	P10-P14	Port 1, Pins 0,1,2,3,4	In/Output
5	P30	Port 3, Pin 0	Input	28	N/C	Not Connected	Input
6	N/C	Not Connected	Input	29-31	P17-P15	Port 1, Pins 5,6,7	In/Output
7	/RESET	Reset	Input	32	P34	Port 3, Pin 4	Output
8	R/W	Read/Write	Output	33	P33	Port 3, Pin 3	Input
9	/DS	Data Strobe	Output	34-38	P24-P20	Port 2, Pins 0,1,2,3,4	In/Output
10	/AS	Address Strobe	Output	39	N/C	Not Connected	Input
11	P35	Port 3, Pin 5	Output	40-42	P27-P25	Port 2, Pins 5,6,7	In/Output
12	GND	Ground	Input	43	P31	Port 3, Pin 1	Input
13	P32	Port 3, Pin 2	Input	44	P36	Port 3, Pin 6	Output

PIN DESCRIPTION

EPROM Mode

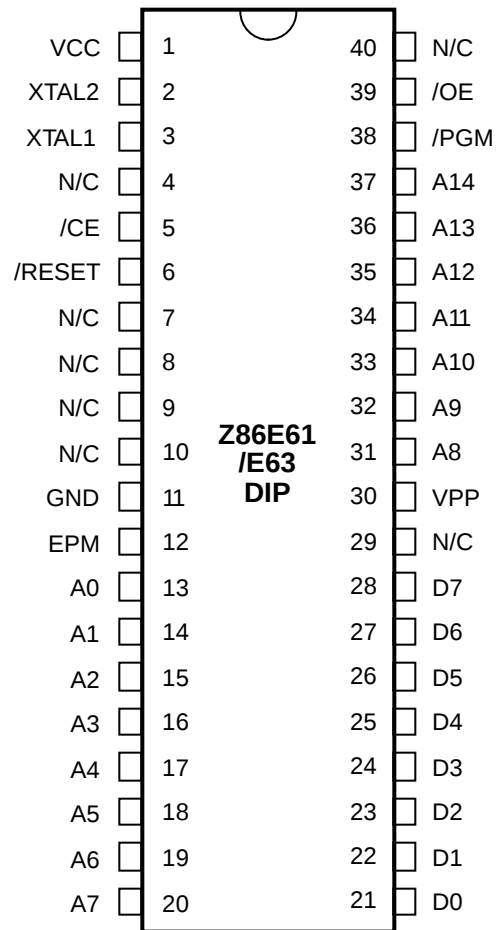


Table 3. 40-Pin DIP Pin Identification

EPROM Mode			
Pin #	Symbol	Function	Direction
1	V _{CC}	Power Supply	Input
2	XTAL2	Crystal, Osc. Clock	Output
3	XTAL1	Crystal, Osc. Clock	Input
4	N/C	Not Connected	Input
5	/CE	Chip Enable	Input
6	/RESET	Reset	Input
7-10	N/C	Not Connected	Input
11	GND	Ground	Input
12	EPM	EPROM Prog Mode	Input
13-20	A7-A0	Address 0,1,2,3,4,5,6,7	Input
21-28	D7-D0	Data 0,1,2,3,4,5,6,7	In/Output
29	N/C	Not Connected	Input
30	V _{PP}	Prog Voltage	Input
31-37	A14-A8	Address 8,9,10,11,12,13,14	Input
38	/PGM	Prog Mode	Input
39	/OE	Output Enable	Input
40	N/C	Not Connected	Input

Figure 4. 40-Pin DIP Pin Configuration

PIN DESCRIPTION (Continued)

EPROM Mode

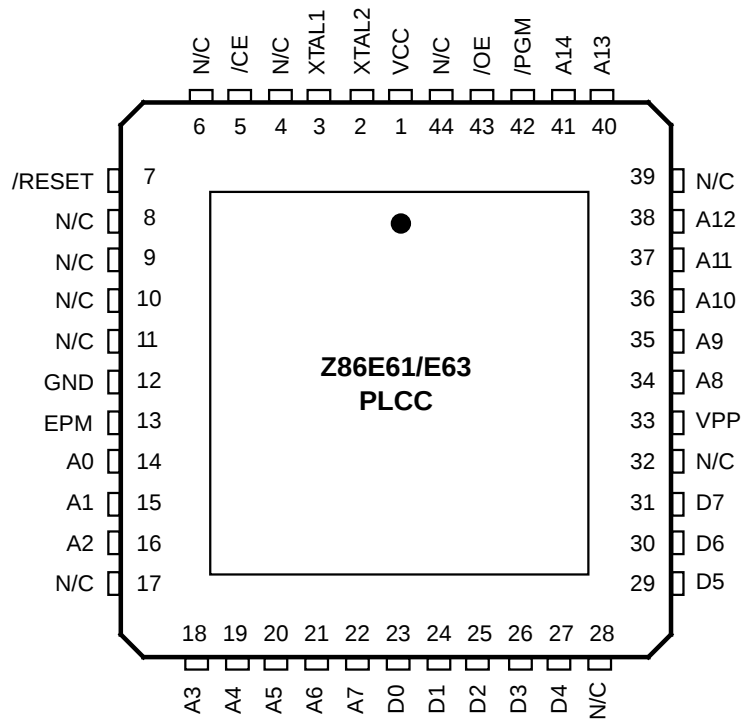


Figure 5. 44-Pin PLCC Pin Configuration

Table 4. 44-Pin PLCC Pin Identification

EPROM Mode Pin #	Symbol	Function	Direction	EPROM Mode Pin #	Symbol	Function	Direction
1	V _{CC}	Power Supply	Input	18-22	A7-A3	Address 3,4,5,6,7	Input
2	XTAL2	Crystal, Osc. Clock	Input	23-27	D4-D0	Data 0,1,2,3,4	In/Output
3	XTAL1	Crystal, Osc. Clock	Input	28	N/C	Not Connected	Input
4	N/C	Not Connected	Input	29-31	D7-D5	Data 5,6,7	In/Output
5	/CE	Chip Enable	Input	32	N/C	Not Connected	Input
6	N/C	Not Connected	Input	33	V _{PP}	Prog Voltage	Input
7	/RESET	Reset	Input	34-38	A12-A8	Address 8,9,10,11,12	Input
8-11	N/C	Not Connected	Input	39	N/C	Not Connected	Input
12	GND	Ground	Input	40-41	A13-A14	Address 13, 14	Input
13	EPM	EPROM Prog Mode	Input	42	/PGM	Prog Mode	Input
14-16	A0-A2	Address 0,1,2	Input	43	/OE	Output Enable	Input
17	N/C	Not Connected	Input	44	N/C	Not Connected	Input

PIN FUNCTIONS

ROMless (input, active Low). Connecting this pin to GND disables the internal ROM and forces the device to function as a Z86C91 ROMless Z8 (see the Z86C91 product specification for more information). When left unconnected or pulled High to V_{CC} , the device functions as a normal Z86E61/E63 EPROM version. **Note:** This pin is only available on the 44-pin versions of the Z86E61/E63.

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL2, XTAL1 *Crystal 2, Crystal 1* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R/W (output, write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86E61/E63 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. When /RESET is deactivated, program execution begins at location 000C (HEX). Power-up reset time must be held low for 50 ms, or until V_{CC} is stable, whichever is longer.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines

can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibbles) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode (Figure 8).

Port 1 (P17-P10). Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. For Z86E61/E63, these eight I/O lines can be programmed as input or output lines or are configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 can be placed under handshake control. In this configuration, Port 3 lines, P33 and P34, are used as the handshake controls RDY1 and /DAV1.

Memory locations greater than 16384 (E61) or 32768 (E63) are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in high-impedance state along with Port 0, /AS, /DS, and R/W, allowing the MCU to share common resources in multiprocessor and DMA applications. Data transfers are controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus Request output (Figure 9).

PIN FUNCTIONS (Continued)

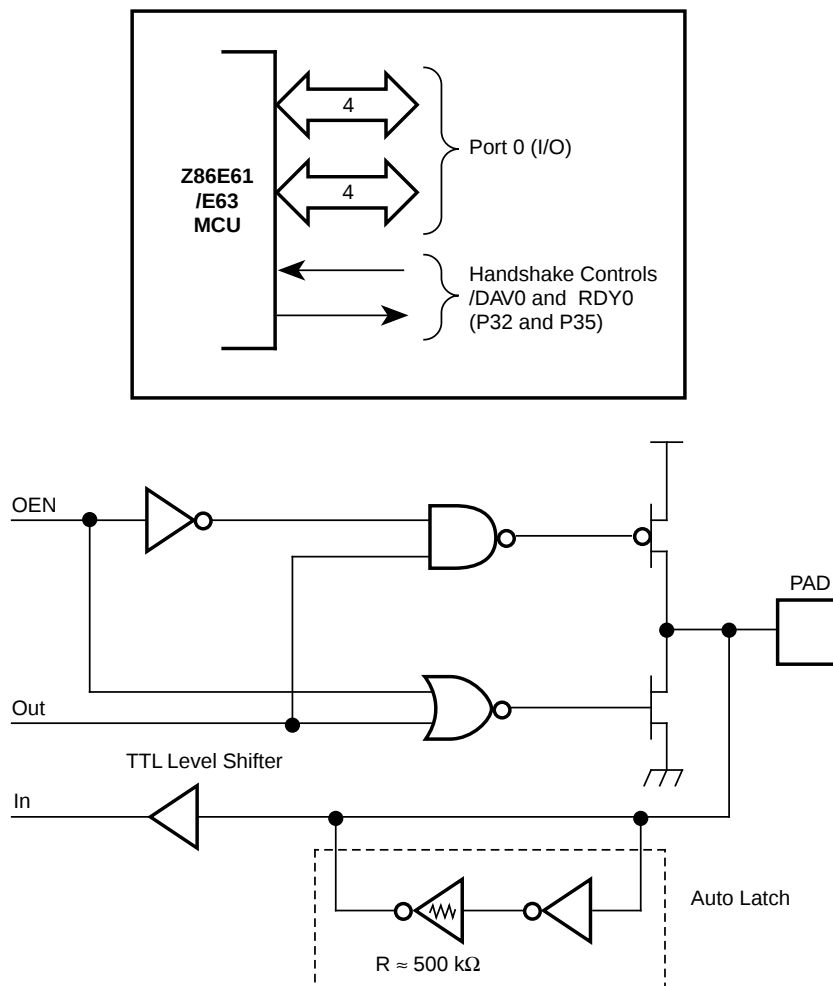


Figure 6. Port 0 Configuration

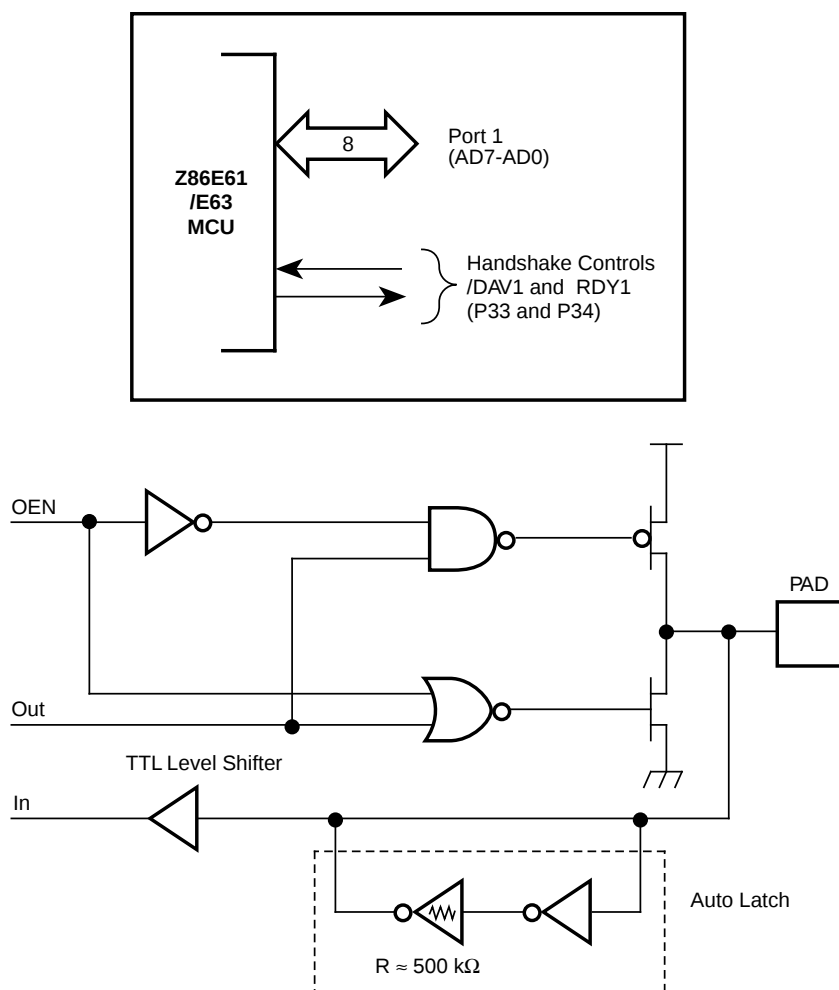


Figure 7. Port 1 Configuration

PIN FUNCTIONS (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bi-directional, CMOS compatible port. Each of these eight I/O lines can be independently programmed as an input or output, or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 can be placed under handshake control. In this

configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27 (Figure 8 and Table 5).

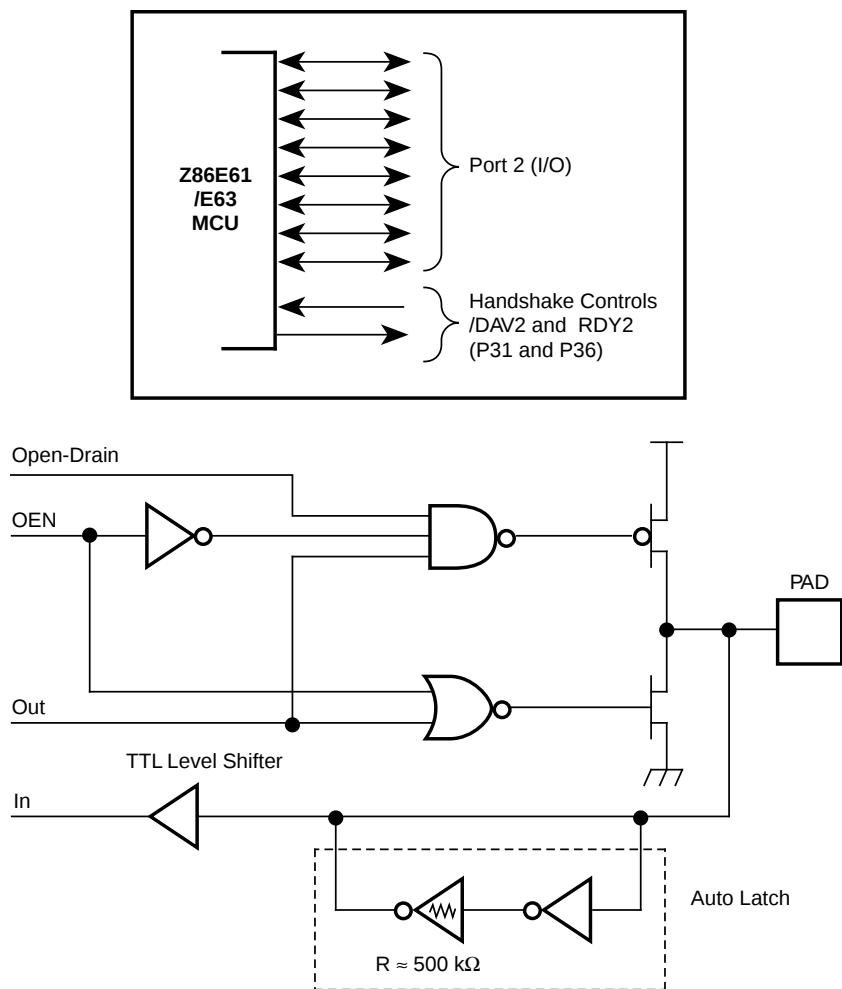


Figure 8. Port 2 Configuration

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33-P30) input and four-fixed (P37-P34)

output ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively (Figure 9).

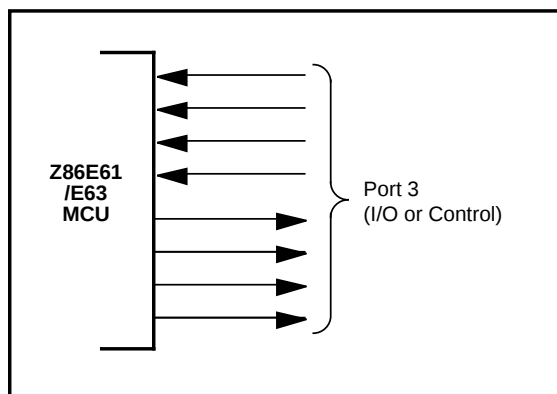


Figure 9. Port 3 Configuration

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals

(IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT}), Data Memory Select (/DM) and EPROM control signals (P30 = /CE, P31 = /OE, P32 = EPM and P33 = V_{PP}).

Table 5. Port 3 Pin Assignments

Pin	I/O	CTC1	Int.	P0 HS	P1 HS	P2 HS	UART	Ext	EPROM
P30	IN	T_{IN}	IRQ3	D/R	D/R	D/R	Serial In		/CE
P31	IN		IRQ2						/OE
P32	IN		IRQ0						EPM
P33	IN		IRQ1						V_{PP}
P34	OUT	T_{OUT}		R/D	R/D	R/D	Serial Out	DM	
P35	OUT								
P36	OUT								
P37	OUT								
T0			IRQ4						
T1			IRQ5						

Notes:

HS = Handshake Signals

D = Data Available

R = Ready

UART OPERATION

Port 3 lines, P37 and P30, are programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/Timer0.

The Z86E61/E63 automatically adds a start bit and two stop bits to transmitted data (Figure 10). Odd parity is also available as an option. Eight data bits are always transmit-

ted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits, and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

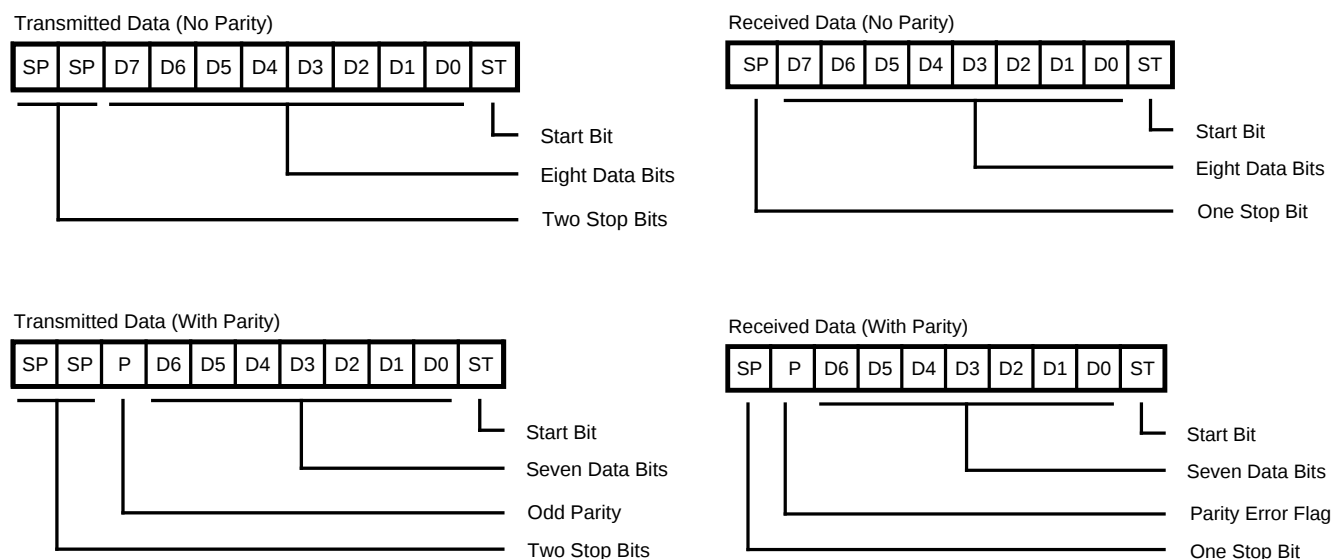


Figure 10. Serial Data Formats

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source.

Note: P33-P30 inputs differ from the Z86C61/C63 in that there is no clamping diode to V_{CC} because of the EPROM high voltage detection circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode

ADDRESS SPACE

Program Memory. The Z86E61/E63 can address 48 Kbytes (E61) or 32 Kbytes (E63) of external program memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 13 to byte

16383 (E61) or 32767 (E63) consists of on-chip EPROM. At addresses 16384 (E61) or 32768 (E63) and above, the Z86E61/E63 executes external program memory fetches. In ROMless mode, the Z86E61/E63 can address up to 64 Kbytes of program memory. Program execution begins at external location 000C (HEX) after a reset.

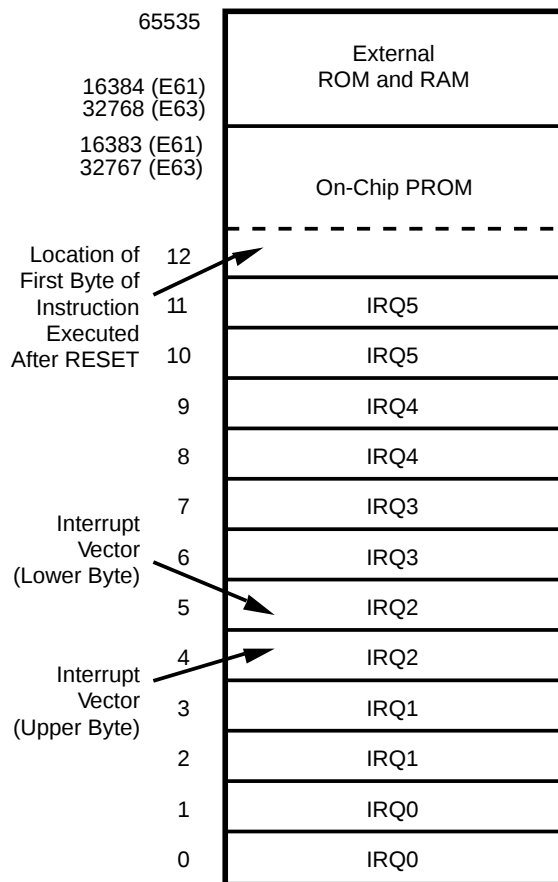


Figure 11. Program Memory Configuration

Data Memory (/DM). The EPROM version can address up to 48 Kbytes (E61) or 32 Kbytes (E63) of external data memory space beginning at location 16384 (E61) or 32768 (E63). The ROMless version can address up to 64 Kbytes of external data memory. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 12). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

Register File. The register file consists of four I/O port registers, 236 general-purpose registers, and 16 control and status registers (Figure 13). The instructions can

access registers directly or indirectly through an 8-bit address field. The Z86E61/E63 also allows short 4-bit register addressing using the Register Pointer (Figure 14). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Stack. The Z86E61/E63 has a 16-bit Stack Pointer (R255-R254) used for external stacks that reside anywhere in the data memory for the ROMless mode, but only from 16384 (E61) or 32768 (E63) to 65535 in the EPROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239-R4). The high byte of the Stack Pointer (SPH Bits 15-8) can be use as a general purpose register when using internal stack only.

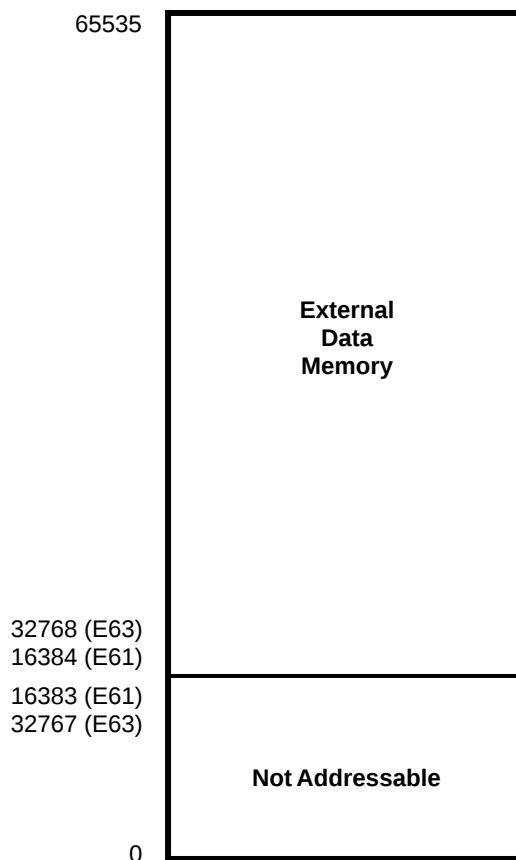


Figure 12. Data Memory Configuration

ADDRESS SPACE (Continued)

LOCATION		IDENTIFIERS
R255	Stack Pointer (Bits 7-0)	SPL
R254	Stack Pointer (Bits 15-8)	SPH
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Ports 0-1 Mode	P01M
R247	Port 3 Mode	P3M
R246	Port 2 Mode	P2M
R245	T0 Prescaler	PRE0
R244	Timer/Counter0	T0
R243	T1 Prescaler	PRE1
R242	Timer/Counter1	T1
R241	Timer Mode	TMR
R240	Serial I/O	SIO
R239	General-Purpose Registers	
R4		
R3		P3
R2		P2
R1	Port 1	P1
R0	Port 0	P0

Figure 13. Register File

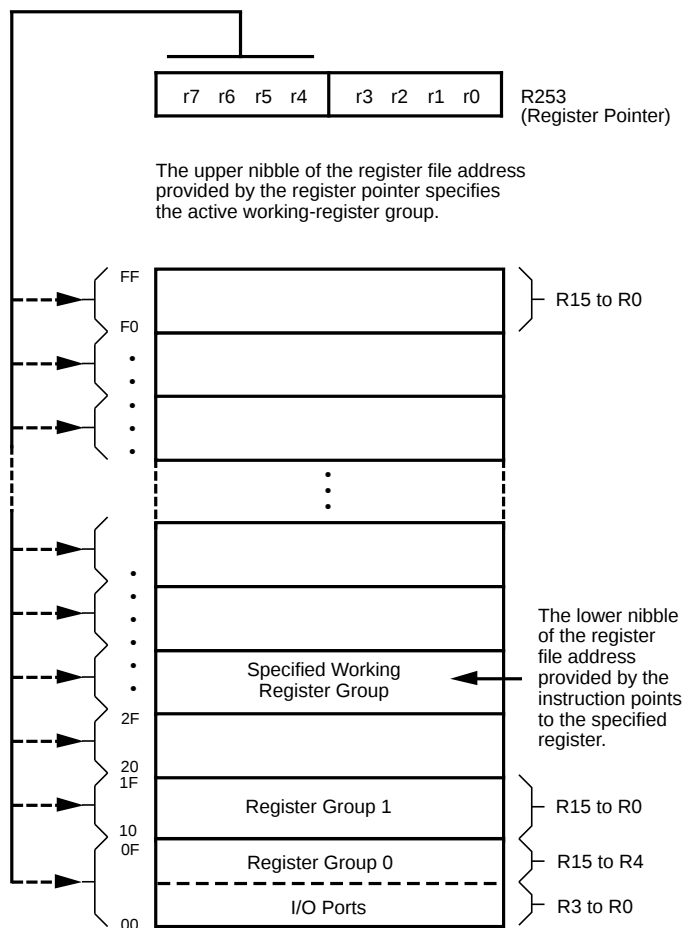


Figure 14. Register Pointer

FUNCTIONAL DESCRIPTION

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 15).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescalers reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter is programmed to start, stop, restart to continue, or restart from the initial value. The counters can also

be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

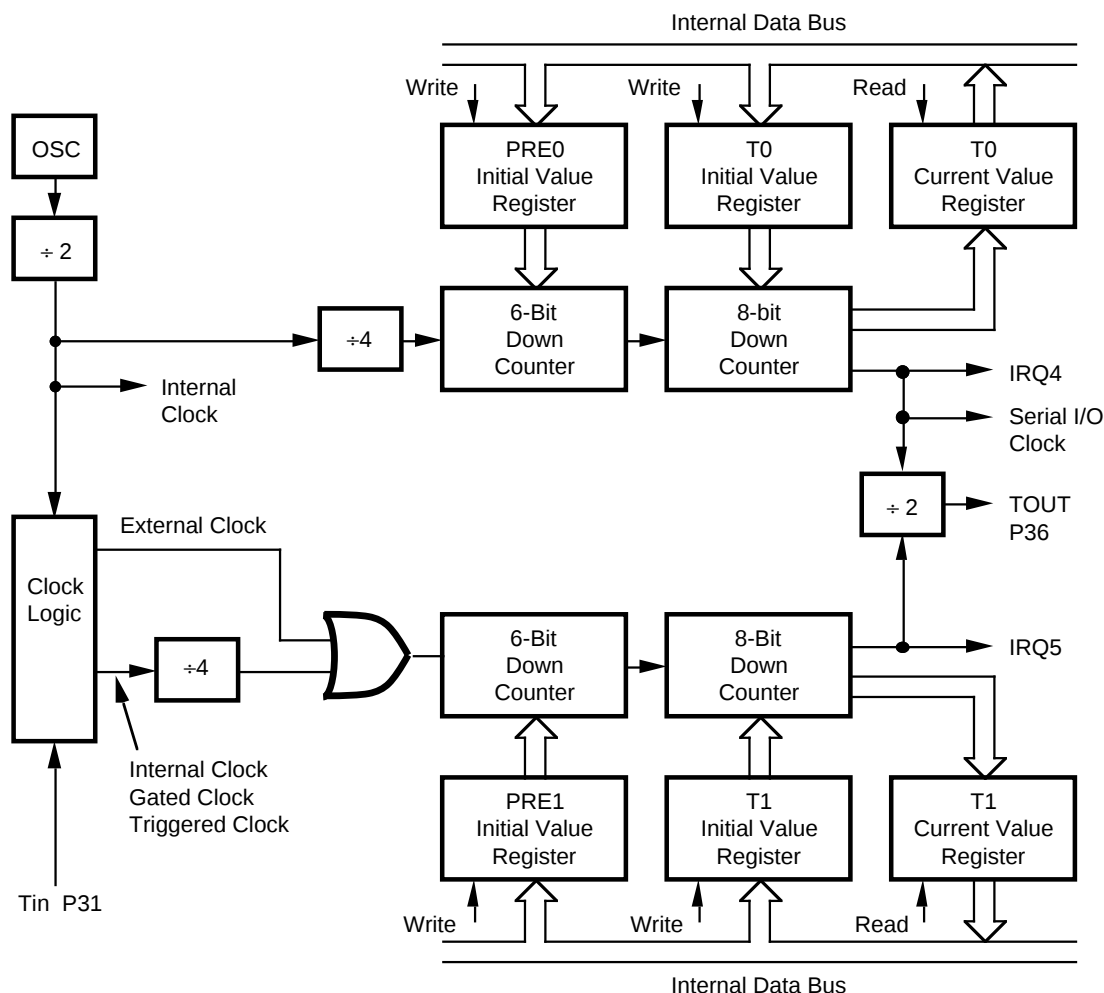


Figure 15. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86E61/E63 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one in Serial In, and two in the counter/timers (Figure 16). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register (refer to Table 5).

All Z86E61/E63 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialized interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

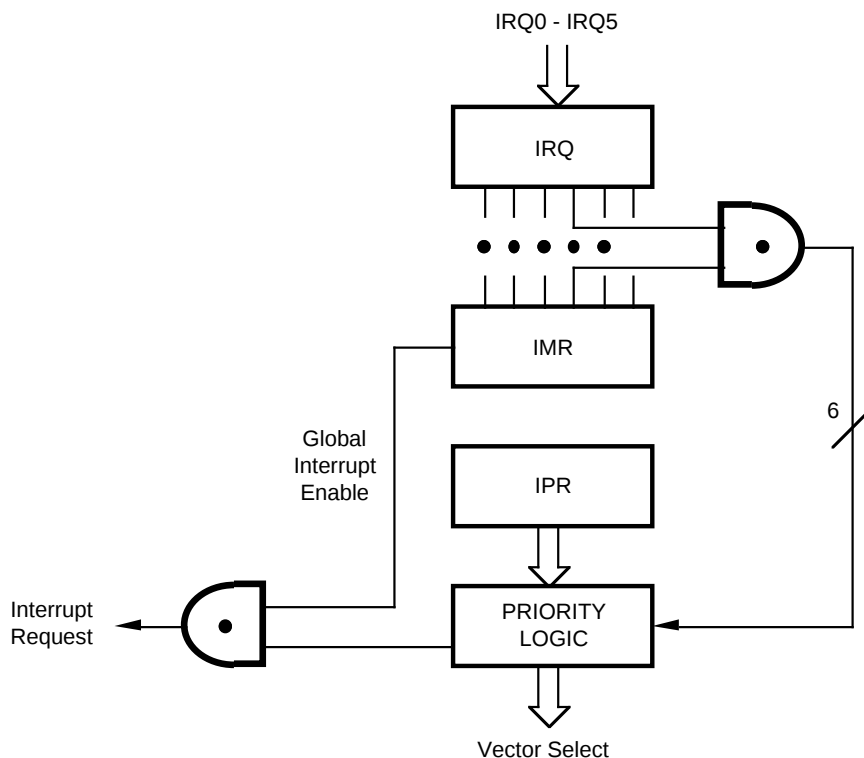


Figure 16. Interrupt Block Diagram

Clock. The Z86E61/E63 on-chip oscillator has a high gain, parallel resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 16 MHz max; series resistance

(RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors ($10\text{ pF} < C_L < 100\text{ pF}$) from each pin to ground (Figure 17). **Note:** Actual capacitor value specified by crystal manufacturer.

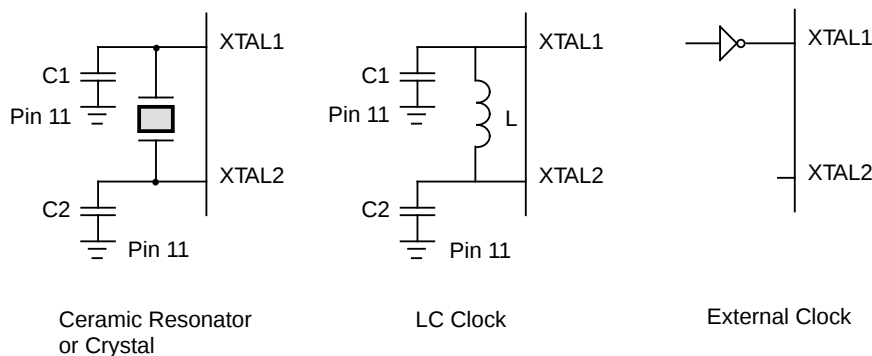


Figure 17. Oscillator Configuration

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation, and reduces the standby current to $5\text{ }\mu\text{A}$ (typical) or less. The STOP mode is terminated by a reset, which causes the processor to restart the application program at address 000C (HEX).

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = 0FFH) immediately before the appropriate SLEEP instruction. i.e.,

```
FF NOP    ; clear the pipeline
6F STOP   ; enter STOP mode
or
FF NOP    ; clear the pipeline
7F HALT   ; enter HALT mode
```

PROGRAMMING

Z86E61/E63 User Modes

The Z86E61/E63 uses separate AC timing cycles for the different User Modes available. Table 6 shows the Z86E61/E63 User Modes. Table 7 shows the timing of the programming waveforms.

User MODE 1 EPROM Read

The Z86E61/E63 EPROM read cycle is provided so that the user may read the Z86E61/E63 as a standard 27128 (E61) or 27256 (E63) EPROM. This is accomplished by driving the /EPM pin (P32) to V_H and activating /CE and /OE. /PGM remains inactive. This mode is not valid after execution of an EPROM protect cycle. Timing for the EPROM read cycle is shown in Figure 18.

User MODE 2 EPROM Program

The Z86E61/E63 Program function conforms to the Intelligent programming algorithm. The device is programmed with V_{CC} at 6.0V and $V_{PP} = 12.5\text{V}$. Programming pulses are applied in 1 ms increments to a maximum of 25 pulses before proper verification. After verification, a programming pulse of three times the duration of the cycles necessary to program the device is issued to ensure proper programming. After all addresses are programmed, a final data comparison is executed and the programming cycle is complete. Timing for the Z86E61/E63 programming cycle is shown in Figure 18.

PROGRAMMING (Continued)

User Mode 3: PROM Verify

The Program Verify cycle is used as part of the intelligent programming algorithm to insure data integrity under worst-case conditions. It differs from the EPROM Read cycle in that V_{PP} is active and V_{CC} must be driven to 6.0V. Timing is shown in Figure 18.

User Modes 4 and 5: EPROM and RAM Protect

To extend program security, EPROM and RAM protect cycles are provided for the Z86E61/E63. Execution of the

EPROM protect cycle prohibits proper execution of the EPROM Read, EPROM Verify, and EPROM programming cycles. Execution of the RAM protect cycle disables accesses to the upper 128 bytes of register memory (excluding mode and configuration registers), but first the user's program must set bit 6 of the IMR (R251). Timing is shown in Figures 20 and 21.

User Modes. Table 6 shows the programming voltage of each mode of the Z86E61/E63.

Table 6. OTP Programming Table

User/Test Mode Device Pin No. User Modes	P33 V_{PP}	P32 EPM	P30 /ICE	P31 /OE	P20 /PGM	ADDR	V_{CC}	Port 1 CNFG Data
EPROM Read	V_{IH}	V_H	V_{IL}	V_{IL}	V_{IH}	Addr	5.0V	Out
Program	V_{PP}	X	V_{IL}	V_{IH}	V_{IL}	Addr	6.0V	In
Program Verify	V_{PP}	X	V_{IL}	V_{IL}	V_{IH}	Addr	6.0V	Out
EPROM Protect	V_{PP}	V_H	V_H	V_{IH}	V_{IL}	XX	6.0V	XX
RAM Protect	V_{PP}	X	V_H	V_{IH}	V_{IL}	XX	6.0V	XX

Notes:

$V_{PP} = 12.0V \pm 0.5V$

$V_H = 12.0V \pm 0.5V$

$V_{IH} = 5V$

$V_{IL} = 0V$

XX = Irrelevant

I_{PP} during programming = 40 mA maximum.

I_{CC} during programming, verify, or read = 40 mA maximum.

Z86E63 Signal Description for EPROM Program/Read

The following signals are required to correctly program or read the Z86E63 device.

ADDR. The address must remain stable throughout the program read cycle.

DATA. The I/O data bus must be stable during programming (/OE High, /PGM Low, V_{PP} High). During read the data bus outputs data.

XCLK. A clock is required to clock the /RESET signal into the registers before programming.

A constant clock can be applied, or the XCLK input can be toggled a minimum of 12 cycles before any programming or verify function begins. The maximum clock frequency to be applied when in the EPROM mode is 12 MHz.

/RESET. The reset input can be held to a constant Low or High value throughout normal programming. It must be held High to program the EPROM protect option bit. Also, any time the /RESET input changes state the XCLK must be clocked a minimum of 12 times to clock the /RESET through the reset filter.

/OE. When the device is placed in EPROM mode, the /OE input also serves as the precharge for the sense amp. The precharge signal should be Low for the first half of the stable address and High for the second half. The PRECHG signal is inverted from the /OE signal so the /OE should be High on the first half and Low on the second half, or stable address. The EPROM output data should be sampled during the second half of stable address.

The access time of the EPROM is defined in later sections. This two part calculation of access time is required because this is a precharged sense amp with a precharge clock.

Table 7. Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		μs
2	Data Setup Time	2		μs
3	V _{PP} Setup	2		μs
4	V _{CC} Setup Time	2		μs
5	Chip Enable Setup Time	2		μs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		μs
8	/OE Setup Time	2		μs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		μs
13	/PGM Setup Time	2		μs
14	Address to /OE Setup Time	2		μs
15	Option Program Pulse Width	78		ms

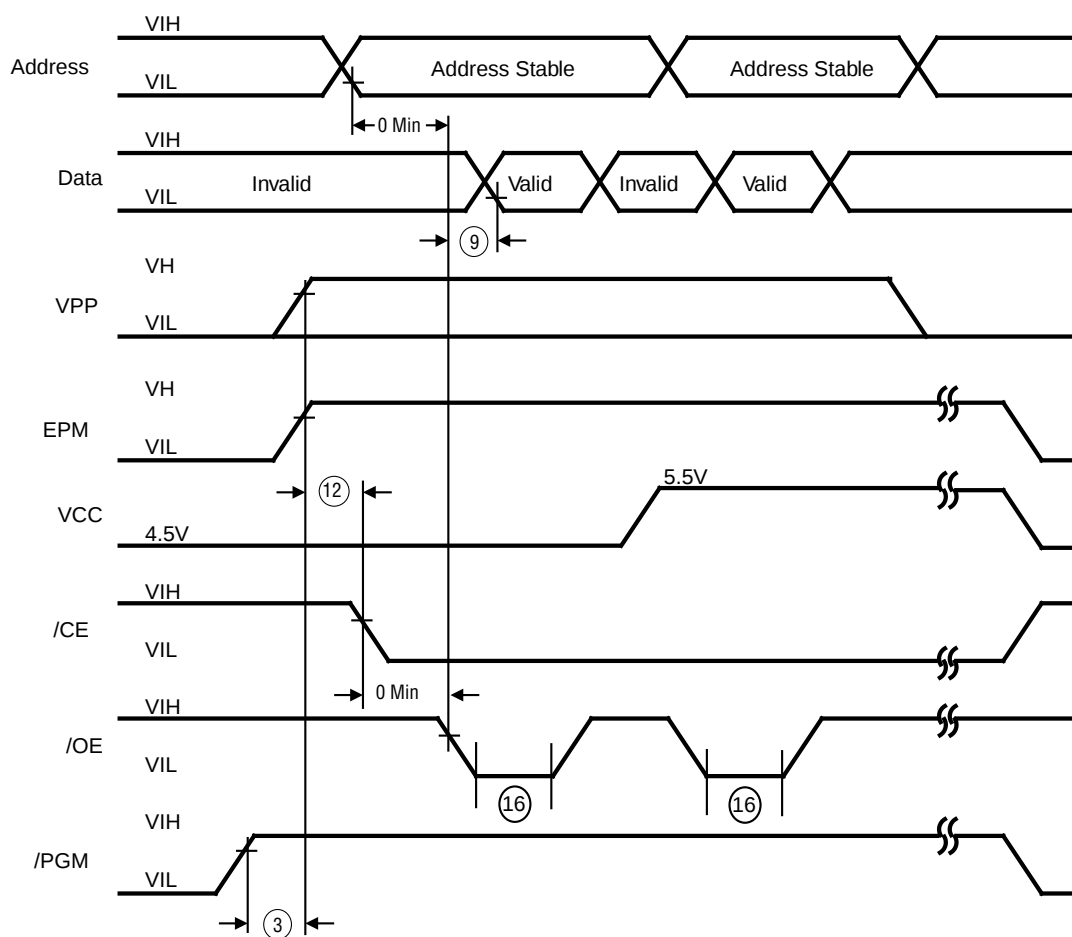


Figure 18. EPROM Read

PROGRAMMING (Continued)

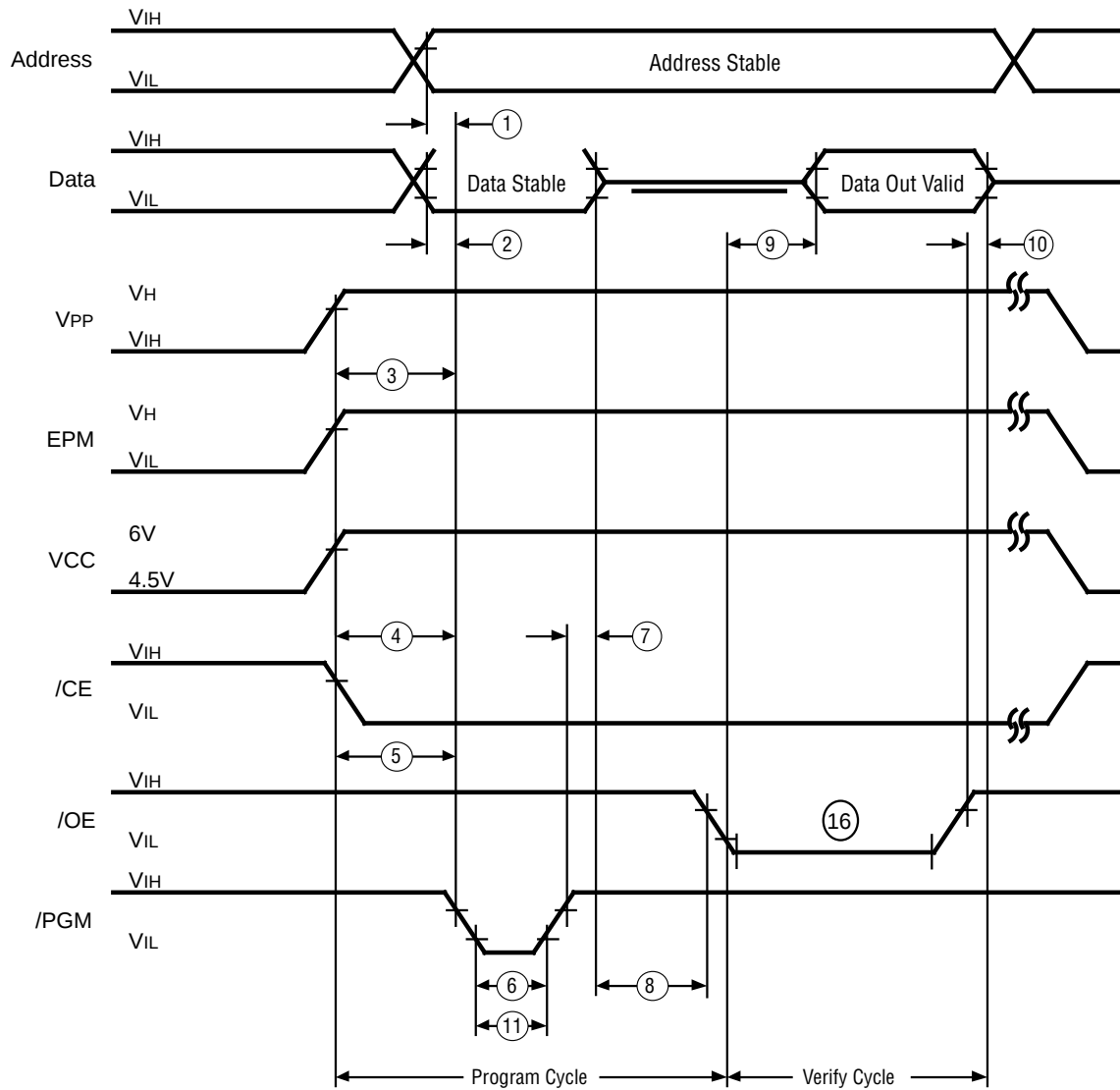


Figure 19. EPROM Program and Verify

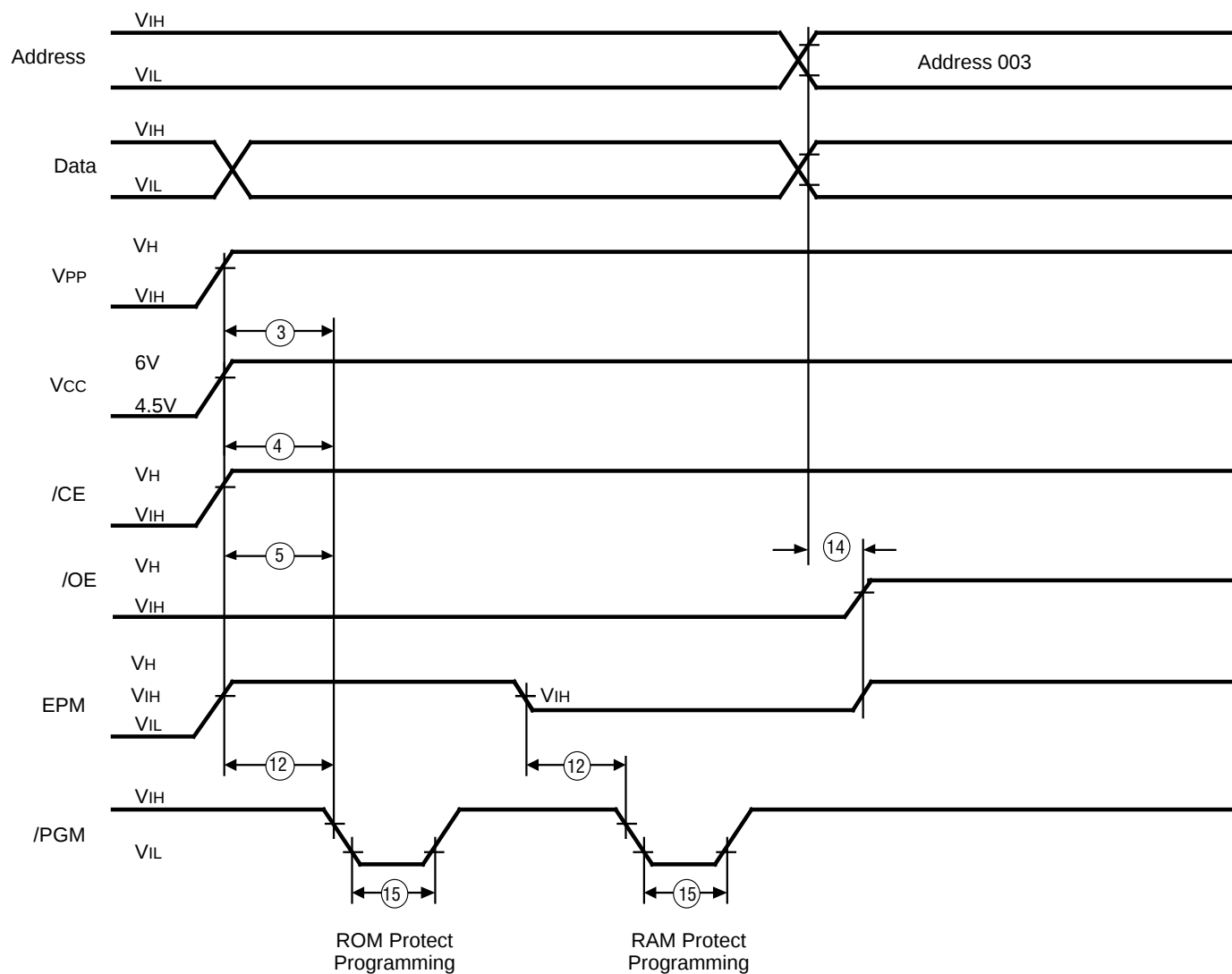


Figure 20. Programming EPROM, RAM Protect and 4K Size Selection

PROGRAMMING (Continued)

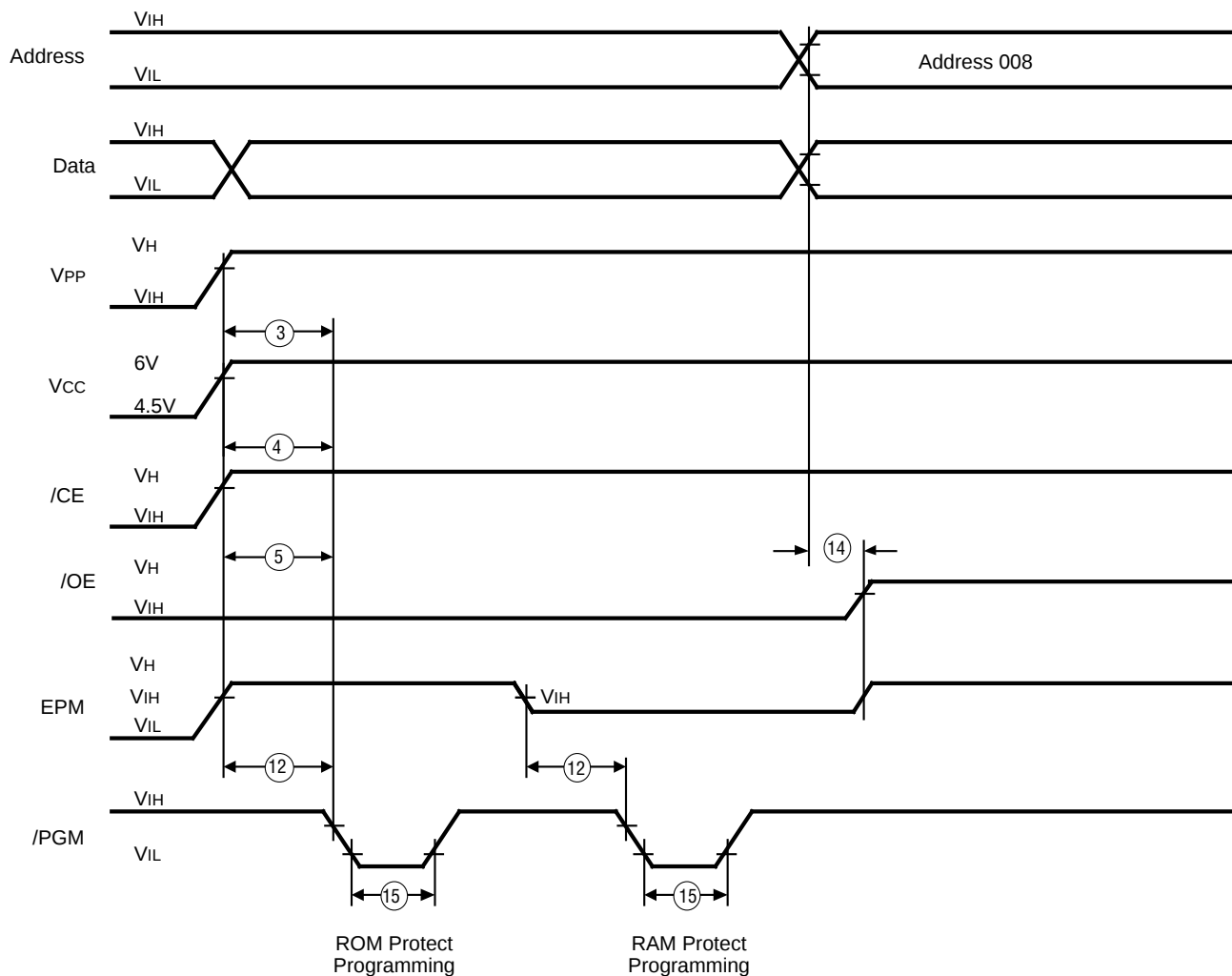


Figure 21. Programming EPROM, RAM Protect and 16K Size Selection

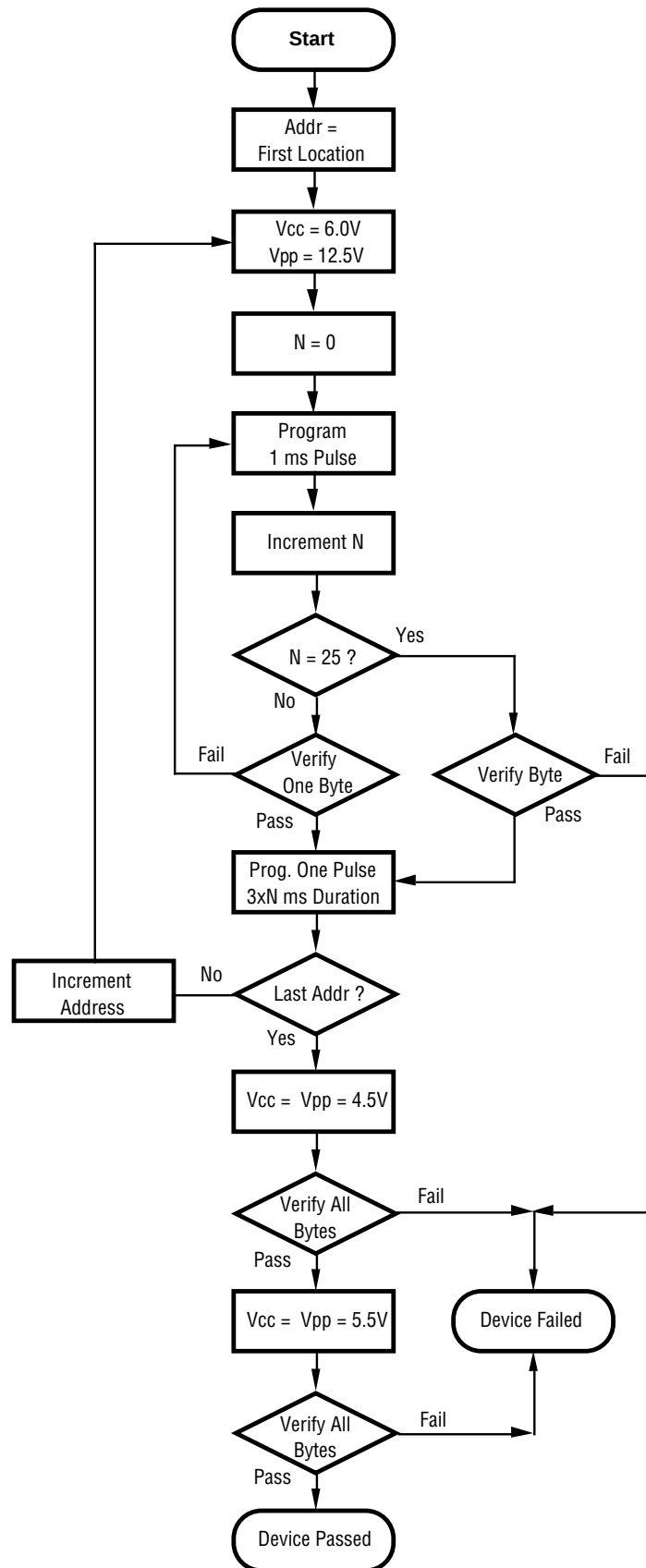


Figure 22. Intelligent Programming Flowchart

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	-0.3	+ 7.0°	V
T_{STG}	Storage Temp	-65°	+150°	C
T_A	Oper Ambient Temp		†	C

Notes:

* Voltages on all pins with respect to GND.

† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 23).

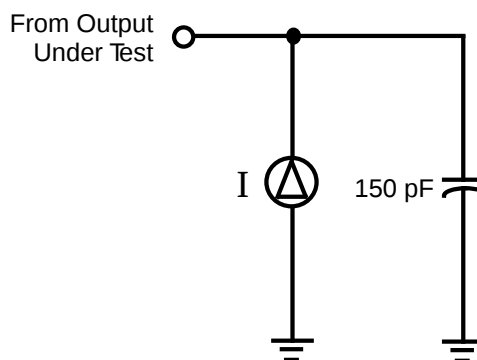


Figure 23. Test Load Diagram

DC CHARACTERISTICS

Sym	Parameter	$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$		Typical @ 25°C	Units	Conditions
		Min	Max			
	Max Input Voltage		7		V	$I_{IN} = 250 \mu\text{A}$
	Max Input Voltage		13		V	P33-P30 Only
V_{CH}	Clock Input High Voltage	3.8	$V_{CC} + 0.3$		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	$V_{CC} + 0.3$		V	
V_{IL}	Input Low Voltage	-0.3	0.8		V	
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -2.0 \text{ mA}$
V_{OL}	Output Low Voltage		0.4		V	$I_{OL} = +2.0 \text{ mA}$
V_{RH}	Reset Input High Voltage	3.8	$V_{CC} + 0.3$		V	
V_{RI}	Reset Input Low Voltage	-0.3	0.8		V	
I_{IL}	Input Leakage	-10	10		μA	0V $V_{IN} + 5.25\text{V}$
I_{OL}	Output Leakage	-10	10		μA	0V $V_{IN} + 5.25\text{V}$
I_{IR}	Reset Input Current		-50		μA	$V_{CC} = +5.25\text{V}, V_{RL} = 0\text{V}$
I_{CC}	Supply Current		50	25	mA	@ 16 MHz
			60	35	mA	@ 20 MHz
I_{CC1}	Standby Current		15	5	mA	HALT Mode $V_{IN} = 0\text{V}, V_{CC} @ 16 \text{ MHz}$
			20	10	mA	HALT Mode $V_{IN} = 0\text{V}, V_{CC} @ 20 \text{ MHz}$
I_{CC2}	Standby Current		20	5	μA	STOP Mode $V_{IN} = 0\text{V}, V_{CC} @ 16 \text{ MHz}$
			20	5	μA	STOP Mode $V_{IN} = 0\text{V}, V_{CC} @ 20 \text{ MHz}$

Notes:

I_{CC2} requires loading TMR (%F1H) with any value prior to STOP execution.

Use this sequence:

LD TMR,#00

NOP

STOP

AC CHARACTERISTICS

External I/O or Memory Read or Write Timing Diagram

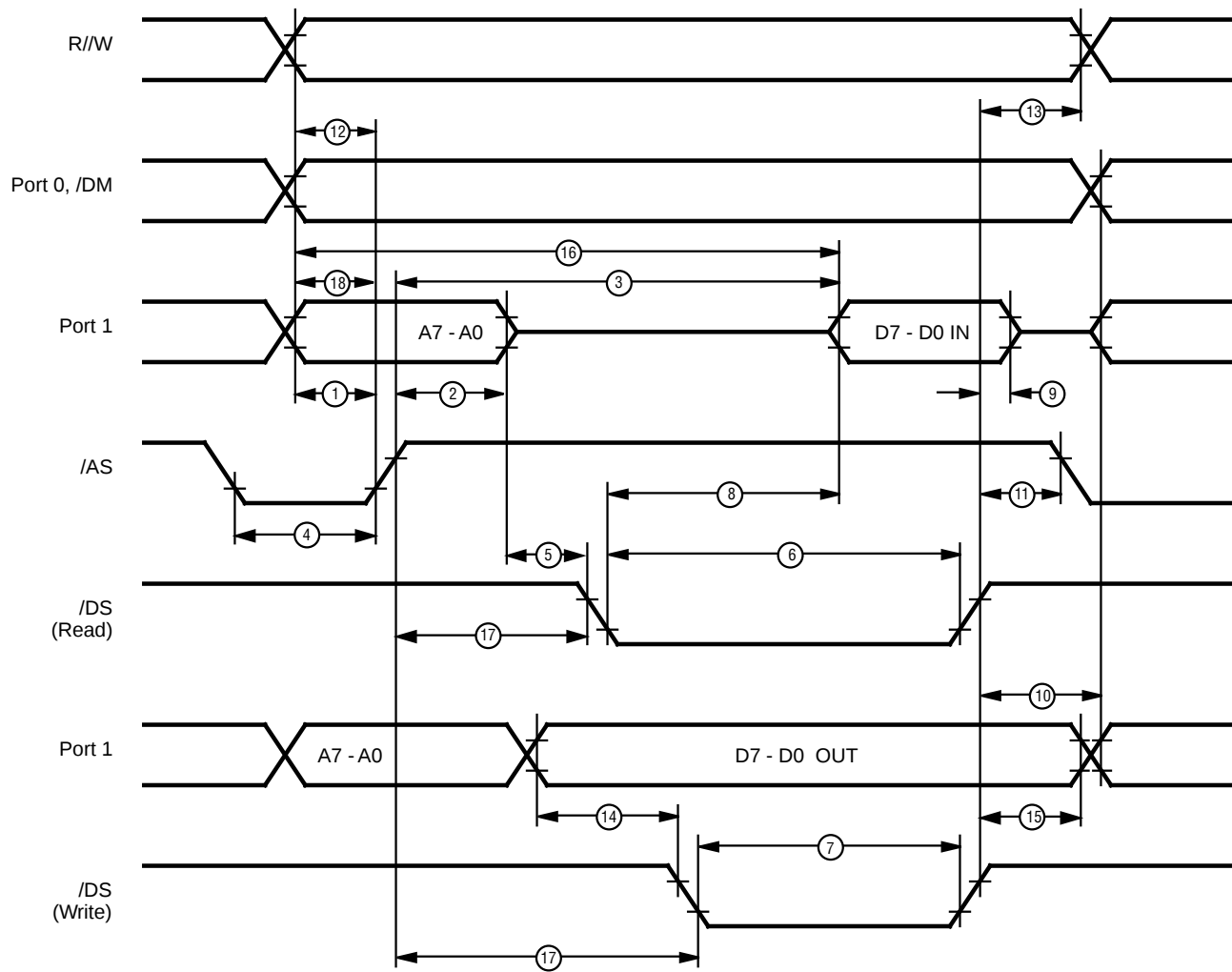


Figure 24. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table

T _A = 0°C to +70°C								
No	Symbol	Parameter	16 MHz		20 MHz		Units	Notes
			Min	Max	Min	Max		
1	TdA(AS)	Address Valid to /AS Rise Delay	20		26		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	30		28		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		180		160	ns	[1,2,3]
4	TwAS	/AS Low Width	35		36		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width	135		130		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	80		75		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		75		100	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	35		48		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	30		36		ns	[2,3]
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	20		32		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R/W Not Valid	30		36		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	25		40		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	30		40		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		200		200	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	40		48		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS Fall Delay	30		36		ns	[2,3]

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

[3] See clock cycle dependent characteristics table.

Standard Test Load

All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	$0.40 \text{ TpC} + 0.32$
2	TdAS(A)	$0.59 \text{ TpC} - 3.25$
3	TdAS(DR)	$2.83 \text{ TpC} + 6.14$
4	TwAS	$0.66 \text{ TpC} - 1.65$
6	TwDSR	$2.33 \text{ TpC} - 10.56$
7	TwDSW	$1.27 \text{ TpC} + 1.67$
8	TdDSR(DR)	$1.97 \text{ TpC} - 42.5$
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	$0.59 \text{ TpC} - 3.14$
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/W)	$0.8 \text{ TpC} - 15$
14	TdDW(DSW)	0.4 sTpC
15	TdDS(DW)	$0.88 \text{ TpC} - 19$
16	TdA(DR)	$4 \text{ TpC} - 20$
17	TdAS(DS)	$0.91 \text{ TpC} - 10.7$
18	TdDM(AS)	$0.9 \text{ TpC} - 26.3$

AC CHARACTERISTICS

Additional Timing Diagram

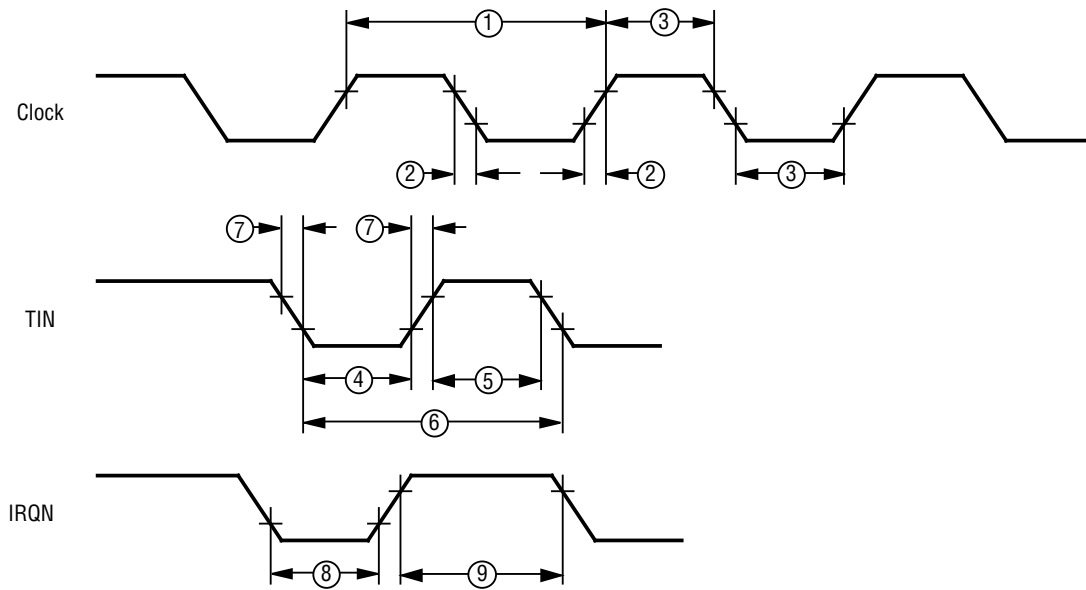


Figure 25. Additional Timing

AC CHARACTERISTICS

Additional Timing Table

T _A = 0°C to +70°C								
No	Symbol	Parameter	16 MHz		20 MHz		Units	Notes
			Min	Max	Min	Max		
1	TpC	Input Clock Period	62.5	1000	50	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		10		15	ns	[1]
3	TwC	Input Clock Width	21		37		ns	[1]
4	TwTinL	Timer Input Low Width	50		75		ns	[2]
5	TwTinH	Timer Input High Width	5TpC		5TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		50		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	5TpC		5TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	5TpC		5TpC			[2,3]

Notes:

- [1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
- [2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
- [3] Interrupt references request through Port 3.
- [4] Interrupt request through Port 3 (P33-P31).
- [5] Interrupt request through Port 30.

AC CHARACTERISTICS

Handshake Timing Diagrams

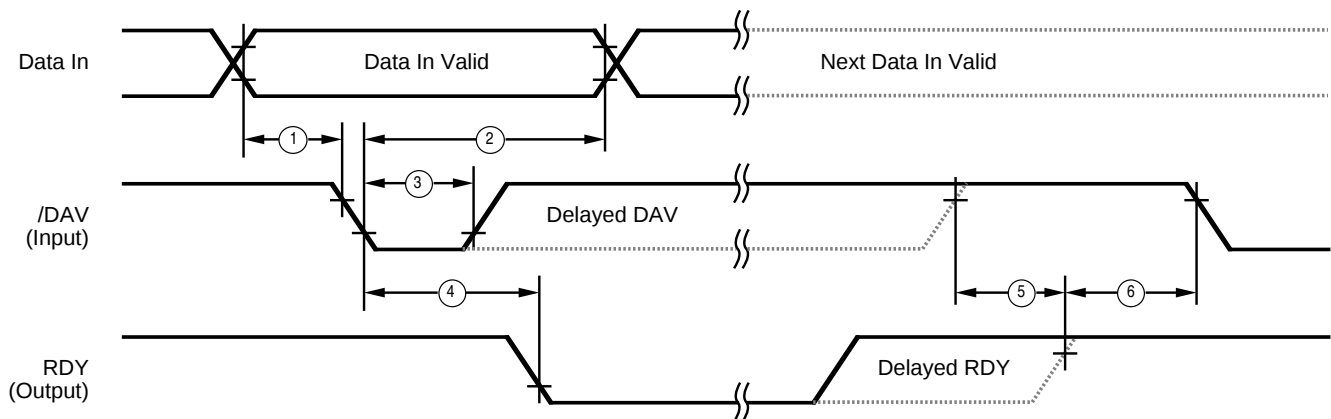


Figure 26. Input Handshake Timing

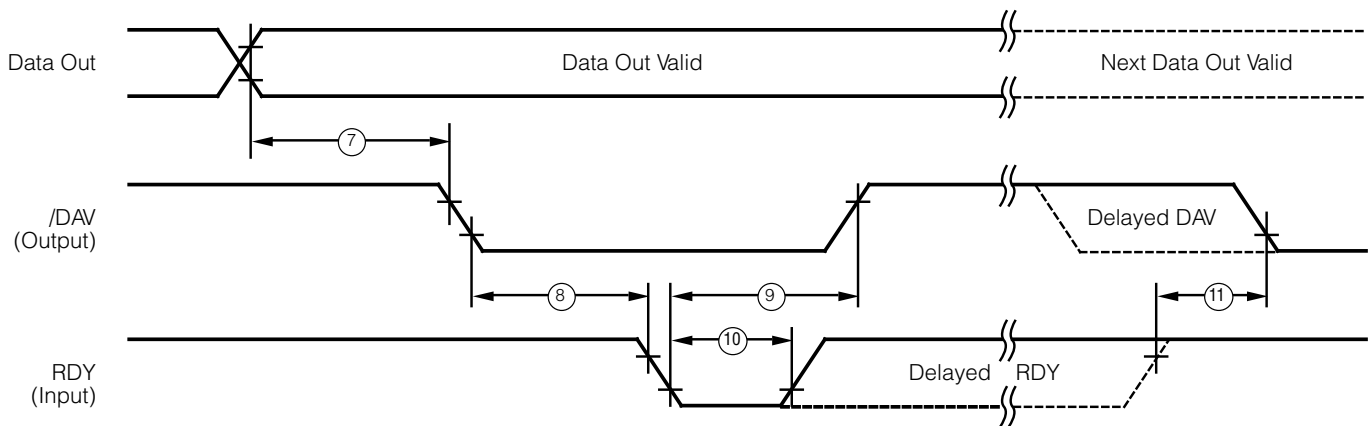


Figure 27. Output Handshake Timing

AC CHARACTERISTICS

Handshake Timing Table

			T _A = 0°C to +70°C				
No	Symbol	Parameter	16 MHz		20 MHz		Data Direction
			Min	Max	Min	Max	
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay		115		115	IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay		TpC		TpC	OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115	OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay		115		115	OUT

Z8 CONTROL REGISTER DIAGRAMS

R240 SIO

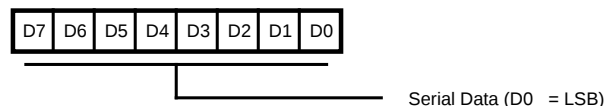


Figure 28. Serial I/O Register
(F0_H: Read/Write)

R241 TMR

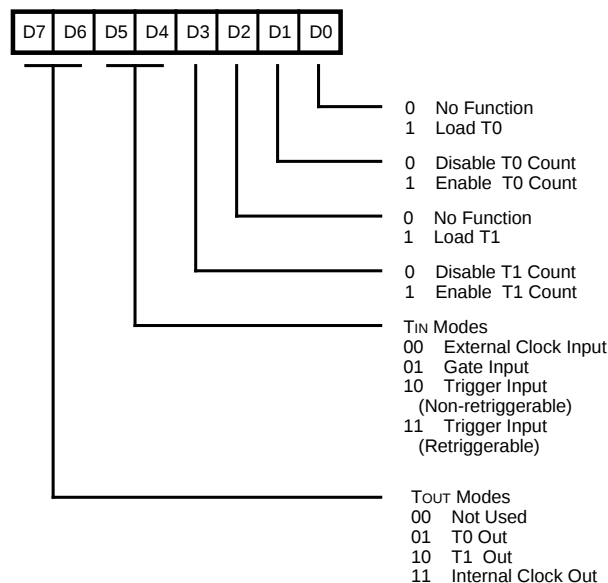


Figure 29. Timer Mode Register
(F1_H: Read/Write)

R242 T1

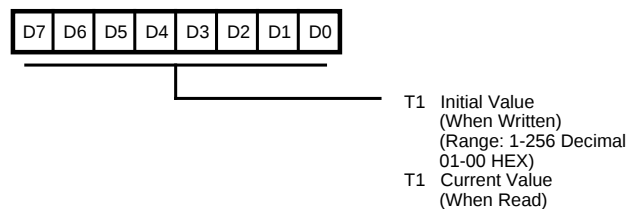


Figure 30. Counter/Timer 1 Register
(F2_H: Read/Write)

R243 PRE1

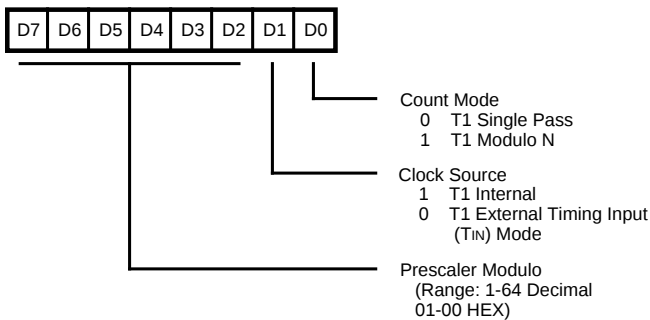


Figure 31. Prescaler 1 Register
(F3_H: Write Only)

R244 T0

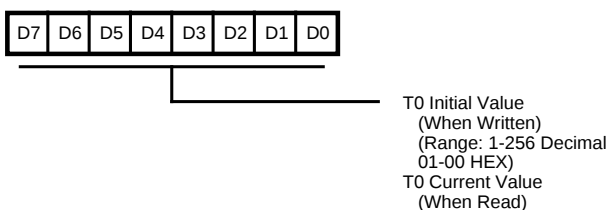


Figure 32. Counter/Timer 0 Register
(F4_H: Read/Write)

R245 PRE0

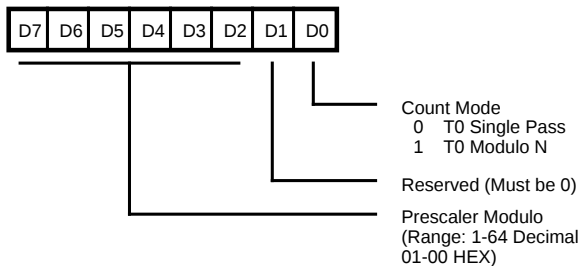
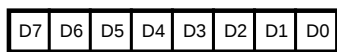


Figure 33. Prescaler 0 Register
(F5_H: Write Only)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

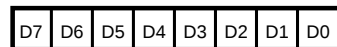
R246 P2M



P2₀ - P2₇ I/O Definition
0 Defines Bit as Output
1 Defines Bit as Input

Figure 34. Port 2 Mode Register
(F6_H: Write Only)

R247 P3M



0 Port 2 Pull-Ups Open Drain
1 Port 2 Pull-Ups Active
Reserved (Must be 0)
0 P32 = Input
P35 = Output
1 P32 = /DAV0/RDY0
P35 = RDY0/DAV0
00 P33 = Input
P34 = Output
01 } P33 = Input
10 } P34 = /DM
11 } P33 = /DAV1/RDY1
P34 = RDY1/DAV1
0 P31 = Input (TIN)
P36 = Output (TOUT)
1 P31 = /DAV2/RDY2
P36 = RDY2/DAV2
0 P30 = Input
P37 = Output
1 P30 = Serial In
P37 = Serial Out
0 Parity Off
1 Parity On

Figure 35. Port 3 Mode Register
(F7_H: Write Only)

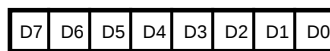
R248 P01M



P0₀ - P0₀ Mode
00 Output
01 Input
1X A₁₁ - A₈
Stack Selection
0 External
1 Internal
P1₇ - P1₀ Mode
00 Byte Output
01 Byte Input
10 AD₇ - AD₀
11 High-Impedance AD₇ - DA₀,
/AS, /DS, /R//W, A₁₁ - A₈,
A₁₅ - A₁₂, If Selected
Reserved (Must be 0)
P0₇ - P0₄ Mode
00 Output
01 Input
1X A₁₅ - A₁₂

Figure 36. Port 0 and 1 Mode Register
(F8_H: Write Only)

R249 IPR



Interrupt Group Priority
Reserved = 000
C > A > B = 001
A > B > C = 010
A > C > B = 011
B > C > A = 100
C > B > A = 101
B > A > C = 110
Reserved = 111
IRQ₁, IRQ₄ Priority (Group C)
0 IRQ₁ > IRQ₄
1 IRQ₄ > IRQ₁
IRQ₀, IRQ₂ Priority (Group B)
0 IRQ₂ > IRQ₀
1 IRQ₀ > IRQ₂
IRQ₃, IRQ₅ Priority (Group A)
0 IRQ₅ > IRQ₃
1 IRQ₃ > IRQ₅
Reserved (Must be 0)

Figure 37. Interrupt Priority Register
(F9_H: Write Only)

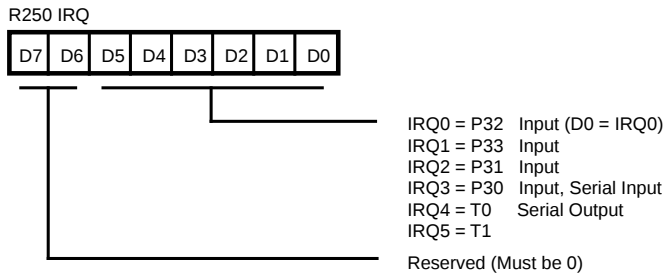


Figure 38. Interrupt Request Register
(FA_H: Read/Write)

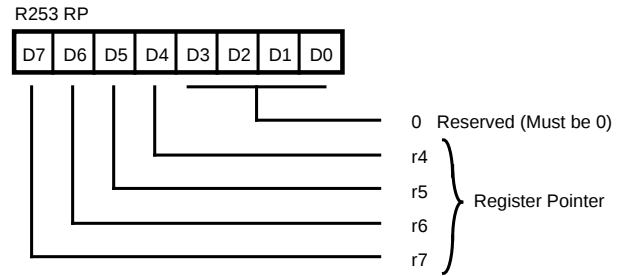


Figure 41. Register Pointer Register
(FD_H: Read/Write)

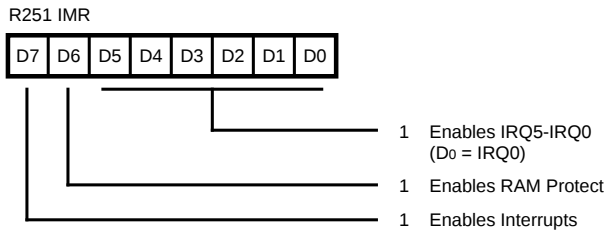


Figure 39. Interrupt Mask Register
(FB_H: Read/Write)

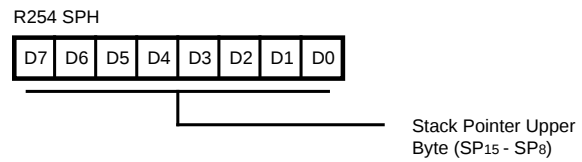


Figure 42. Stack Pointer Register
(FE_H: Read/Write)

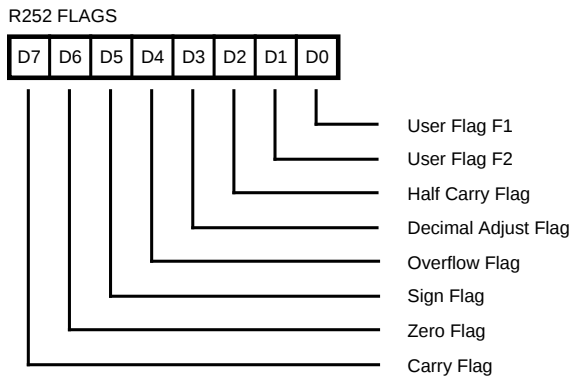


Figure 40. Flag Register
(FC_H: Read/Write)

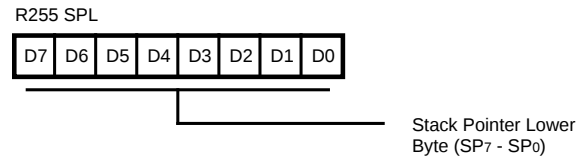


Figure 43. Stack Pointer Register
(FF_H: Read/Write)

DC CHARACTERISTICS

Supply Current

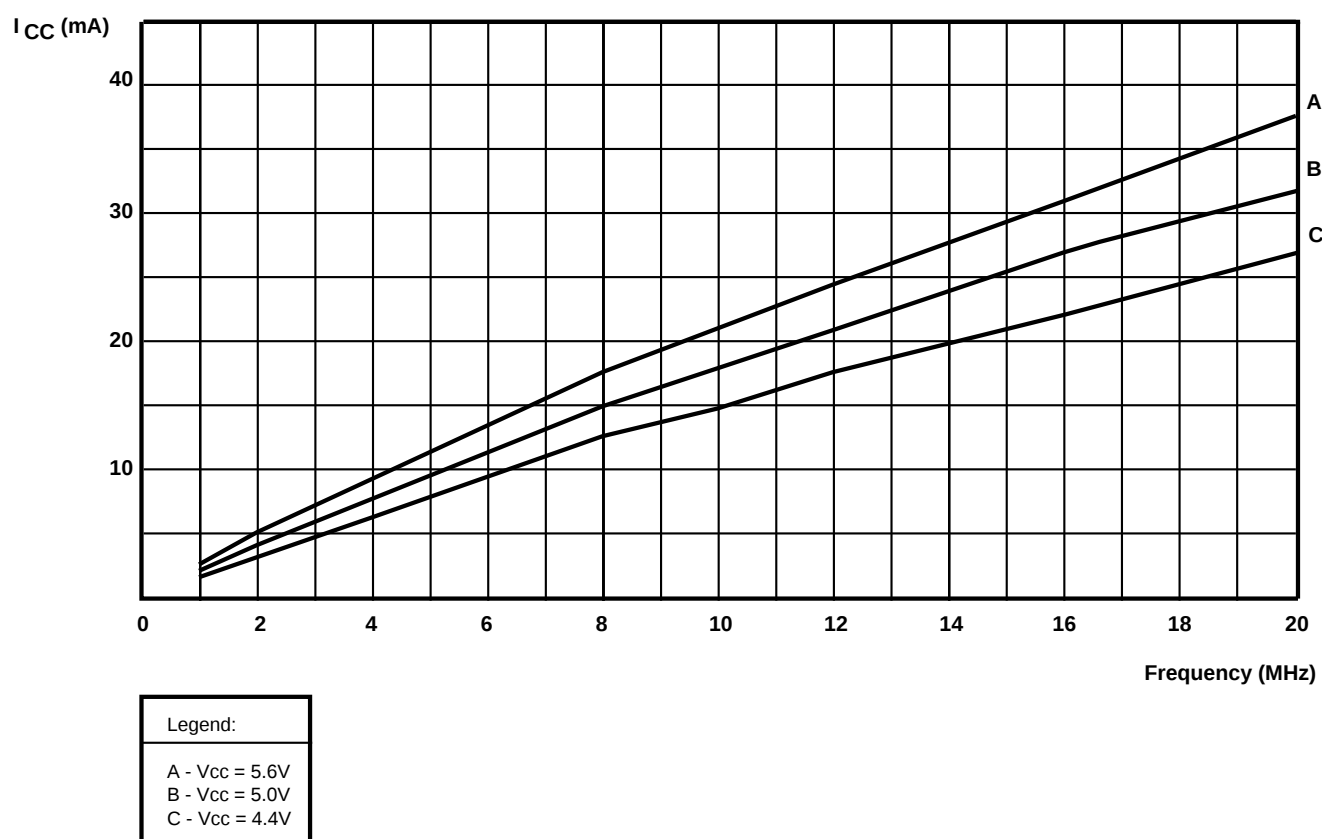


Figure 44. Typical I_{cc} vs Frequency

DC CHARACTERISTICS

Standby Current

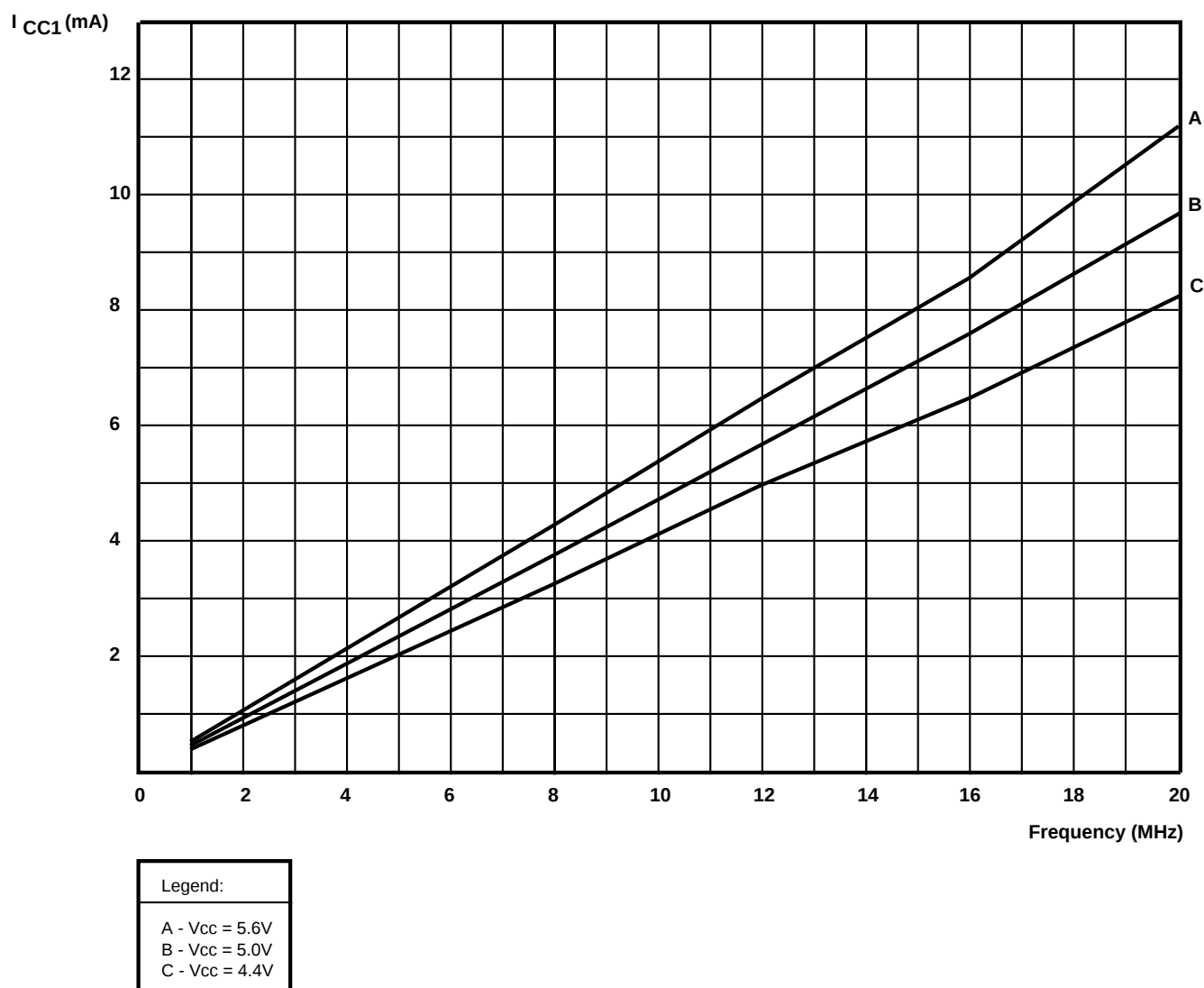


Figure 45. Typical I_{CC1} vs Frequency

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working register pair address
Irr	Indirect working register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working register address
r	Working register address only
IR	Indirect register or indirect working register address
Ir	Indirect working register address only
RR	Register pair or working register pair address

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition Code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag Register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt Mask Register (R251)

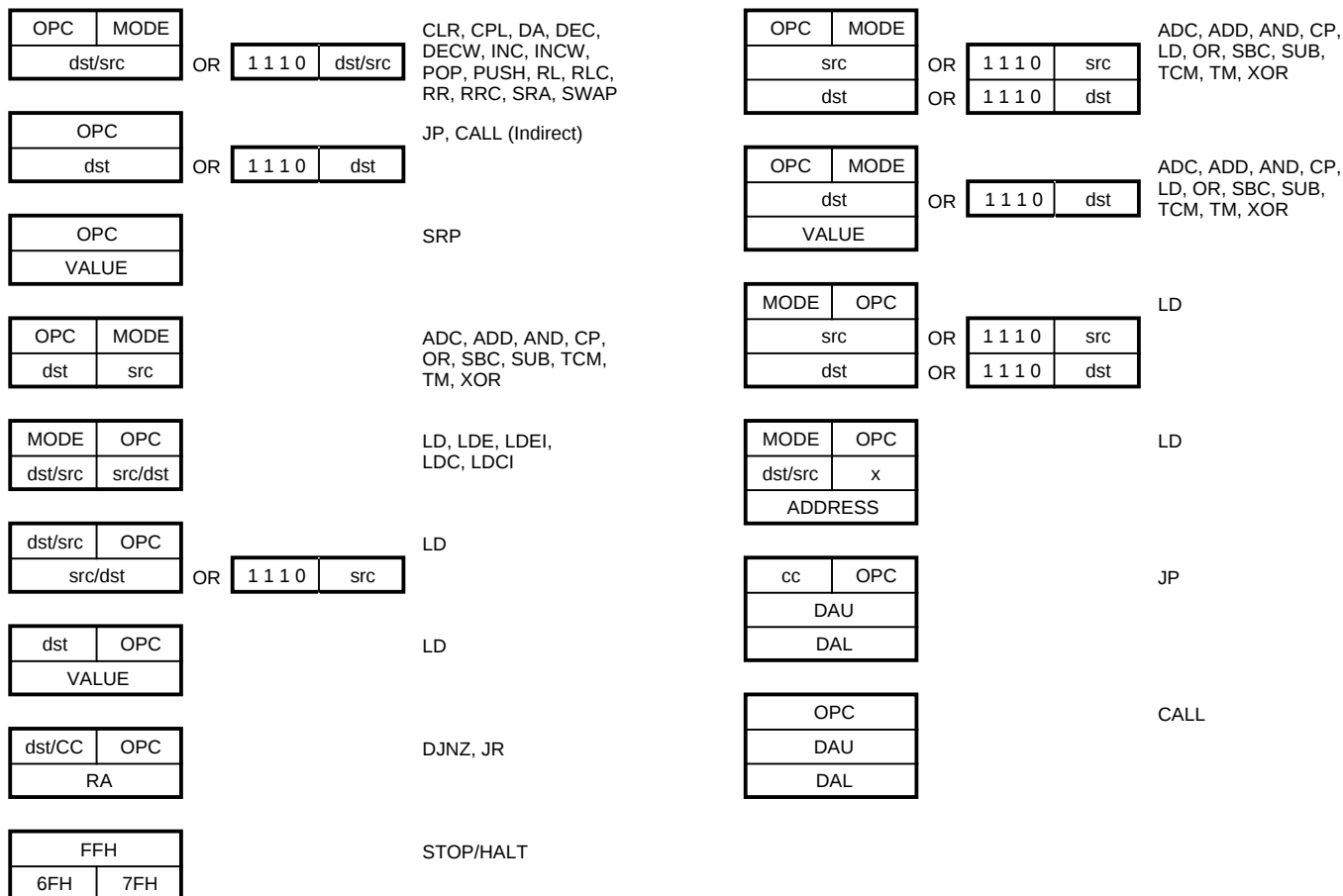
CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	

INSTRUCTION FORMATS



One-Byte Instructions



Two-Byte Instructions

Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol “←”. For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The

notation “addr (n)” is used to refer to bit (n) of a given operand location. For example:

dst (7)

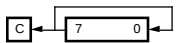
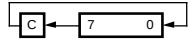
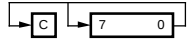
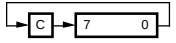
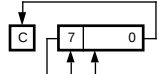
refers to bit 7 of the destination operand.

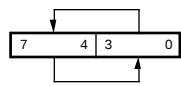
INSTRUCTION SUMMARY

Instruction and Operation	Address Mode		Opcode Byte (Hex)	Flags Affected						
	dst	src		C	Z	S	V	D	H	
ADC dst, src dst ← dst + src + C	†		1[]	*	*	*	*	0	*	
ADD dst, src dst ← dst + src	†		0[]	*	*	*	*	0	*	
AND dst, src dst ← dst AND src	†		5[]	-	*	*	*	0	-	-
CALL dst SP ← SP - 2 @SP ← PC, PC ← dst	DA IRR		D6 D4	-	-	-	-	-	-	-
CCF C ← NOT C			EF	*	-	-	-	-	-	-
CLR dst dst ← 0	R IR		B0 B1	-	-	-	-	-	-	-
COM dst dst ← NOT dst	R IR		60 61	-	*	*	*	0	-	-
CP dst, src dst - src	†		A[]	*	*	*	*	*	-	-
DA dst dst ← DA dst	R IR		40 41	*	*	*	*	X	-	-
DEC dst dst ← dst - 1	R IR		00 01	-	*	*	*	*	-	-
DECW dst dst ← dst - 1	RR IR		80 81	-	*	*	*	*	-	-
DI IMR(7) ← 0			8F	-	-	-	-	-	-	-
DJNZr , dst r ← r - 1 if r ≠ 0 PC ← PC + dst Range: +127, -128	RA		rA r = 0 - F	-	-	-	-	-	-	-
EI IMR(7) ← 1			9F	-	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-	-

Instruction and Operation	Address Mode		Opcode Byte (Hex)	Flags Affected						
	dst	src		C	Z	S	V	D	H	
INC dst dst ← dst + 1	r R IR		rE r = 0 - F 20 21	-	*	*	*	*	-	-
INCW dst dst ← dst + 1	RR IR		A0 A1	-	*	*	*	*	-	-
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR(7) ← 1			BF	*	*	*	*	*	*	*
JP cc, dst if cc is true, PC ← dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-	-
JR cc, dst if cc is true, PC ← PC + dst Range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-	-
LD dst, src dst ← src	r r R r r X r lr lr R R R IR IR R	lm R r X r lr r R IR IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-	-
LDC dst, src dst ← src	r	lrr	C2	-	-	-	-	-	-	-
LDCI dst, src dst ← src r ← r + 1; rr ← rr + 1	lr	lrr	C3	-	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode		Opcode Byte (Hex)	Flags Affected						
	dst	src		C	Z	S	V	D	H	
NOP			FF	-	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[]	-	*	*	0	-	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src	R IR		70 71	-	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-	-
SBC dst, src dst←dst←src←C	†		3[]	*	*	*	*	1	*	*
SCF C←1			DF	1	-	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-	-
SRP dst RP←src	Im		31	-	-	-	-	-	-	-

Instruction and Operation	Address Mode		Opcode Byte (Hex)	Flags Affected						
	dst	src		C	Z	S	V	D	H	
STOP			6F	1	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[]	[	[	[	[	1	[	[
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-	-
TCM dst, src (NOT dst) AND src	†		6[]	-	*	*	0	-	-	-
TM dst, src dst AND src	†		7[]	-	*	*	0	-	-	-
XOR dst, src dst←dst XOR src	†		B[]	-	*	*	0	-	-	-

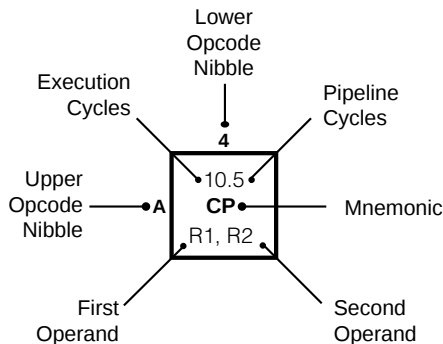
† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode		Lower Opcode Nibble
dst	src	
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

		Lower Nibble (Hex)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Upper Nibble (Hex)	0	6.5 DEC R1	6.5 DEC IR1	6.5 ADD r1, r2	6.5 ADD r1, Ir2	10.5 ADD R2, R1	10.5 ADD IR2, R1	10.5 ADD R1, IM	10.5 ADD IR1, IM	6.5 LD r1, R2	6.5 LD r2, R1	12/10.5 DJNZ r1, RA	12/10.0 JR cc, RA	6.5 LD r1, IM	12.10.0 JP cc, DA	6.5 INC r1	
	1	6.5 RLC R1	6.5 RLC IR1	6.5 ADC r1, r2	6.5 ADC r1, Ir2	10.5 ADC R2, R1	10.5 ADC IR2, R1	10.5 ADC R1, IM	10.5 ADC IR1, IM								
	2	6.5 INC R1	6.5 INC IR1	6.5 SUB r1, r2	6.5 SUB r1, Ir2	10.5 SUB R2, R1	10.5 SUB IR2, R1	10.5 SUB R1, IM	10.5 SUB IR1, IM								
	3	8.0 JP IRR1	6.1 SRP IM	6.5 SBC r1, r2	6.5 SBC r1, Ir2	10.5 SBC R2, R1	10.5 SBC IR2, R1	10.5 SBC R1, IM	10.5 SBC IR1, IM								
	4	8.5 DA R1	8.5 DA IR1	6.5 OR r1, r2	6.5 OR r1, Ir2	10.5 OR R2, R1	10.5 OR IR2, R1	10.5 OR R1, IM	10.5 OR IR1, IM								
	5	10.5 POP R1	10.5 POP IR1	6.5 AND r1, r2	6.5 AND r1, Ir2	10.5 AND R2, R1	10.5 AND IR2, R1	10.5 AND R1, IM	10.5 AND IR1, IM								
	6	6.5 COM R1	6.5 COM IR1	6.5 TCM r1, r2	6.5 TCM r1, Ir2	10.5 TCM R2, R1	10.5 TCM IR2, R1	10.5 TCM R1, IM	10.5 TCM IR1, IM								6.0 STOP
	7	10/12.1 PUSH R2	12/14.1 PUSH IR2	6.5 TM r1, r2	6.5 TM r1, Ir2	10.5 TM R2, R1	10.5 TM IR2, R1	10.5 TM R1, IM	10.5 TM IR1, IM								7.0 HALT
	8	10.5 DECW RR1	10.5 DECW IR1	12.0 LDE r1, Irr2	18.0 LDEI Ir1, Irr2												6.1 DI
	9	6.5 RL R1	6.5 RL IR1	12.0 LDE r2, Irr1	18.0 LDEI Ir2, Irr1												6.1 EI
	A	10.5 INCW RR1	10.5 INCW IR1	6.5 CP r1, r2	6.5 CP r1, Ir2	10.5 CP R2, R1	10.5 CP IR2, R1	10.5 CP R1, IM	10.5 CP IR1, IM								14.0 RET
	B	6.5 CLR R1	6.5 CLR IR1	6.5 XOR r1, r2	6.5 XOR r1, Ir2	10.5 XOR R2, R1	10.5 XOR IR2, R1	10.5 XOR R1, IM	10.5 XOR IR1, IM								16.0 IRET
	C	6.5 RRC R1	6.5 RRC IR1	12.0 LDC r1, Irr2	18.0 LDCI Ir1, Irr2												6.5 RCF
	D	6.5 SRA R1	6.5 SRA IR1	12.0 LDC r1, Irr2	18.0 LDCI Ir1, Irr2	20.0 CALL* IRR1		20.0 CALL DA	10.5 LD r2,x,R1								6.5 SCF
	E	6.5 RR R1	6.5 RR IR1		6.5 LD r1, IR2	10.5 LD R2, R1	10.5 LD IR2, R1	10.5 LD R1, IM	10.5 LD IR1, IM								6.5 CCF
	F	8.5 SWAP R1	8.5 SWAP IR1		6.5 LD Ir1, r2		10.5 LD R2, IR1										6.0 NOP



Legend:

R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

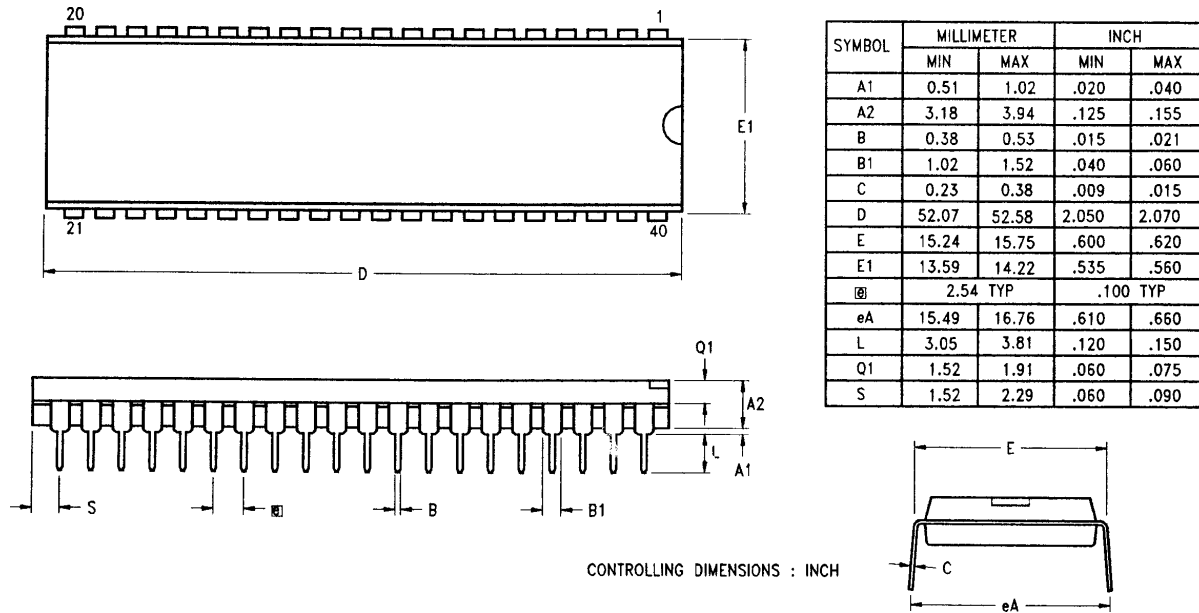
Sequence:

Opcode, First Operand,
Second Operand

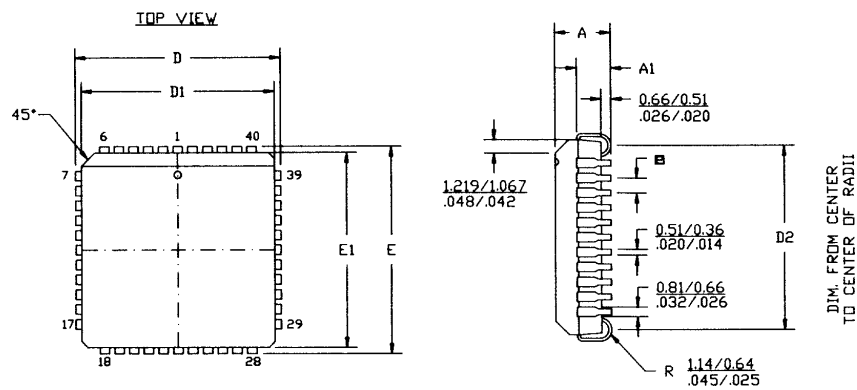
Note: Blank areas not defined.

*2-byte instruction appears as
a 3-byte instruction

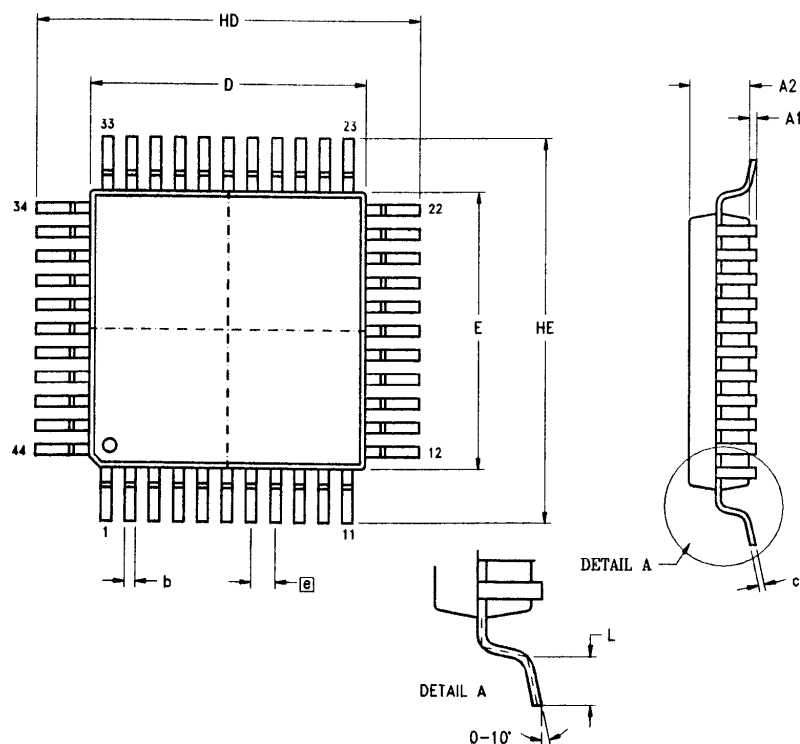
PACKAGE INFORMATION



40-Pin DIP Package Diagram



44-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX $\frac{.10}{.004}$

44-Pin QFP Package Diagram

ORDERING INFORMATION

Z86E61

16 MHz

40-Pin DIP

Z86E6116PSC

44-Pin PLCC

Z86E6116VSC

20 MHz

40-Pin DIP

Z86E6120PSC

44-Pin PLCC

Z86E6120VSC

44-Pin QFP

Z86E6116FEC

Z86E63

16 MHz

40-Pin DIP

Z86E6316PSC

44-Pin PLCC

Z86E6316VSC

20 MHz

40-Pin DIP

Z86E6320PSC

44-Pin PLCC

Z86E6320VSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Preferred Package

P = Plastic DIP

V = Plastic Chip Carrier

Temperature

S = 0°C to +70°C

Speeds

12 = 16 MHz

16 = 20 MHz

Environmental

C = Plastic Standard

Example:

Z 86E61 16 P S C is an Z86E61, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

