



## 1-Mbit (64K x 16) Static RAM

### Features

- **Temperature Ranges**
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
  - Automotive: -40°C to 125°C
- **High speed**
  - $t_{AA} = 10$  ns (Commercial & Industrial)
  - $t_{AA} = 15$  ns (Automotive)
- **CMOS for optimum speed/power**
- **Low active power**
  - 825 mW (max.)
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **Available in 44-pin TSOP II and 400-mil SOJ**
- **Also available in Lead (Pb)-Free 44-pin TSOP II**

### Functional Description<sup>[1]</sup>

The CY7C1021B/10211B is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

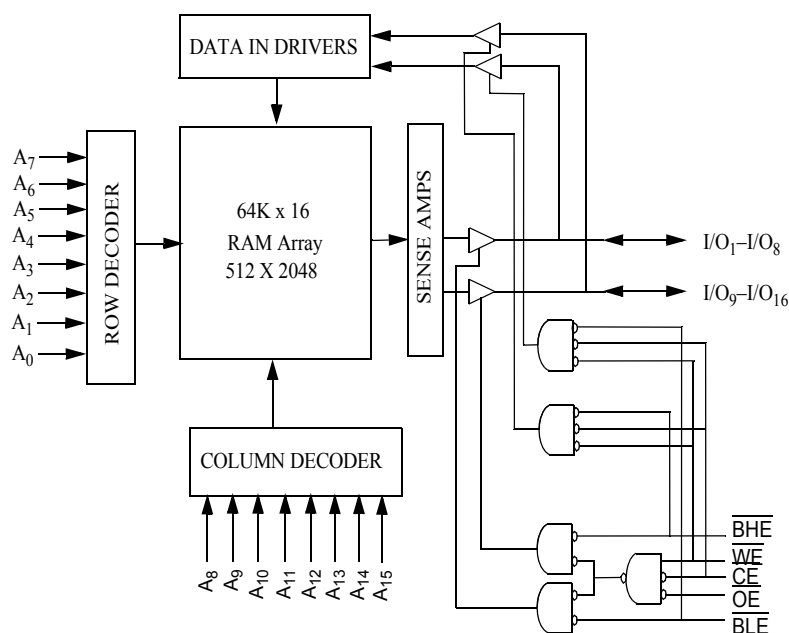
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_1$  through  $I/O_8$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_9$  through  $I/O_{16}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_1$  to  $I/O_8$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_9$  to  $I/O_{16}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins ( $I/O_1$  through  $I/O_{16}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1021B/10211B is available in standard 44-pin TSOP Type II and 400-mil-wide SOJ packages. Customers should use part number CY7C10211B when ordering parts with 10-ns  $t_{AA}$ , and CY7C1021B when ordering 12- and 15-ns  $t_{AA}$ .

### Logic Block Diagram



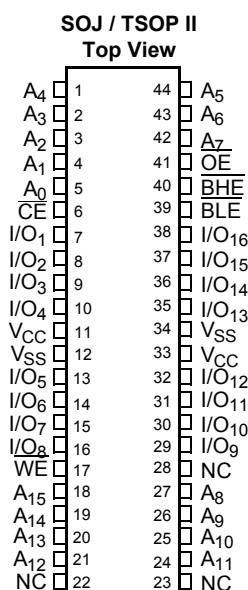
#### Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

## Selection Guide

		7C10211B-10	7C1021B-12	7C1021B-15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)	Com'l / Ind'l	150	140	130
	Automotive	-	-	150
Maximum CMOS Standby Current (mA)	Com'l / Ind'l	10	10	10
	Automotive	-	-	15
	L Version	0.5	0.5	0.5

## Pin Configurations



## Pin Definitions

Pin Name	SOJ, TSOP-Pin Number	I/O Type	Description
A <sub>0</sub> –A <sub>15</sub>	1–5, 18–21, 24–27, 42–44	Input	<b>Address Inputs used to select one of the address locations.</b>
I/O <sub>1</sub> –I/O <sub>16</sub>	7–10, 13–16, 29–32, 35–38	Input/Output	<b>Bidirectional Data I/O lines.</b> Used as input or output lines depending on operation.
NC	22, 23, 28	No Connect	<b>No Connects.</b> Not connected to the die.
$\overline{\text{WE}}$	17	Input/Control	<b>Write Enable Input, active LOW.</b> When selected LOW, a Write is conducted. When deselected HIGH, a Read is conducted.
$\overline{\text{CE}}$	6	Input/Control	<b>Chip Enable Input, active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{BHE}}$ , $\overline{\text{BLE}}$	39, 40	Input/Control	<b>Byte Write Select Inputs, active LOW.</b> $\overline{\text{BLE}}$ controls I/O <sub>8</sub> –I/O <sub>1</sub> , $\overline{\text{BHE}}$ controls I/O <sub>16</sub> –I/O <sub>9</sub> .
$\overline{\text{OE}}$	41	Input/Control	<b>Output Enable, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins.
V <sub>SS</sub>	12, 34	Ground	<b>Ground for the device.</b> Should be connected to ground of the system.
V <sub>CC</sub>	11, 33	Power Supply	<b>Power Supply inputs to the device.</b>

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[2]</sup> .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State<sup>[2]</sup> ..... -0.5V to  $V_{CC}+0.5V$

DC Input Voltage<sup>[2]</sup> ..... -0.5V to  $V_{CC}+0.5V$

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

Range	Ambient Temperature ( $T_A$ ) <sup>[3]</sup>	$V_{CC}$
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Automotive	-40°C to +125°C	5V ± 10%

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C10211B-10		7C1021B-12		7C1021B-15		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = −4.0 mA		2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA			0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.2	6.0	2.2	6.0	2.2	6.0	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>			−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Com'l / Ind'l	−1	+1	−1	+1	−1	+1	μA
			Automotive	-	-	-	-	-4	+4	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	Com'l / Ind'l	−1	+1	−1	+1	−1	+1	μA
			Automotive	-	-	-	-	-4	+4	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[4]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND			−300		−300		−300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com'l / Ind'l		150		140		130	mA
			Automotive		-		-		150	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Com'l / Ind'l		40		40		40	mA
			Automotive		-		-		50	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l / Ind'l		10		10		10	mA
			Automotive		-		-		15	mA
			L Version		0.5		0.5		0.5	mA

## Thermal Resistance<sup>[5]</sup>

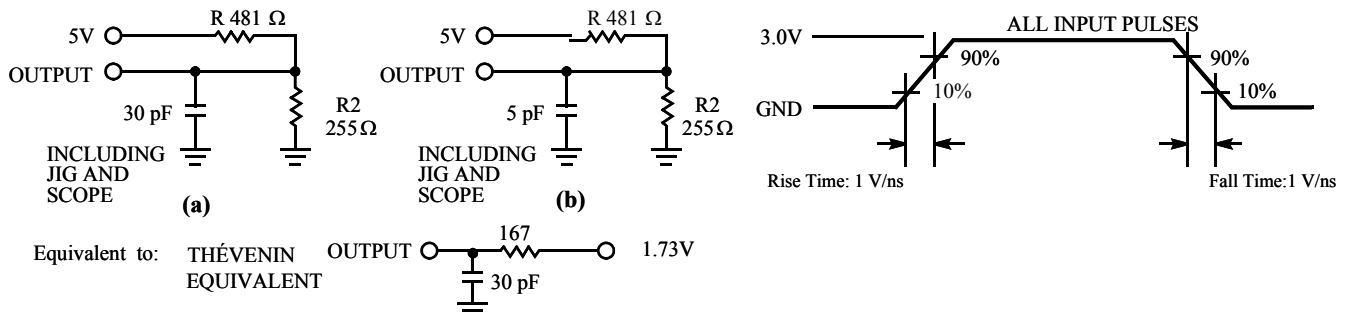
Parameter	Description	Test Conditions	44-lead SOJ	44-lead TSOP-II	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	64.32	76.89	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		31.03	14.28	°C/W

### Notes:

- $V_{IL}(\text{min.}) = -2.0V$  and  $V_{IH}(\text{max.}) = V_{CC} + 0.5V$  for pulse durations of less than 20 ns.
- $T_A$  is the "Instant On" case temperature.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{V}$	8	pF
$C_{OUT}$	Output Capacitance		8	pF

**AC Test Loads and Waveforms**

**Switching Characteristics<sup>[6]</sup> Over the Operating Range**

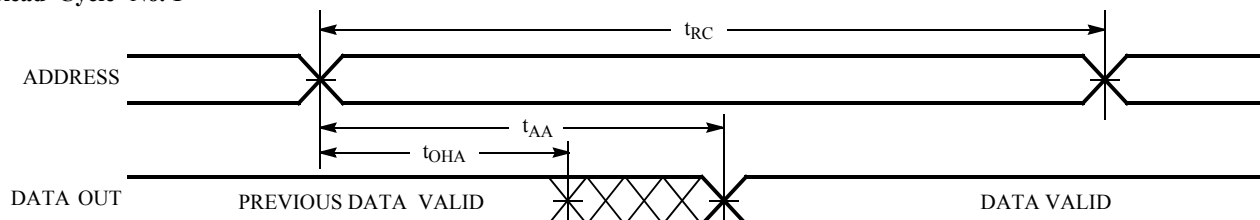
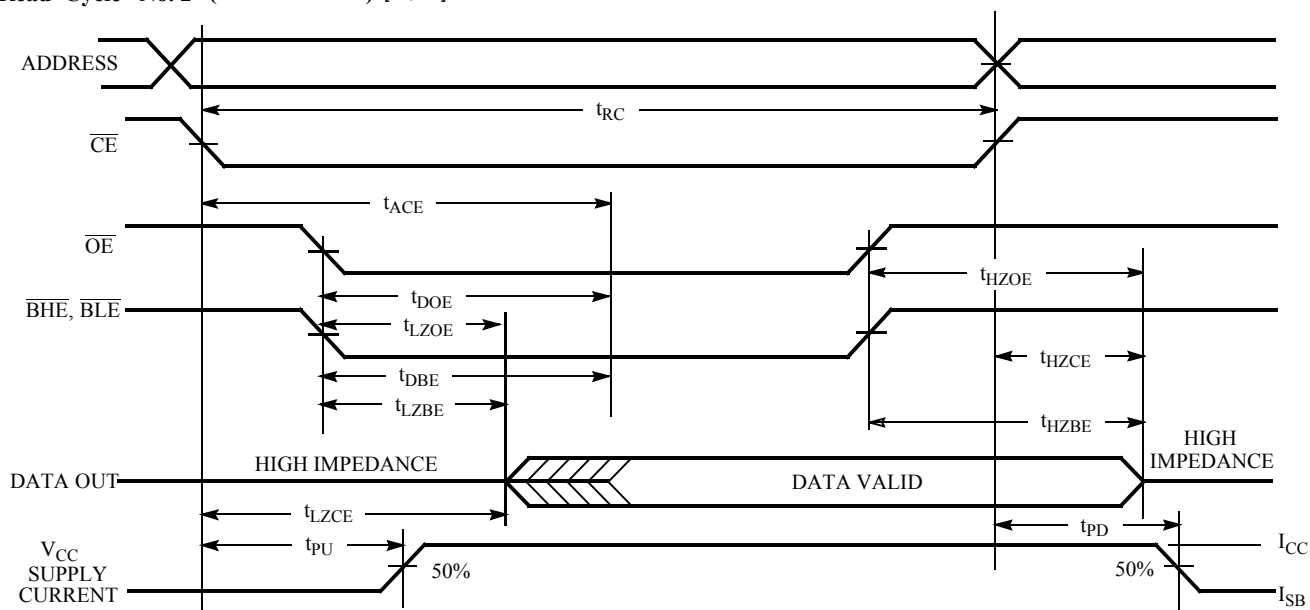
Parameter	Description	7C10211B-10		7C1021B-12		7C1021B-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t <sub>RC</sub>	Read Cycle Time	10		12		15		ns
t <sub>AA</sub>	Address to Data Valid		10		12		15	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		5		6		7	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[7]</sup>	0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[7, 8]</sup>		5		6		7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup>		5		6		7	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		10		12		15	ns
t <sub>DBE</sub>	Byte Enable to Data Valid		5		6		7	ns
t <sub>LZBE</sub>	Byte Enable to Low Z	0		0		0		ns
t <sub>HZBE</sub>	Byte Disable to High Z		5		6		7	ns
Write Cycle <sup>[9]</sup>								
t <sub>WC</sub>	Write Cycle Time	10		12		15		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	8		9		10		ns
t <sub>AW</sub>	Address Set-Up to Write End	7		8		10		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		ns
t <sub>SD</sub>	Data Set-Up to Write End	5		6		8		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns

**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500\text{ mV}$  from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and  $\overline{BHE}/\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$  and  $\overline{BHE}/\overline{BLE}$  must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

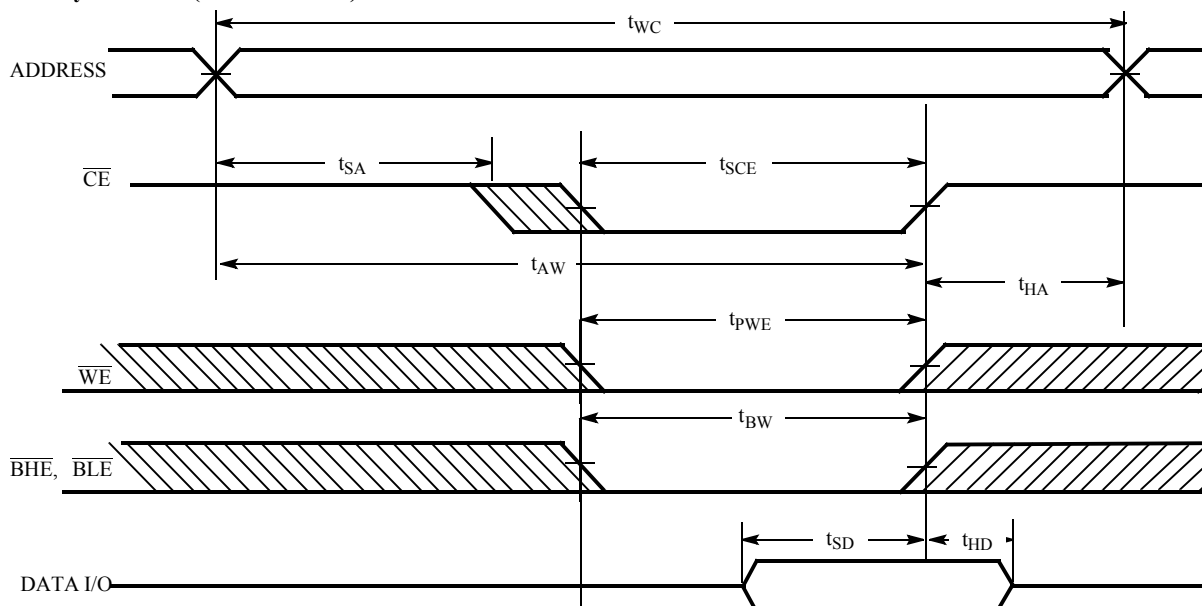
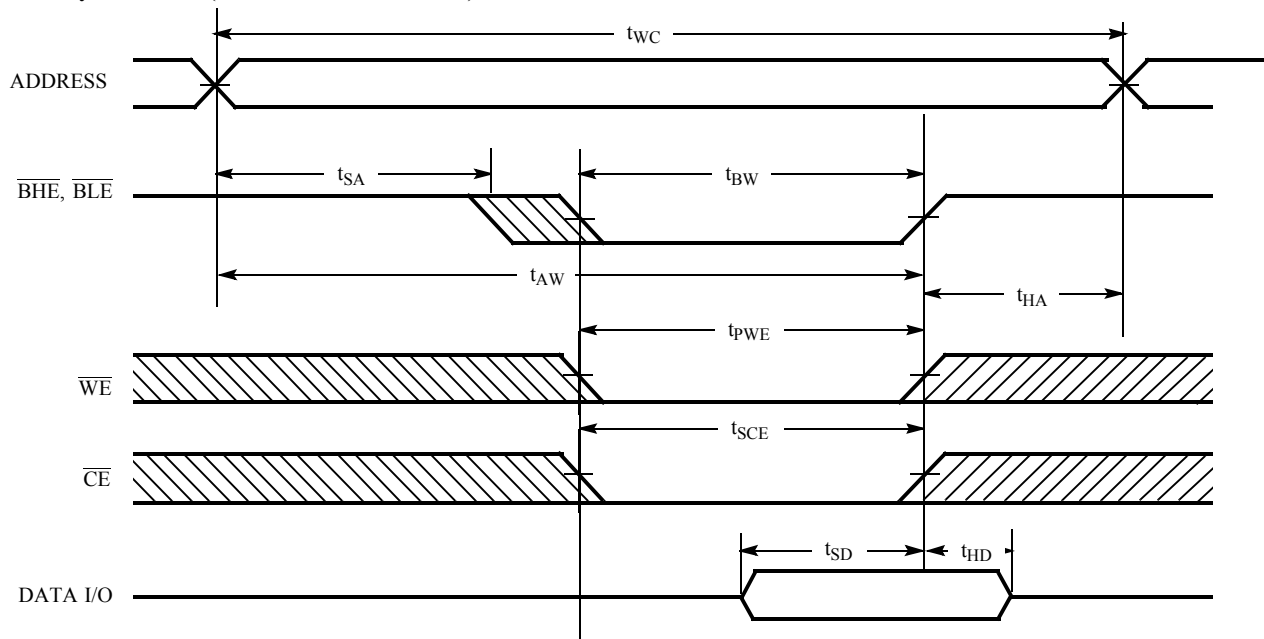
**Switching Characteristics<sup>[6]</sup> Over the Operating Range (continued)**

Parameter	Description	7C10211B-10		7C1021B-12		7C1021B-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>		5		6		7	ns
$t_{BW}$	Byte Enable to End of Write	7		8		9		ns

**Switching Waveforms**
**Read Cycle No. 1** <sup>[10, 11]</sup>

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)** <sup>[11, 12]</sup>

**Notes:**

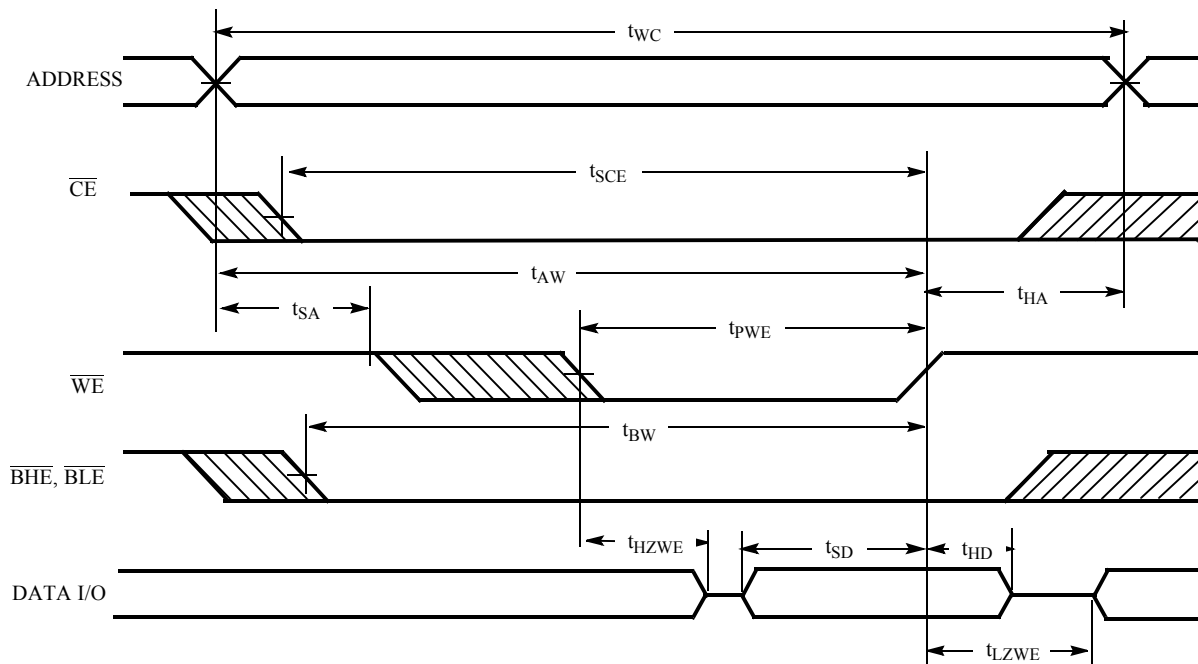
10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IL}$ .

11.  $\overline{WE}$  is HIGH for read cycle.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [13, 14]**

**Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**

**Notes:**

12. Address valid prior to or coincident with  $\overline{\text{CE}}$  transition LOW.
13. Data I/O is high impedance if OE or BHE and/or BLE =  $V_{\text{IH}}$ .
14. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled, LOW)**

**Truth Table**

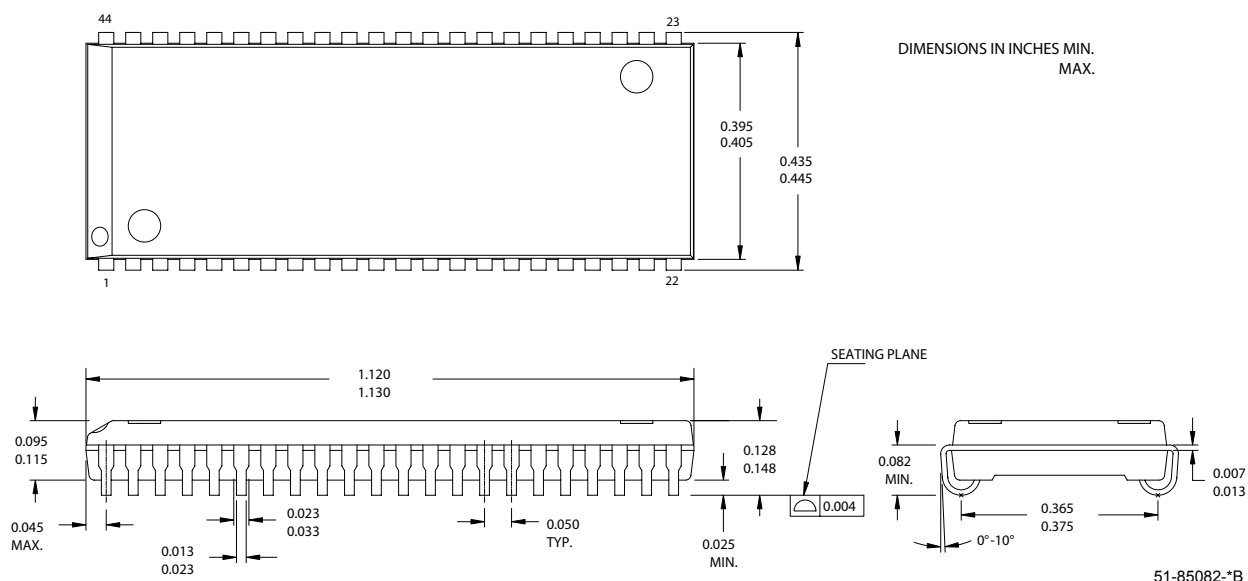
$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O <sub>1</sub> –I/O <sub>8</sub>	I/O <sub>9</sub> –I/O <sub>16</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby ( $I_{\text{SB}}$ )
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active ( $I_{\text{CC}}$ )
			L	H	Data Out	High Z	Read - Lower bits only	Active ( $I_{\text{CC}}$ )
			H	L	High Z	Data Out	Read - Upper bits only	Active ( $I_{\text{CC}}$ )
L	X	L	L	L	Data In	Data In	Write - All bits	Active ( $I_{\text{CC}}$ )
			L	H	Data In	High Z	Write - Lower bits only	Active ( $I_{\text{CC}}$ )
			H	L	High Z	Data In	Write - Upper bits only	Active ( $I_{\text{CC}}$ )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{\text{CC}}$ )
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{\text{CC}}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C10211B-10VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C10211B-10ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C10211BL-10ZC	Z44	44-Lead TSOP Type II	Commercial
12	CY7C1021B-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1021B-12VI	V34	44-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1021BL-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1021B-12ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1021B-12ZI	Z44	44-Lead TSOP Type II	Industrial
	CY7C1021BL-12ZC	Z44	44-Lead TSOP Type II	Commercial

**Ordering Information** (continued)

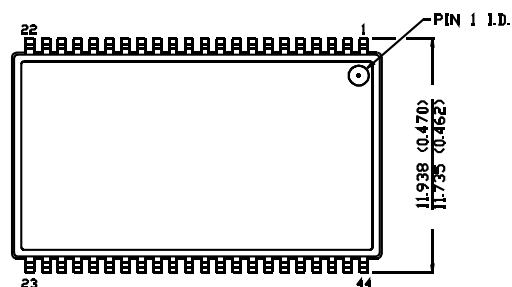
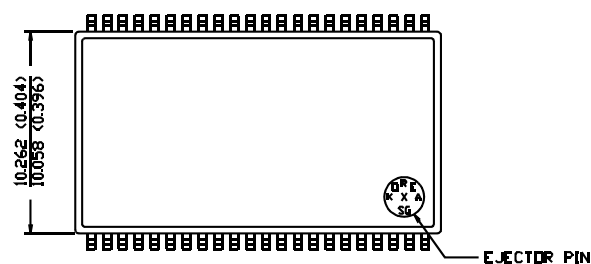
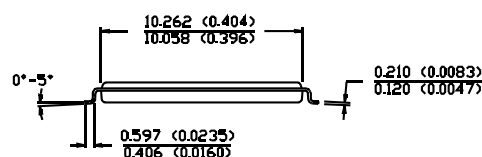
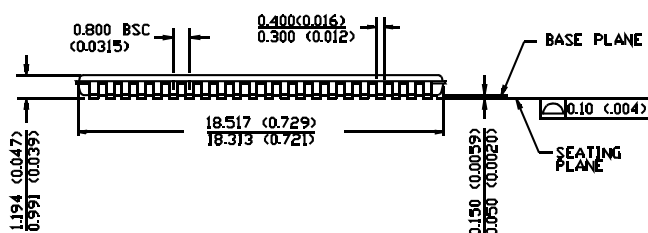
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1021B-15VC	V34	44-pin (400-Mil) Molded SOJ	Commercial
	CY7C1021B-15VI	V34	44-pin (400-Mil) Molded SOJ	Industrial
	CY7C1021BL-15VC	V34	44-pin (400-Mil) Molded SOJ	Commercial
	CY7C1021B-15VE	V34	44-pin (400-Mil) Molded SOJ	Automotive
	CY7C1021B-15ZC	Z44	44-pin TSOP Type II	Commercial
	CY7C1021B-15ZXC	Z44	Lead (Pb)-Free, 44-pin TSOP Type II	Commercial
	CY7C1021B-15ZI	Z44	44-pin TSOP Type II	Industrial
	CY7C1021BL-15ZC	Z44	44-pin TSOP Type II	Commercial
	CY7C1021B-15ZE	Z44	44-pin TSOP Type II	Automotive

**Package Diagrams**
**44-Lead (400-Mil) Molded SOJ V34**




**Package Diagrams** (continued)

**44-Pin TSOP II Z44**

 DIMENSION IN MM (INCH)  
 MAX  
 MIN

**TOP VIEW**

**BOTTOM VIEW**


51-85087-\*A

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**Document History Page**

<b>Document Title: CY7C1021B/CY7C10211B 64K x 16 Static RAM</b> <b>Document Number: 38-05145</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	109889	09/22/01	SZV	Change from Spec number: 38-00951 to 38-05145
*A	238454	See ECN	RKF	1) Added Automotive Specs to Data Sheet 2) Added Pb-Free device offering in the Ordering Information