

Multimode SCSI 9 Line Terminator

FEATURES

- Auto Selection Single Ended (SE) or Low Voltage Differential (LVD) Termination
- Meets SCSI-1, SCSI-2, SCSI-3, SPI, Ultra (Fast-20), Ultra2 (SPI-2 LVD) and Ultra3 Standards
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Thermal packaging for low junction temperature and better MTBF
- Master/Slave Input
- Supports Active Negation
- 3pF Channel Capacitance
- Reversed Disconnect Polarity

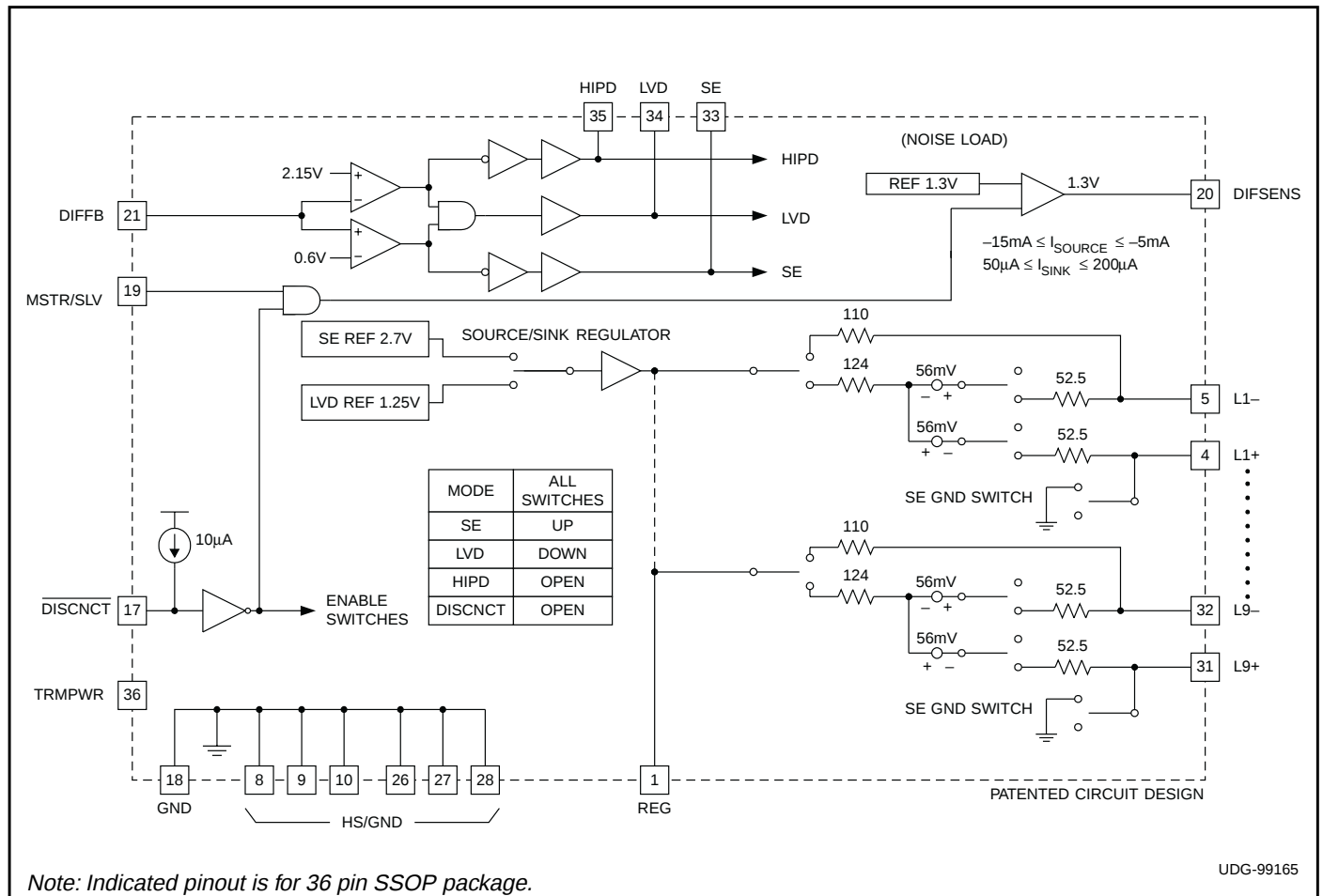
DESCRIPTION

The UCC5631A Multimode SCSI Terminator provides a smooth transition into the next generation of the SCSI Parallel Interface (SPI-2). It automatically senses the bus, via DIFFB, and switches the termination to either single ended (SE) or low voltage differential (LVD) SCSI, dependent on which type of devices are connected to the bus. The UCC5631A can not be used on a HVD, EIA485, differential SCSI bus. If the UCC5631A detects a HVD SCSI device, it switches to a high impedance state.

The Multimode terminator contains all functions required to terminate and auto detect and switch modes for SPI-2 bus architectures. Single Ended and Differential impedances and currents are trimmed for maximum effectiveness. Fail Safe biasing is provided to insure signal integrity. Device/Bus type detection circuitry is integrated into the terminator to provide automatic switching of termination between single ended and LVD SCSI and a high impedance for HVD SCSI. The multimode function provides all the performance analog functions necessary to implement SPI-2 termination in a single monolithic device.

The UCC5631A is offered in a 36 pin SSOP package, as well as a 48 pin LQFP package for a temperature range of 0°C to 70°C.

BLOCK DIAGRAM



UDG-99165

ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage 6V
 Signal Line Voltage 0V to TRMPWR
 Package Power Dissipation 2W
 Storage Temperature -65°C to +150°C
 Junction Temperature -55°C to +150°C
 Lead Temperature (Soldering, 10sec.) +300°C

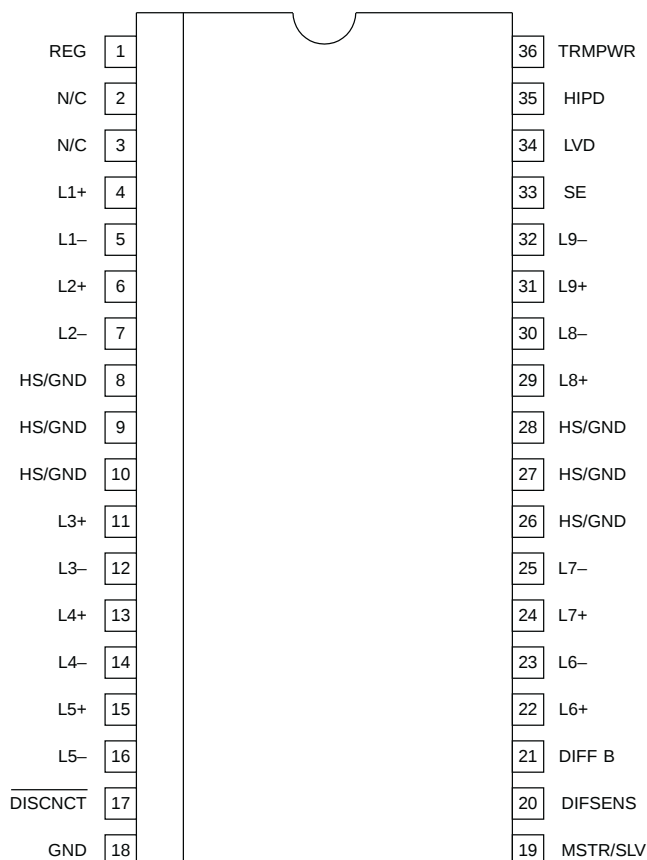
All voltages are with respect to pin 18. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

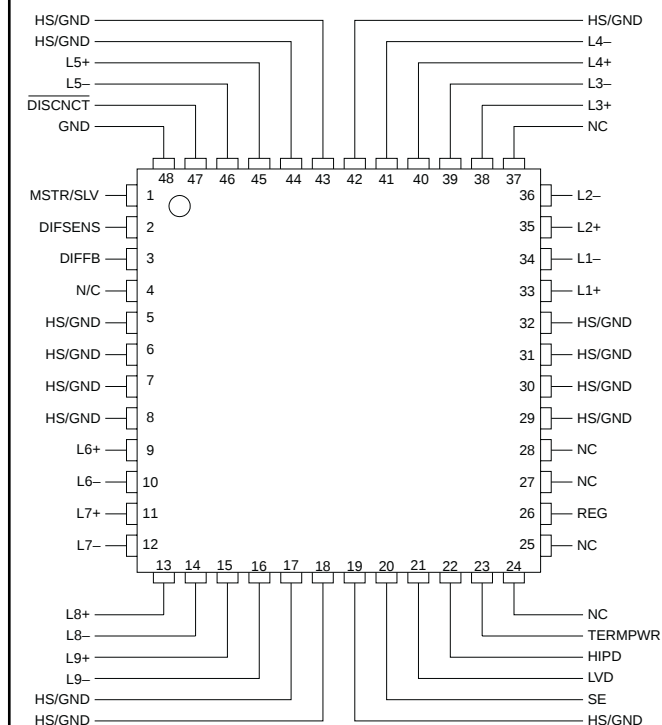
TRMPWR Voltage 2.7V to 5.25V

CONNECTION DIAGRAM

QSOP-36 (Top View)
MWP Package



LQFP-48 (Top View)
FQP Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0^\circ\text{C}$ to 70°C ,
TRMPWR = 2.7V to 5.25V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current	LVD Mode (No Load)		13	20	mA
	SE Mode (No Load)		1.6	10	mA
	Disabled		250	400	μA
Regulator Section					
REG Output Voltage (LVD Mode)	$0.5\text{V} \leq V_{\text{CM}} \leq 2.0\text{V}$ (Note1)	1.15	1.25	1.35	V
REG Output Voltage (SE Mode)	$0\text{V} \leq V_{\text{L-}} \leq 4.2\text{V}$ (Note2)	2.5	2.7	3.0	V
REG Short-Circuit Source Current (LVD and SE Modes)	$V_{\text{REG}} = 0\text{V}$	-800	-420	-225	mA
REG Short-Circuit Sink Current (LVD and SE Modes)	$V_{\text{REG}} = 3.0\text{V}$	100	180	800	mA
DIFSENS Output Section					
Output Voltage	$-5\text{mA} \leq I_{\text{DIFSENS}} \leq 50\mu\text{A}$	1.2	1.3	1.4	V
Short-Circuit Source Current	$V_{\text{DIFSENS}} = 0\text{V}$	-15	-8	-5	mA
Short-Circuit Sink Current	$V_{\text{DIFSENS}} = 2.75\text{V}$	50	80	200	μA
Differential Termination Section (Applies to each line pair, 1-9, in LVD mode)					
Differential Impedance		100	105	110	Ω
Common Mode Impedance	L+ and L- shorted together. (Note 3)	110	140	165	Ω
Differential Bias Voltage		100		125	mV
Common Mode Bias Voltage	L+ and L- shorted together.	1.15	1.25	1.35	V
Output Capacitance	Single ended measurement to ground. (Note 4)			3	pF
Single Ended Termination Section (Applies to each line pair, 1-9, in SE mode)					
Impedance	(Note 5)	102.3	110	117.7	Ω
Termination Current	Signal Level 0.2V	-25.4		-21	mA
	Signal Level 0.5V	-22.4		-18	mA
Output Capacitance	Single ended measurement to ground. (Note 4)			3	pF
Single Ended GND Switch Impedance	$I = 10\text{mA}$		20	60	Ω
Disconnected Termination Section (Applies to each line pair, 1-9, in DISCNCT or HIPD mode)					
Output Leakage				400	nA
Output Capacitance	Single ended measurement to ground. (Note 4)			3	pF
DISCNCT and DIFFB Input Section					
DISCNCT Threshold		0.8		2.0	V
DISCNCT Input Current	$V_{\text{DISCNCT}} = 0\text{V}$	-30	-10	-3	μA
DIFFB Single Ended to LVD Threshold		0.5		0.7	V
DIFFB LVD to HIPD Threshold		1.9		2.4	V
DIFFB Input Current	$0\text{V} \leq V_{\text{DIFFB}} \leq 2.75\text{V}$	-1		1	μA

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0^\circ\text{C}$ to 70°C , $V_{\text{TRMPWR}} = 2.7\text{V}$ to 5.25V .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Master/Slave (MSTR/SLV) Input Section					
MSTR/SLV Threshold	$V_{\text{TRMPWR}} = 2.7\text{V}$	0.8		1.9	V
	$V_{\text{TRMPWR}} = 3.3\text{V}$	1		2.4	V
	$V_{\text{TRMPWR}} = 5.25\text{V}$	1.5		3.7	V
MSTR/SLV Input Current		-1		1	μA
Status Bits (SE, LVD, HIPD) Output Section					
I_{SOURCE}	$V_{\text{LOAD}} = 2.4\text{V}$		-8.7	-4	mA
I_{SINK}	$V_{\text{LOAD}} = 0.5\text{V}$	3	6		mA
	$V_{\text{LOAD}} = 0.4\text{V}$	2	5		mA

Note 1: V_{CM} is applied to all L+ and L- lines simultaneously.

Note 2: $V_{\text{L-}}$ is applied to all L- lines simultaneously.

Note 3: $Z_{\text{CM}} = \frac{(2.0\text{V} - 0.5\text{V})}{I_{(\text{at } V_{\text{CM}} = 2\text{V})} - I_{(\text{at } V_{\text{CM}} = 0.5\text{V})}};$

Note 4: Guaranteed by design. Not 100% tested in production.

Note 5: $Z = \frac{(V_{\text{L}(X)} - 0.2\text{V})}{I_{\text{L}(X)}};$ where

$V_{\text{L}(X)}$ = Output voltage for each terminator minus output pin (L1- through L9-) with each pin unloaded.

$I_{\text{L}(X)}$ = Output current for each terminator minus output pin (L1- through L9-) with the minus output pin forced to 0.2V.

PIN DESCRIPTIONS

DIFFB: Input pin for the comparators that select SE, LVD, or HIPD modes of operation. This pin should be decoupled with a $0.1\mu\text{F}$ capacitor to ground and then coupled to the DIFSENS pin through a $20\text{k}\Omega$ resistor.

DIFSENS: Connects to the Diff Sense line of the SCSI bus. The bus mode is controlled by the voltage level on this pin.

DISNCT: Input pin used to shut down the terminator if the terminator is not connected at the end of the bus. Connect this pin to ground to disable the terminator or open pin to activate the terminator.

HIPD: TTL compatible status bit. This output pin is high when a high voltage differential device is detected on the bus.

HS/GND: Heat sink ground pins. These should be connected to large area PC board traces to increase the power dissipation capability.

GND: Power Supply return.

L1- thru L9-: Termination lines. These are the active lines in SE mode and are the negative lines for LVD mode. In HIPD mode, these lines are high impedance.

L1+ thru L9+: Termination lines. These lines switch to ground in SE mode and are the positive lines for LVD mode. In HIPD mode, these lines are high impedance.

MSTR/SLV: If the terminator is enabled, this input pin enables / disables the DIFSENS driver, when connected to TRMPWR or ground respectively. When the terminator is disabled, the DIFSENS driver is off, independent of this input.

LVD: TTL compatible status bit. This output pin is high when the SCSI bus is in LVD mode.

REG: Regulator output bypass pin. This pin must be connected to a $4.7\mu\text{F}$ capacitor to ground.

SE: TTL compatible status bit. This output pin is high when the SCSI bus is in SE mode.

TRMPWR: 2.7V to 5.25V power input pin.

APPLICATION INFORMATION

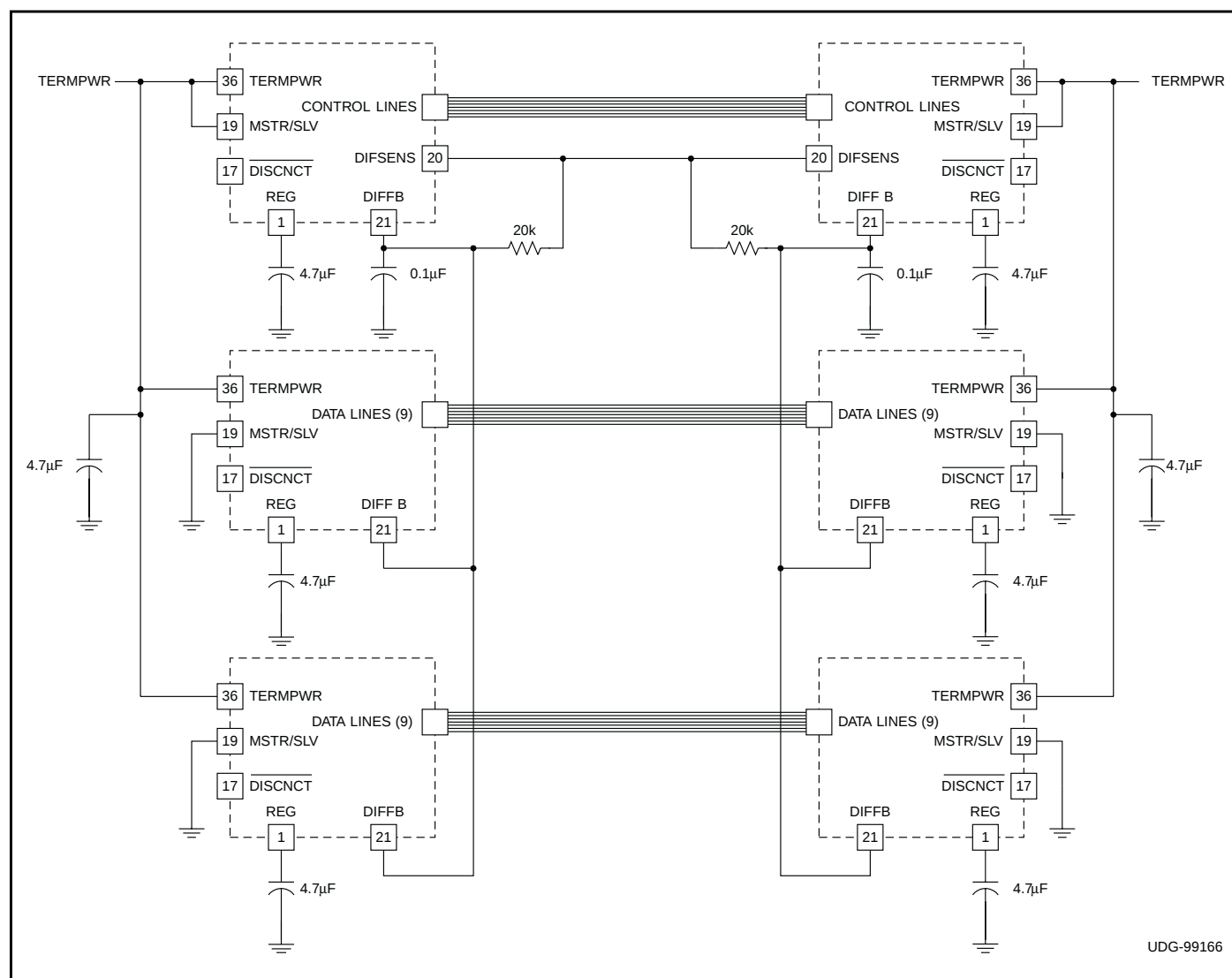


Figure 2. Application diagram.

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI devices are present on the bus.

The UCC5631A is used in multi-mode active termination applications, where single ended (SE) and low voltage differential (LVD) devices might coexist. The UCC5631A has both SE and LVD termination networks integrated into a single monolithic component. The correct termination network is automatically determined by the SCSI bus "DIFSENS" signal.

The SCSI bus DIFSENS signal line is used to identify which types of SCSI devices are present on the bus. On power-up, the UCC5631A DIFSENS drivers will try to deliver 1.3V to the DIFSENS line. If only LVD devices are present, the DIFSENS line will be successfully driven to 1.3V and the terminators will configure for LVD operation. If any single ended devices are present, they will present a short to ground on the DIFSENS line, signaling the UCC5631A(s) to configure into the SE mode, accommodating the SE devices. Or, if any high voltage differential (HVD) devices are present, the DIFSENS line is pulled high and the terminator will enter a high impedance state, effectively disconnecting from the bus.

APPLICATION INFORMATION (cont.)

The DIFSENS line is monitored by each terminator through a 50Hz noise filter at the DIFFB input pin. A set of comparators detect and select the appropriate termination for the bus as follows. If the DIFSENS signal is below 0.5V, the termination network is SE. Between 0.7V and 1.9V, the termination network switches to LVD, and above 2.4V is HVD, causing the terminators to disconnect from the bus. The thresholds accommodate differences in ground potential that can occur with long lines.

Three UCC5631A multi-mode parts are required at each end of the bus to terminate 27 (18 data, plus 9 control) lines. Each part includes a DIFSENS driver, but only one is necessary to drive the line. A MSTR/SLV input pin is provided to disable the other two. The "master" part must have its' MSTR/SLV pin connected to TRMPWR and the two "slave" parts must have the MSTR/SLV inputs grounded. Only the "master" is connected directly to the SCSI bus DIFSENS line. The DIFFB inputs on all three parts are connected together, allowing them to share the same 50Hz noise filter. This multi-mode terminator operates in full specification down to 2.7V TRMPWR voltage. This accommodates 3.3V systems, with allowance for the 3.3V supply tolerance (+/- 10%), a unidirectional fusing device and cable drop. In 3.3V TRMPWR systems, the UCC3912 is recommended in place of the fuse and diode. The UCC3912's lower voltage drop allows additional margin over the fuse and diode, for the far end terminator.

Layout is critical for Ultra2 and Ultra3 systems. The SPI-2 standard for capacitance loading is 10pF maximum from each positive and negative signal line to ground, and a maximum of 5pF between the positive and negative signal lines of each pair is allowed. These maximum capacitances apply to differential bus termination circuitry that is not part of a SCSI device, (e.g. a cable terminator). If the termination circuitry is included as part of a SCSI device, (e.g., a host adaptor, disk or tape drive), then the corresponding requirements are 30pF maximum from each positive and negative signal line to ground and 15pF maximum between the positive and negative signal lines of each pair.

The SPI-2 standard for capacitance balance of each pair and balance between pairs is more stringent. The standard is 0.75pF maximum difference from the positive and negative signal lines of each pair to ground. An additional

requirement is a maximum difference of 2pF when comparing pair to pair. These requirements apply to differential bus termination circuitry that is not part of a SCSI device. If the termination circuitry is included as part of a device, then the corresponding balance requirements are 2.25pF maximum difference within a pair, and 3pF from pair to pair.

Feed-throughs, through-hole connections, and etch lengths need to be carefully balanced. Standard multi-layer power and ground plane spacing add about 1pF to each plane. Each feed-through will add about 2.5pF to 3.5pF. Enlarging the clearance holes on both power and ground planes will reduce the capacitance. Similarly, opening up the power and ground planes under the connector will reduce the capacitance for through-hole connector applications. Capacitance will also be affected by components, in close proximity, above and below the circuit board.

Unitrode multi-mode terminators are designed with very tight balance, typically 0.1pF between pins in a pair and 0.3pF between pairs. At each L+ pin, a ground driver drives the pin to ground, while in single ended mode. The ground driver is specially designed to not effect the capacitive balance of the bus when the device is in LVD or disconnect mode.

Multi-layer boards need to adhere to the 120Ω impedance standard, including the connectors and feed-throughs. This is normally done on the outer layers with 4 mil etch and 4 mil spacing between runs within a pair, and a minimum of 8 mil spacing to the adjacent pairs to reduce crosstalk. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50Ω rather than 120Ω differential systems. Careful consideration must be given to the issue of heat management. A multi-mode terminator, operating in SE mode, will dissipate as much as 130mW of instantaneous power per active line with TRMPWR = 5.25V. The UCC5631A is offered in a 36 pin SSOP and a 48 lead LFQP. Both packages include heat sink ground pins. These heat sink/ground pins are directly connected to the die mount paddle under the die and conduct heat from the die to reduce the junction temperature. All of the HS/GND pins need to be connected to etch area or a feed-through per pin connecting to the ground plane layer on a multi-layer board.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UCC5631AMWP	ACTIVE	SSOP	DCE	36	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC5631AMWPG4	ACTIVE	SSOP	DCE	36	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC5631AMWPTR	ACTIVE	SSOP	DCE	36	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC5631AMWPTRG4	ACTIVE	SSOP	DCE	36	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

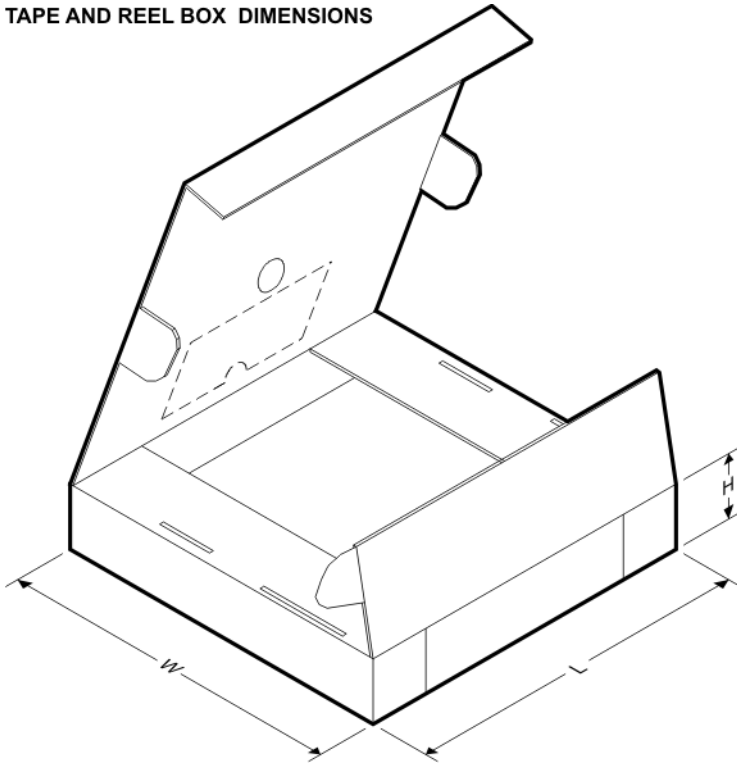
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5631AMWPTR	SSOP	DCE	36	1000	330.0	24.4	10.85	15.8	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5631AMWPTR	SSOP	DCE	36	1000	346.0	346.0	41.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated