

SN74CBTK16245
16-BIT FET BUS SWITCH
WITH ACTIVE-CLAMP UNDERSHOOT-PROTECTION CIRCUIT
SCDS105D – APRIL 2000 – REVISED NOVEMBER 2001

- Member of the Texas Instruments Widebus™ Family
- Standard '16245-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- I_{off} Supports Partial-Power-Down Mode Operation
- Active-Clamp Undershoot-Protection Circuit on the I/Os Clamps Undershoots up to -2 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description

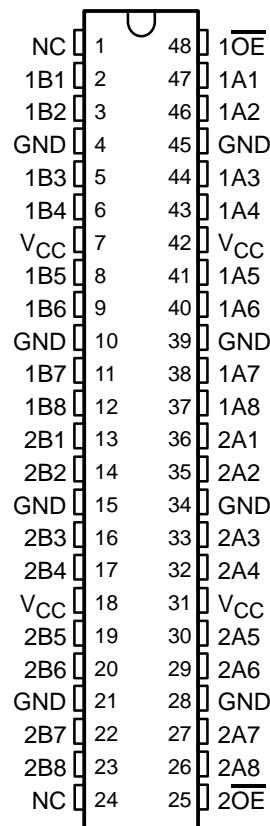
The SN74CBTK16245 device provides 16 bits of high-speed TTL-compatible bus switching in a standard '16245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The A and B ports have an active-clamp undershoot-protection circuit. When there is an undershoot, the active-clamp circuit is enabled, and current from V_{CC} is supplied to clamp the output, preventing the pass transistor from turning on.

The device is organized as two 8-bit low-impedance switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on, and data can flow from the A port to the B port, or vice versa. When \overline{OE} is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBTK16245DL	CBTK16245
		Tape and reel	SN74CBTK16245DLR	
	TSSOP – DGG	Tape and reel	SN74CBTK16245DGGR	CBTK16245
	TVSOP – DGV	Tape and reel	SN74CBTK16245DGVR	CP245

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

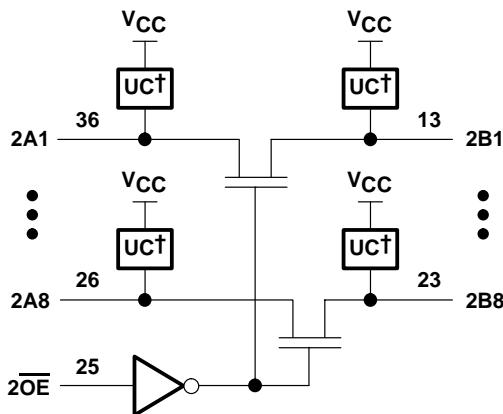
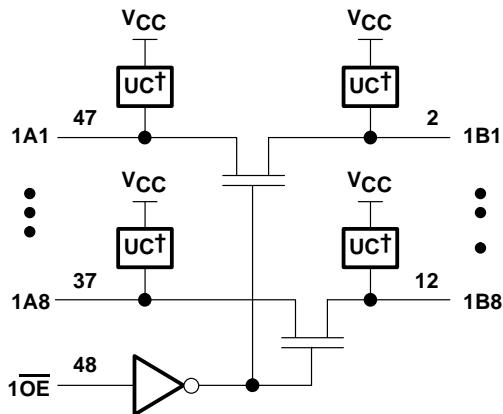
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FUNCTION TABLE
(each 8-bit bus switch)

INPUT OE	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)

† Undershoot clamp

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, T_{STG}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT	
V_{IK}	$V_{CC} = 4.5 \text{ V}$,	$I_I = -18 \text{ mA}$				-1.2	V	
V_{IKU}	$V_{CC} = 5.5 \text{ V}$,	$0 \text{ mA} \geq I_I \geq -50 \text{ mA}$,	$\overline{OE} = 5.5 \text{ V}$			-2	V	
I_I	$V_{CC} = 0$,	$V_I = 5.5 \text{ V}$				10	μA	
	$V_{CC} = 5.5 \text{ V}$,	$V_I = 5.5 \text{ V or GND}$				± 1		
I_{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 5.5 V				20	μA	
I_{CC}	$V_{CC} = 5.5 \text{ V}$,	$V_I = V_{CC}$ or GND,	$I_O = 0$			3	μA	
$\Delta I_{CC}^{\$}$	Control inputs	$V_{CC} = 5.5 \text{ V}$,	One input at 3.4 V ,	Other inputs at V_{CC} or GND		2.5	mA	
C_i	Control inputs	$V_I = 3 \text{ V or } 0$				3.5	pF	
$C_{io(OFF)}$		$V_O = 3 \text{ V or } 0$,	$\overline{OE} = V_{CC}$			5.5	pF	
r_{on}^{\parallel}	$V_{CC} = 4 \text{ V}$, TYP at $V_{CC} = 4 \text{ V}$	$V_I = 2.4 \text{ V}$,	$I_I = 15 \text{ mA}$			14	20	Ω
	$V_{CC} = 4.5 \text{ V}$	$V_I = 0$	$I_I = 64 \text{ mA}$			5	7	
			$I_I = 30 \text{ mA}$			5	7	
		$V_I = 2.4 \text{ V}$,	$I_I = 15 \text{ mA}$			8	12	

[‡]All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ This is the increase in supply current for each input that is at the specified TTL-voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} [†]	A or B	B or A	0.35		0.25		ns
t _{en}	OE	A or B	7.4	1.6	4.9		ns
t _{dis}	OE	A or B	7.4	4.2	7.5		ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{OUTU}	See Figures 1 and 2, and Table 1	2	$V_{OH}-0.3$		V

† All typical values are at $V_{CC} = 5$ V (unless otherwise noted), $T_A = 25^\circ\text{C}$.

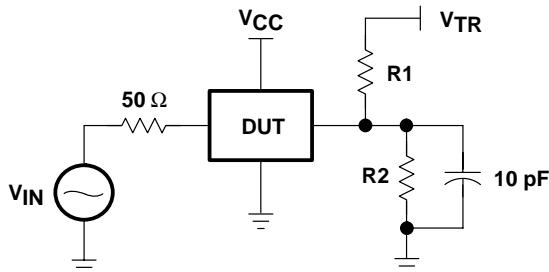


Figure 1. Device Test Setup

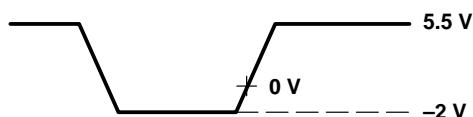


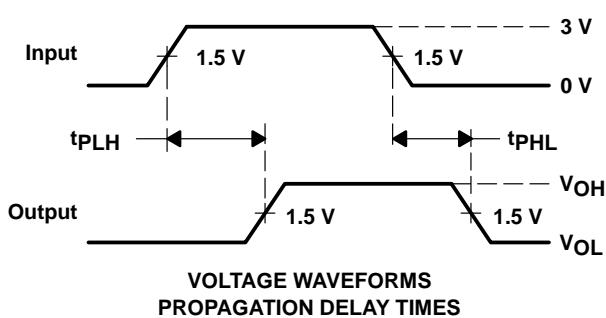
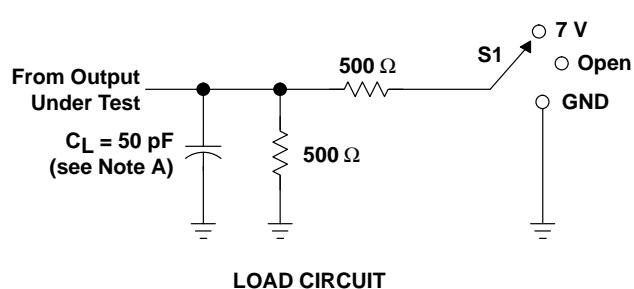
Figure 2. Transient Input Voltage Waveform

Table 1. Device Test Conditions

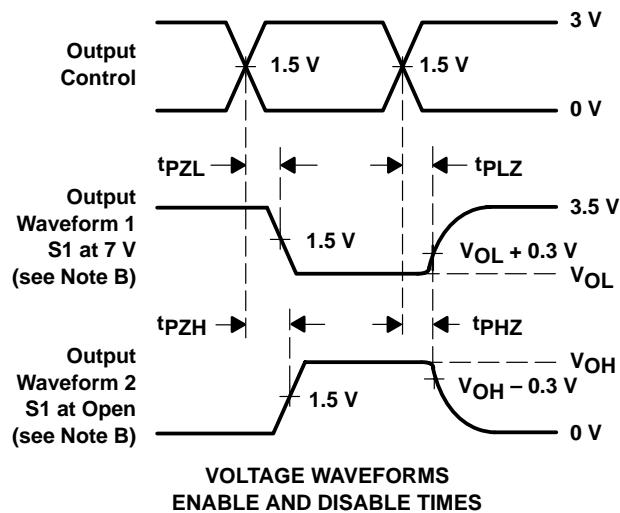
PARAMETER	VALUE	UNIT
B port under test	See Figure 1	
V_{IN}	See Figure 2	V
t_W	20	ns
t_r	2	ns
t_f	2	ns
$R_1 = R_2$	100	$k\Omega$
V_{TR}	11	V
V_{CC}	5.5	V

§ Other B-port outputs are open.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



NOTES:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CBTK16245DGGRE4	OBsolete	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85		
74CBTK16245DGGRG4	OBsolete	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85		
74CBTK16245DGVR4	OBsolete	TVSOP	DGV	48		TBD	Call TI	Call TI	-40 to 85		
74CBTK16245DGVRG4	OBsolete	TVSOP	DGV	48		TBD	Call TI	Call TI	-40 to 85		
74CBTK16245DLRG4	OBsolete	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85		
SN74CBTK16245DGGR	OBsolete	TSSOP	DGG	48		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTK16245	
SN74CBTK16245DGVR	OBsolete	TVSOP	DGV	48		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CP245	
SN74CBTK16245DL	OBsolete	SSOP	DL	48		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTK16245	
SN74CBTK16245DLR	OBsolete	SSOP	DL	48		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTK16245	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

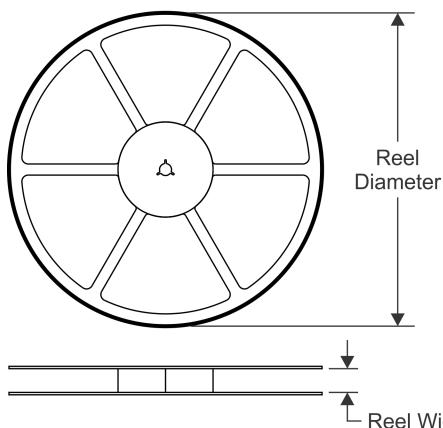
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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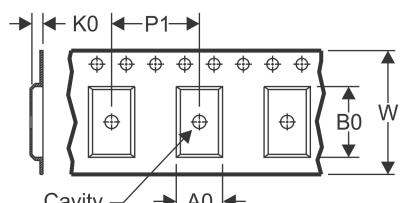
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

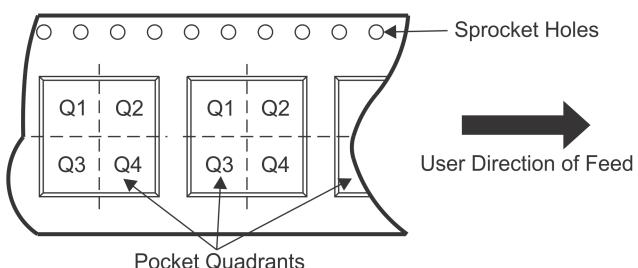


TAPE DIMENSIONS



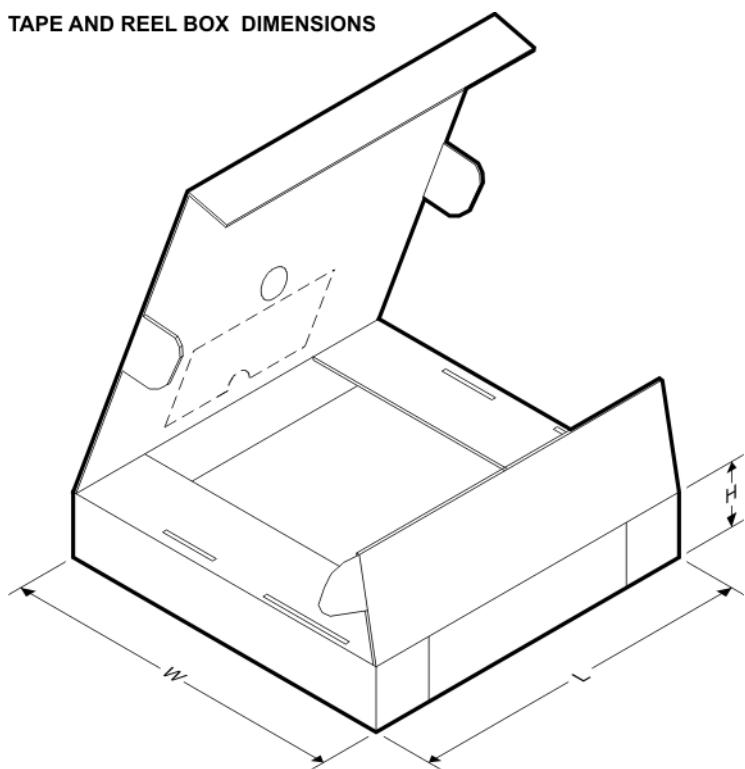
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

All dimensions are nominal													
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant	
SN74CBTK16245DGGR	TSSOP	DGG	48	0	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1	
SN74CBTK16245DGVR	TVSOP	DGV	48	0	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1	
SN74CBTK16245DLR	SSOP	DL	48	0	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1	

TAPE AND REEL BOX DIMENSIONS


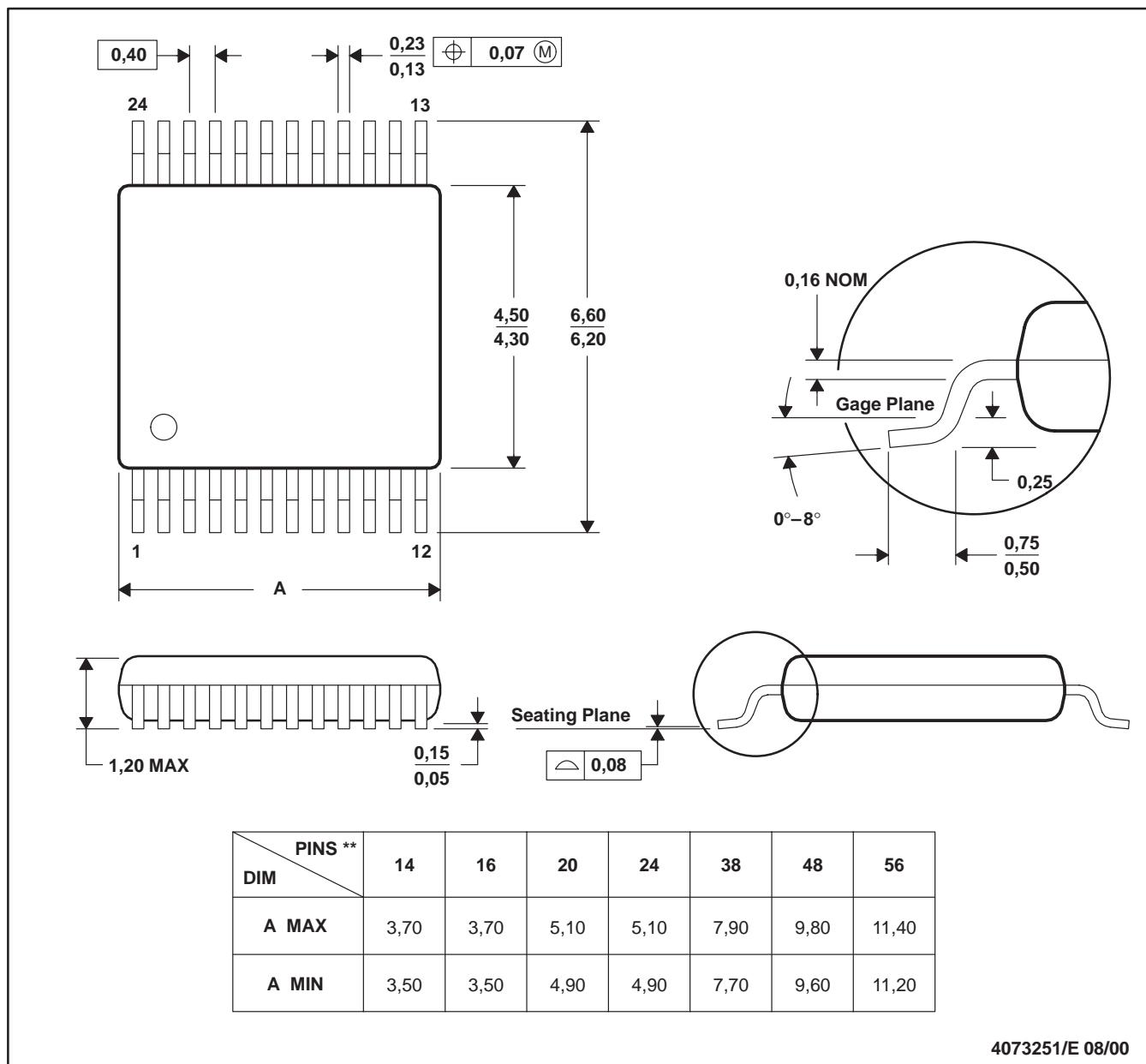
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTK16245DGGR	TSSOP	DGG	48	0	367.0	367.0	45.0
SN74CBTK16245DGVR	TVSOP	DGV	48	0	367.0	367.0	38.0
SN74CBTK16245DLR	SSOP	DL	48	0	367.0	367.0	55.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

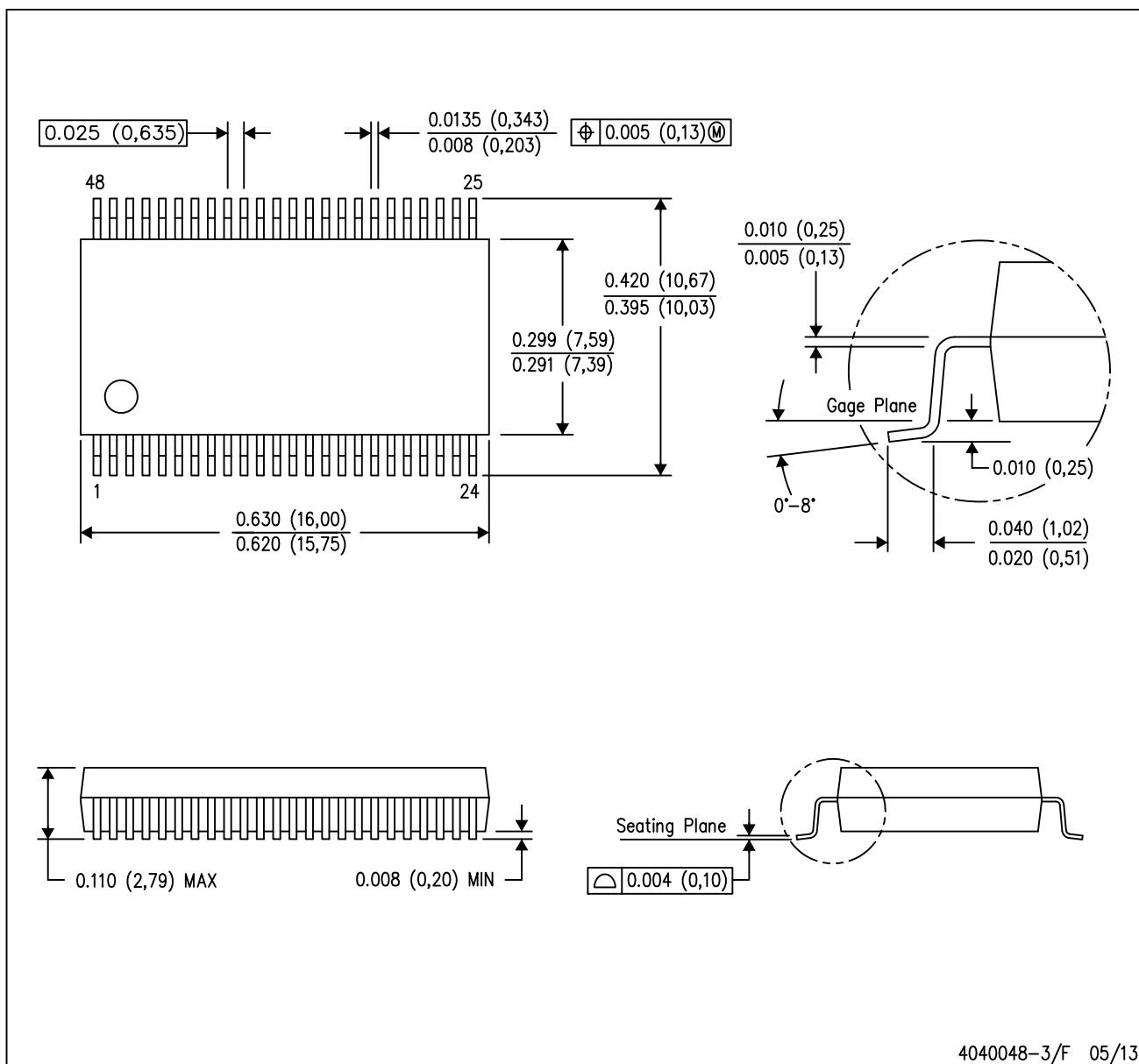
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



4040048-3/F 05/13

NOTES:

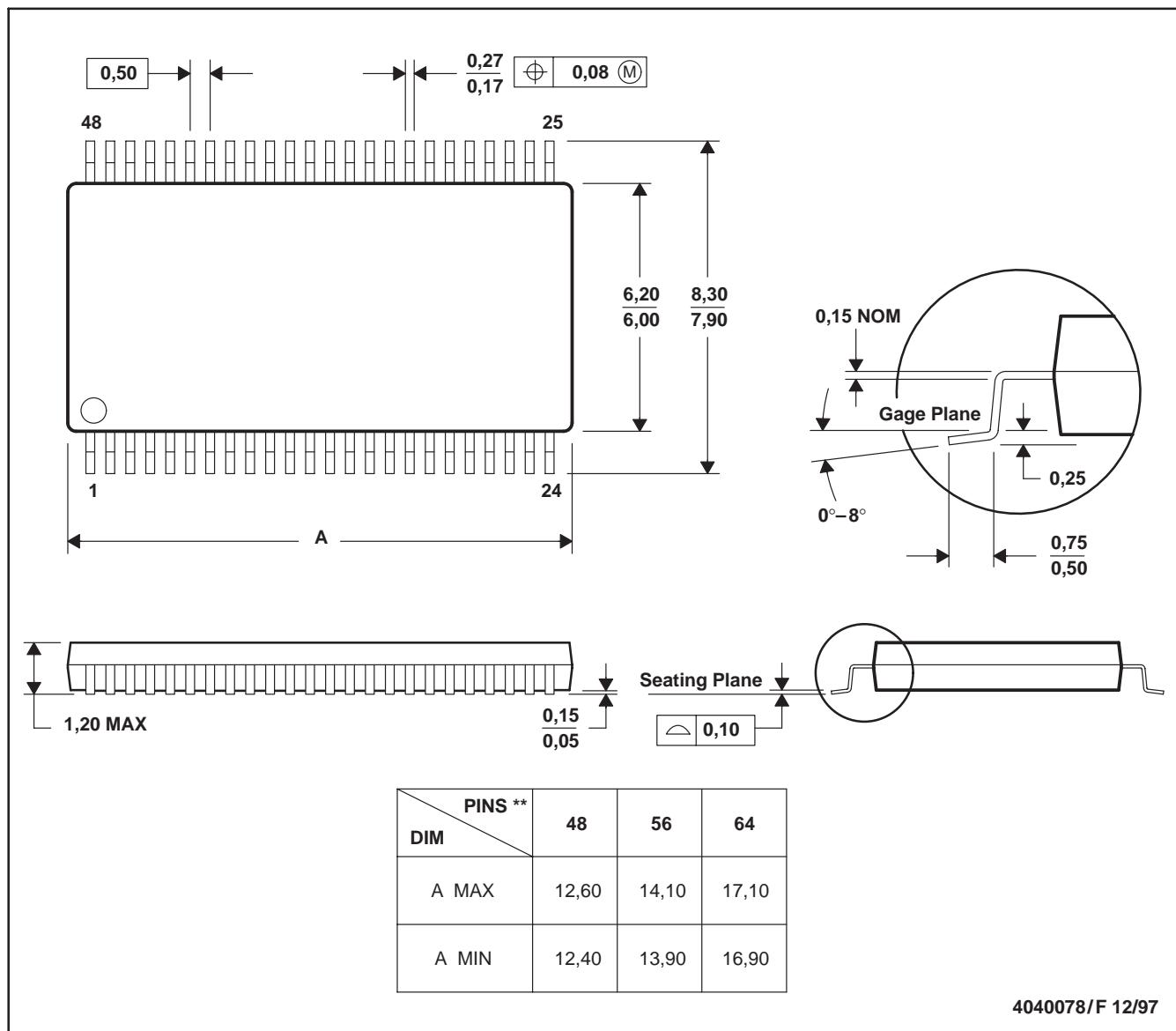
- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MO-118

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DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



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 D. Falls within JEDEC MO-153

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