LM4923 Boomer® Audio Power Amplifier Series 1.1 Watt Fully Differential Audio Power Amplifier With Shutdown Select

Check for Samples: LM4923, LM4923LQBD

FEATURES

- **Fully Differential Amplification**
- **Available in Space-saving WQFN Package**
- **Ultra Low Current Shutdown Mode**
- **Can Drive Capacitive Loads up to 100pF**
- **Improved Pop & Click Circuitry Eliminates Noises During Turn-on and Turn-off Transitions**
- **2.4 - 5.5V Operation**
- **No Output Coupling Capacitors, Snubber Networks or Bootstrap Capacitors Required**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Portable Electronic Devices**

KEY SPECIFICATIONS

- **Improved PSRR at 217Hz 85dB(typ)**
- **Power Output at 5.0V @ 1% THD+N 1.1W(typ)**
- **Power Output at 3.3V @ 1% THD+N 400mW(typ)**
- **Shutdown Current 0.1µA(typ)**

DESCRIPTION

The LM4923 is a fully differential audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1.1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a $5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4923 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4923 features a low-power consumption shutdown mode. To facilitate this, Shutdown may be enabled by logic low. Additionally, the LM4923 features an internal thermal shutdown protection mechanism.

The LM4923 contains advanced pop & click circuitry which eliminates noises which would otherwise occur during turn-on and turn-off transitions.

Connection Diagrams

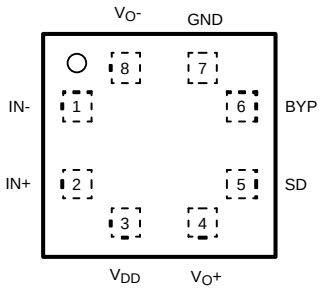


Figure 1. NGP Package, Top View
See Package Number NGP0008A

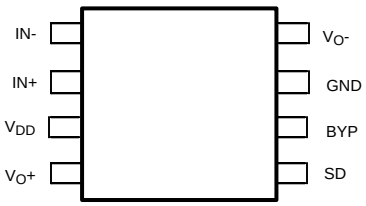


Figure 2. 8 Pin VSSOP Package, Top View
See Package Number DGK0008A

Typical Application

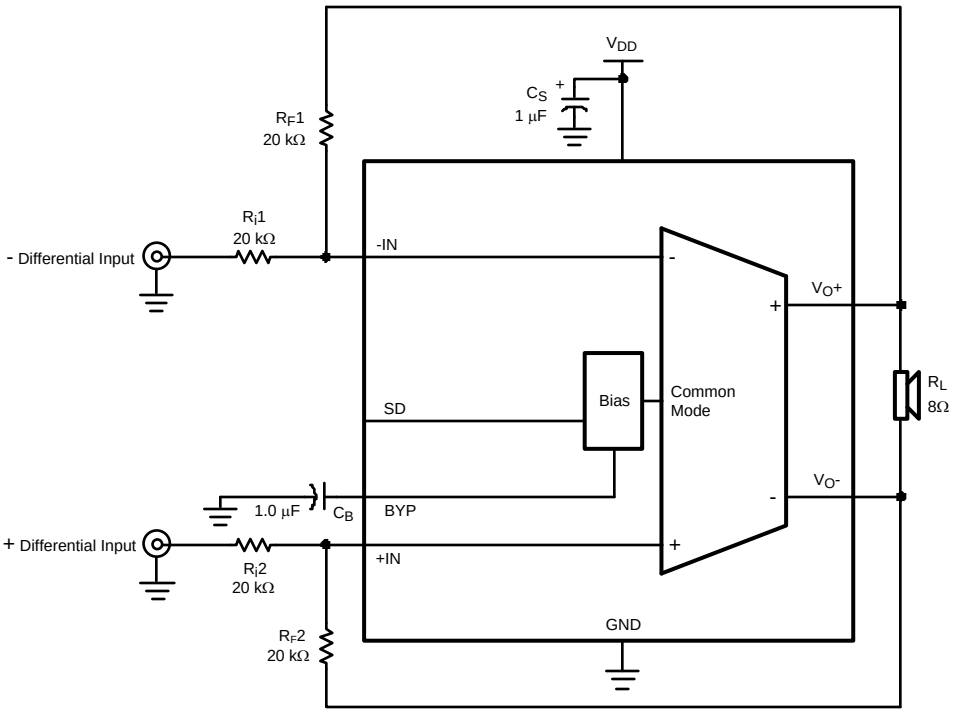


Figure 3. Typical Audio Amplifier Application Circuit

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation(3)		Internally Limited
ESD Susceptibility(4)		2000V
ESD Susceptibility(5)		200V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} (WQFN)	140°C/W
	θ_{JA} (DGK)	210°C/W
	θ_{JC} (DGK)	56°C/W
Soldering Information		
See AN-1187 (SNOA401)		

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4923, see power derating curve for additional information.

(4) Human body model, 100pF discharged through a 1.5kΩ resistor.

(5) Machine Model, 220pF – 240pF discharged through all pins.

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage	$2.4V \le V_{DD} \le 5.5V$

Electrical Characteristics V_{DD} = 5V(1)(2)

The following specifications apply for V_{DD} = 5V, A_V = 1, and 8Ω load unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4923		Units (Limits)
			Typical(3)	Limit(4)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, no load V_{IN} = 0V, R_L = 8Ω	4 4	9 9	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1	1	µA (max)
P_o	Output Power	THD = 1% (max); f = 1 kHz			
		LM4923, R_L = 8Ω	1.1	1	
THD+N	Total Harmonic Distortion+Noise	P_o = 0.4 Wrms; f = 1kHz	0.02		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p			
		f = 217Hz(5)	85	73	
		f = 1kHz(5)	85	73	
CMRR	Common_Mode Rejection Ratio	f = 217Hz, V_{CM} = 200mV_{pp}	50		dB
V_{OS}	Output Offset	V_{IN} = 0V	4		mV
V_{SDIH}	Shutdown Voltage Input High		0.9		V
V_{SDIL}	Shutdown Voltage Input Low		0.7		V

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(5) 10Ω terminated input.

Electrical Characteristics V_{DD} = 3V(1) (2)

The following specifications apply for V_{DD} = 3V, A_V = 1, and 8Ω load unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4923		Units (Limits)
			Typical(3)	Limit(4)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, no load V_{IN} = 0V, R_L = 8Ω	3 3	5.5 5.5	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1	1	µA (max)
P_o	Output Power	THD = 1% (max); f = 1kHz LM4923, R_L = 8Ω	0.375		W
THD+N	Total Harmonic Distortion+Noise	P_o = 0.25Wrms; f = 1kHz	0.02		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p			
		f = 217Hz (5)	85		
		f = 1kHz (5)	85	73	
CMRR	Common-Mode Rejection Ratio	f = 217Hz V_{CM} = 200mV_{pp}	50		dB
V_{OS}	Output Offset	V_{IN} = 0V	4		mV
V_{SDIH}	Shutdown Voltage Input High		0.8		V
V_{SDIL}	Shutdown Voltage Input Low		0.6		V

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(5) 10Ω terminated input.

EXTERNAL COMPONENTS DESCRIPTION

(Figure 3)

Components		Functional Description
1.	R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f.
2.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i.
3.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the Power Supply Bypassing section for information concerning proper placement and selection of the supply bypass capacitor.
4.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, Proper Selection of External Components, for information concerning proper placement and selection of C_B.

Typical Performance Characteristics

THD+N vs Frequency V_{DD} = 2.6V, R_L = 8Ω, P_O = 150mW

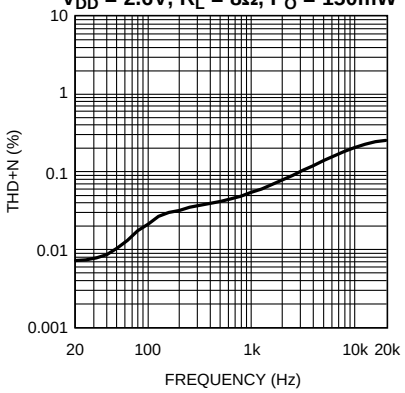


Figure 4.

THD+N vs Frequency V_{DD} = 2.6V, R_L = 4Ω, P_O = 150mW

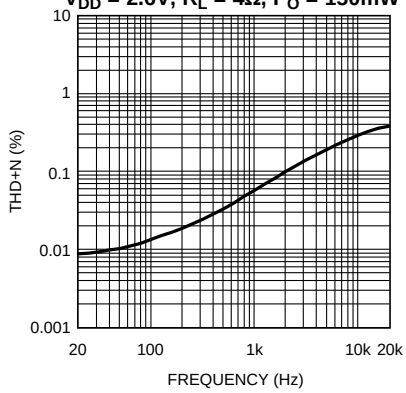


Figure 5.

THD+N vs Frequency V_{DD} = 5V, R_L = 8Ω, P_O = 400mW

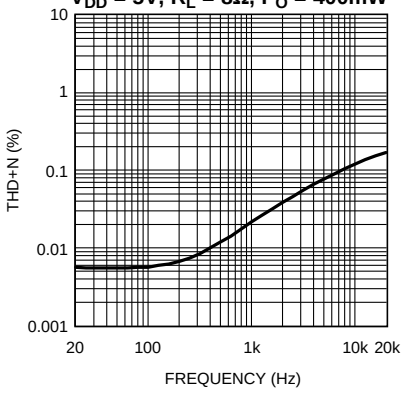


Figure 6.

THD+N vs Frequency V_{DD} = 3V, R_L = 8Ω, P_O = 275mW

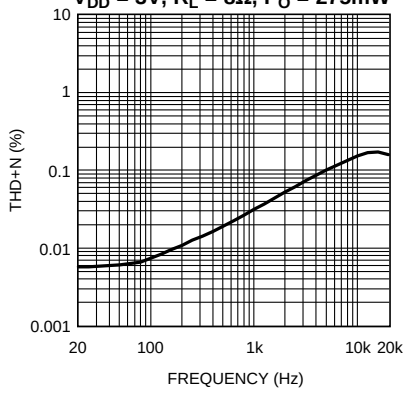


Figure 7.

THD+N vs Frequency V_{DD} = 3V, R_L = 4Ω, P_O = 225mW

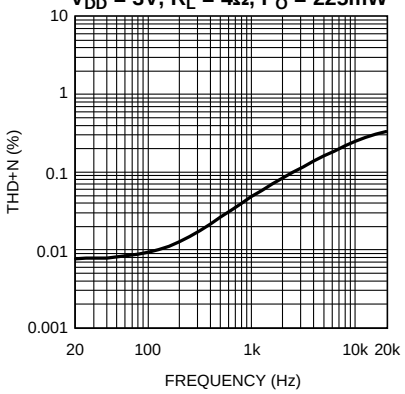


Figure 8.

THD+N vs Output Power V_{DD} = 2.6V, R_L = 8Ω

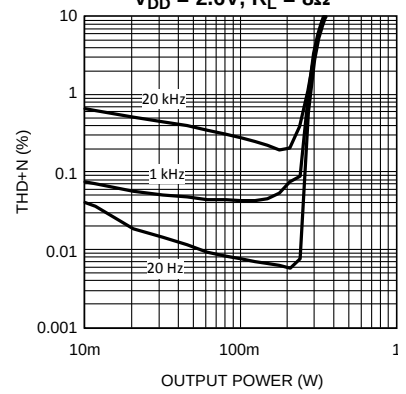


Figure 9.

Typical Performance Characteristics (continued)

THD+N vs Output Power V_{DD} = 2.6V, R_L = 4Ω

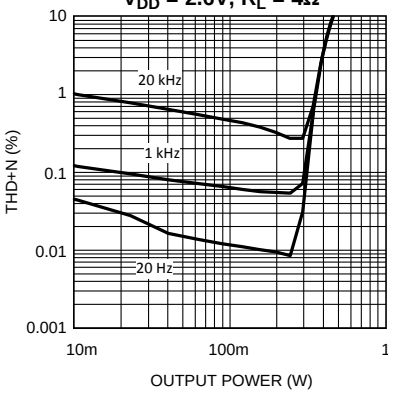


Figure 10.

THD+N vs Output Power V_{DD} = 5V, R_L = 8Ω

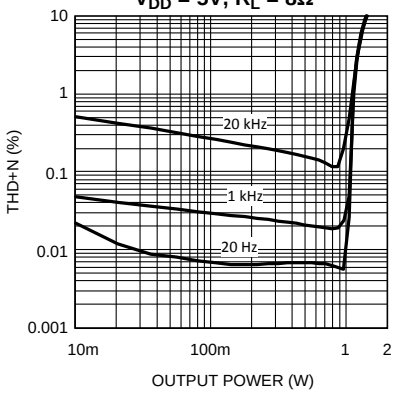


Figure 11.

THD+N vs Output Power V_{DD} = 3V, R_L = 8Ω

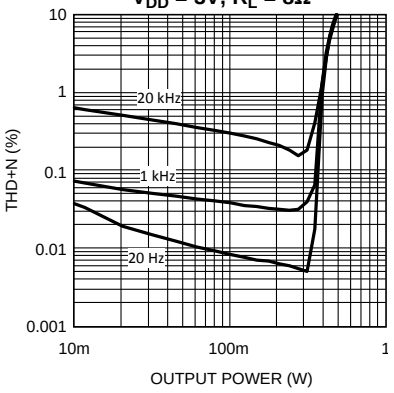


Figure 12.

THD+N vs Output Power V_{DD} = 3V, R_L = 4Ω

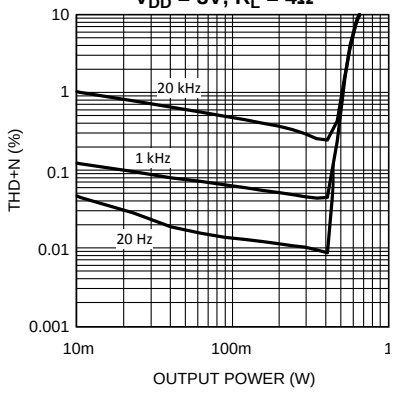


Figure 13.

PSRR vs Frequency V_{DD} = 5V, R_L = 8Ω, Input terminated

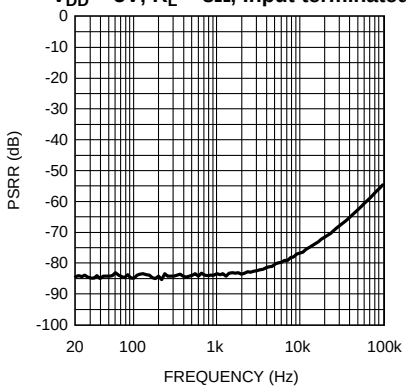


Figure 14.

PSRR vs Frequency V_{DD} = 3V, R_L = 8Ω, Input terminated

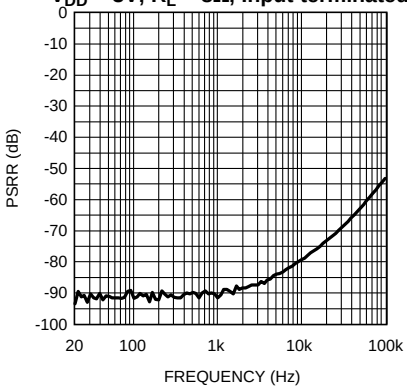


Figure 15.

Typical Performance Characteristics (continued)

Output Power vs Supply Voltage R_L = 8Ω

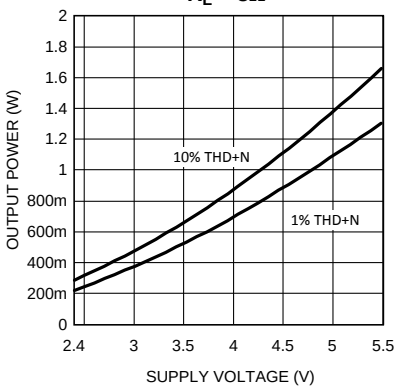


Figure 16.

CMRR vs Frequency V_{DD} = 5V, R_L = 8Ω

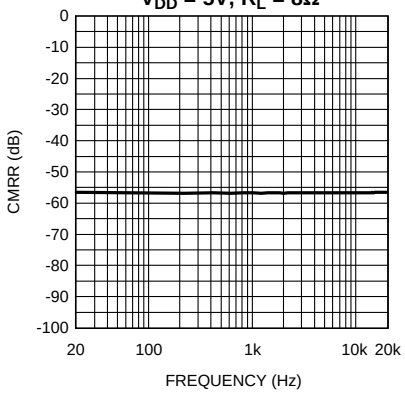


Figure 17.

CMRR vs Frequency V_{DD} = 3V, R_L = 8Ω

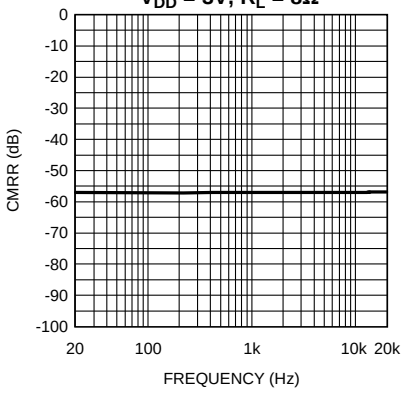


Figure 18.

PSRR vs Common Mode Voltage V_{DD} = 3V, R_L = 8Ω, f = 217Hz

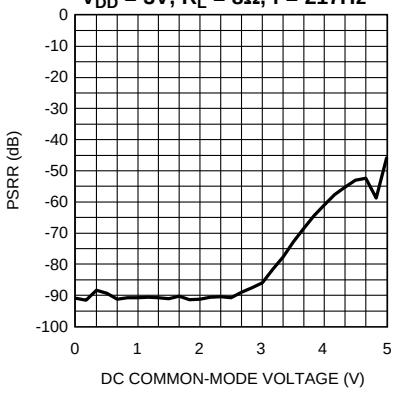


Figure 19.

PSRR vs Common Mode Voltage V_{DD} = 5V, R_L = 8Ω, f = 217Hz

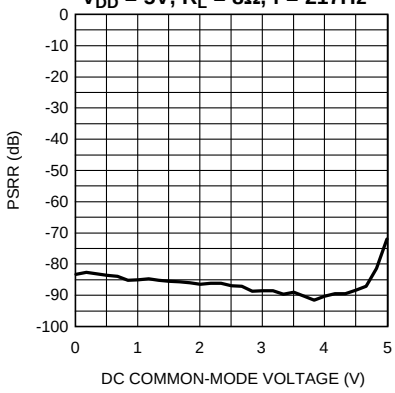


Figure 20.

Power Dissipation vs Output Power V_{DD} = 2.6V, R_L = 8Ω and 4Ω

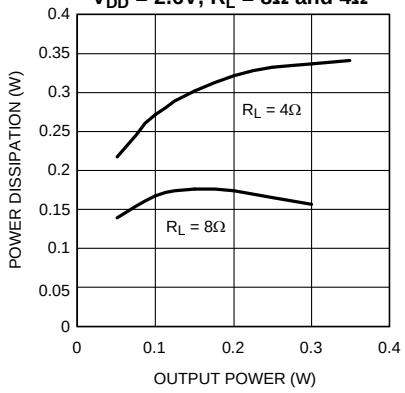


Figure 21.

Typical Performance Characteristics (continued)

Power Dissipation vs Output Power V_{DD} = 5V, R_L = 8Ω

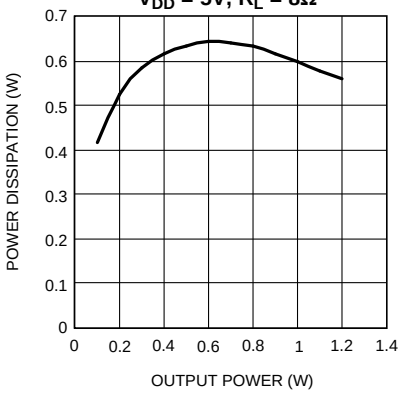


Figure 22.

Power Dissipation vs Output Power V_{DD} = 3V, R_L = 8Ω

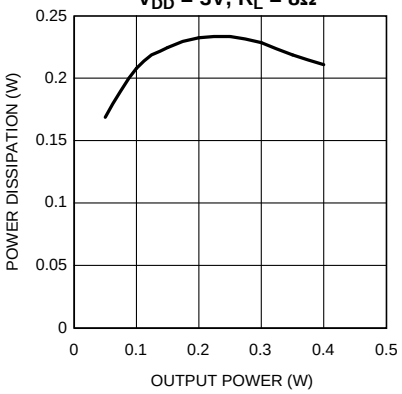


Figure 23.

Power Derating Curve

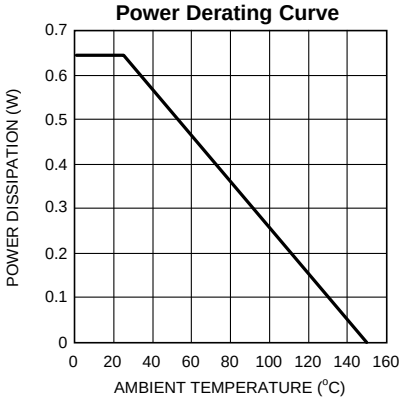


Figure 24.

Noise Floor V_{DD} = 5V

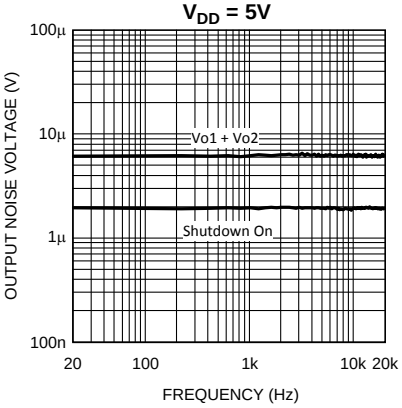


Figure 25.

Noise Floor V_{DD} = 3V

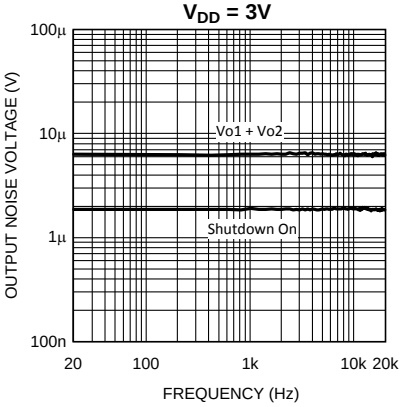


Figure 26.

Clipping Voltage vs Supply Voltage

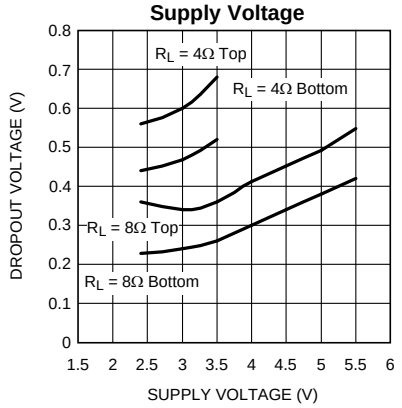


Figure 27.

Typical Performance Characteristics (continued)

Output Power vs Load Resistance

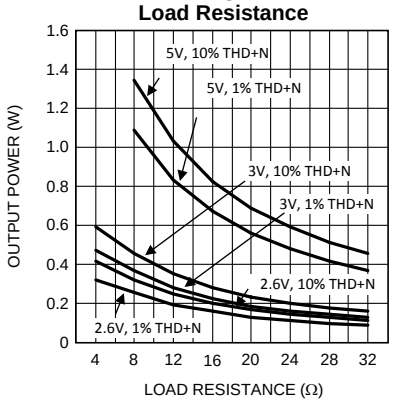


Figure 28.

Supply Current Shutdown Voltage

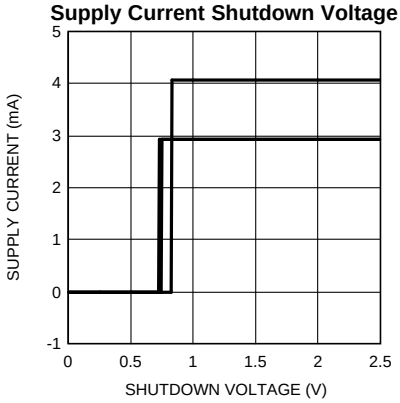


Figure 29.

APPLICATION INFORMATION

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM4923 is a fully differential audio amplifier that features differential input and output stages. Internally this is accomplished by two circuits: a differential amplifier and a common mode feedback amplifier that adjusts the output voltages so that the average value remains V_{DD} / 2. When setting the differential gain, the amplifier can be considered to have "halves". Each half uses an input and feedback resistor (R_{i1} and R_{F1}) to set its respective closed-loop gain (see Figure 1). With $R_{i1} = R_{i2}$ and $R_{F1} = R_{F2}$, the gain is set at $-R_F / R_i$ for each half. This results in a differential gain of

$$A_{VD} = -R_F/R_i \quad (1)$$

It is extremely important to match the input resistors to each other, as well as the feedback resistors to each other for best amplifier performance. See the Proper Selection of External Components section for more information. A differential amplifier works in a manner where the difference between the two input signals is amplified. In most applications, this would require input signals that are 180° out of phase with each other. The LM4923 can be used, however, as a single ended input amplifier while still retaining its fully differential benefits. In fact, completely unrelated signals may be placed on the input pins. The LM4923 simply amplifies the difference between them.

All of these applications provide what is known as a "bridged mode" output (bridge-tied-load, BTL). This results in output signals at V_{o1} and V_{o2} that are 180° out of phase with respect to each other. Bridged mode operation is different from the single-ended amplifier configuration that connects the load between the amplifier output and ground. A bridged amplifier design has distinct advantages over the single-ended configuration: it provides differential drive to the load, thus doubling maximum possible output swing for a specific supply voltage. Four times the output power is possible compared with a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excess clipping, please refer to the Audio Power Amplifier Design section.

A bridged configuration, such as the one used in the LM4923, also creates a second advantage over single-ended amplifiers. Since the differential outputs, V_{o1} and V_{o2}, are biased at half-supply, no net DC voltage exists across the load. This assumes that the input resistor pair and the feedback resistor pair are properly matched (see PROPER SELECTION OF EXTERNAL COMPONENTS). BTL configuration eliminates the output coupling capacitor required in single-supply, single-ended amplifier configurations. If an output coupling capacitor is not used in a single-ended output configuration, the half-supply bias across the load would result in both increased internal IC power dissipation as well as permanent loudspeaker damage. Further advantages of bridged mode operation specific to fully differential amplifiers like the LM4923 include increased power supply rejection ratio, common-mode noise reduction, and click and pop reduction.

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The LM4923's exposed-DAP (die attach paddle) package (WQFN) provide a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air. Failing to optimize thermal design may compromise the LM4923's high power performance and activate unwanted, though necessary, thermal shutdown protection. The WQFN package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with a thermal via. The via diameter should be 0.012in - 0.013in. Ensure efficient thermal conductivity by plating-through and solder-filling the vias.

Best thermal performance is achieved with the largest practical copper heat sink area. In all circumstances and conditions, the junction temperature must be held below 150°C to prevent activating the LM4923's thermal shutdown protection. Figure 24 in the Typical Performance Characteristics shows the maximum power dissipation versus temperature. Example PCB layouts are shown in the Demonstration Board Layout section. Further detailed and specific information concerning PCB layout, fabrication, and mounting an WQFN package is available from Texas Instruments's package Engineering Group under application note AN1187.

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifer, whether the amplifier is bridged or single-ended. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \text{ Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation versus a single-ended amplifier operating at the same conditions.

$$P_{DMAX} = 4 * (V_{DD})^2 / (2\pi^2 R_L) \text{ Bridge Mode} \quad (3)$$

Since the LM4923 has bridged outputs, the maximum internal power dissipation is 4 times that of a single-ended amplifier. Even with this substantial increase in power dissipation, the LM4923 does not require additional heatsinking under most operating conditions and output loading. From Equation 3, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 625mW. The maximum power dissipation point obtained from Equation 3 must not be greater than the power dissipation results from Equation 4:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (4)$$

The LM4923's θ_{JA} in an NGP0008A package is 140°C/W. Depending on the ambient temperature, T_A, of the system surroundings, Equation 4 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 3 is greater than that of Equation 4, then either the supply voltage must be decreased, the load impedance increased, the ambient temperature reduced, or the θ_{JA} reduced with heatsinking. In many cases, larger traces near the output, V_{DD}, and GND pins can be used to lower the θ_{JA}. The larger areas of copper provide a form of heatsinking allowing higher power dissipation. For the typical application of a 5V power supply, with an 8Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 62°C provided that device operation is around the maximum power dissipation point. Recall that internal power dissipation is a function of output power. If typical operation is not around the maximum power dissipation point, the LM4923 can operate at higher ambient temperatures. Refer to the Typical Performance Characteristics curves for power dissipation information.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection ratio (PSRR). The capacitor location on both the bypass and power supply pins should be as close to the device as possible. A larger half-supply bypass capacitor improves PSRR because it increases half-supply stability. Typical applications employ a 5V regulator with 10µF and 0.1µF bypass capacitors that increase supply stability. This, however, does not eliminate the need for bypassing the supply nodes of the LM4923. The LM4923 will operate without the bypass capacitor C_B, although the PSRR may decrease. A 1µF capacitor is recommended for C_B. This value maximizes PSRR performance. Lesser values may be used, but PSRR decreases at frequencies below 1kHz. The issue of C_B selection is thus dependant upon desired PSRR and click and pop performance as explained in the section Proper Selection of External Components.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4923 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. The device may then be placed into shutdown mode by toggling the Shutdown Select pin to logic low. The trigger point for shutdown is shown as a typical value in the Supply Current vs Shutdown Voltage graphs in the Typical Performance Characteristics section. It is best to switch between ground and supply for maximum performance. While the device may be disabled with shutdown voltages in between ground and supply, the idle current may be greater than the typical value of 0.1µA. In either case, the shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry, which provides a quick, smooth transition to shutdown. Another solution is to use a single-throw switch in conjunction with an external pull-up resistor. This scheme ensures that the shutdown pin will not float, thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical when optimizing device and system performance. Although the LM4923 is tolerant to a variety of external component combinations, consideration of component values must be made when maximizing overall system quality.

The LM4923 is unity-gain stable, giving the designer maximum system flexibility. The LM4923 should be used in low closed-loop gain configurations to minimize THD+N values and maximize signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs. Please refer to the AUDIO POWER AMPLIFIER DESIGN section for a more complete explanation of proper gain selection. When used in its typical application as a fully differential power amplifier the LM4923 does not require input coupling capacitors for input sources with DC common-mode voltages of less than V_{DD}. Exact allowable input common-mode voltage levels are actually a function of V_{DD}, R_i, and R_f and may be determined by Equation 5:

$$V_{CMi} < (V_{DD}-1.2)*((R_f+(R_i)/(R_f)-V_{DD}*(R_i / 2R_f) \quad (5)$$

$$-R_F / R_I = A_{VD} \quad (6)$$

Special care must be taken to match the values of the feedback resistors (R_{F1} and R_{F2}) to each other as well as matching the input resistors (R_{i1} and R_{i2}) to each other (see Figure 1) more in front. Because of the balanced nature of differential amplifiers, resistor matching differences can result in net DC currents across the load. This DC current can increase power consumption, internal IC power dissipation, reduce PSRR, and possibly damaging the loudspeaker. The chart below demonstrates this problem by showing the effects of differing values between the feedback resistors while assuming that the input resistors are perfectly matched. The results below apply to the application circuit shown in Figure 1, and assumes that V_{DD} = 5V, R_L = 8Ω, and the system has DC coupled inputs tied to ground.

Tolerance	R_{F1}	R_{F2}	V_{02} - V_{01}	I_{LOAD}
20%	0.8R	1.2R	-0.500V	62.5mA
10%	0.9R	1.1R	-0.250V	31.25mA
5%	0.95R	1.05R	-0.125V	15.63mA
1%	0.99R	1.01R	-0.025V	3.125mA
0%	R	R	0	0

Similar results would occur if the input resistors were not carefully matched. Adding input coupling capacitors in between the signal source and the input resistors will eliminate this problem, however, to achieve best performance with minimum component count it is highly recommended that both the feedback and input resistors matched to 1% tolerance or better.

AUDIO POWER AMPLIFIER DESIGN

Design a 1W/8Ω Audio Amplifier

Given:	
Power Output	1Wrms
Load Impedance	8Ω
Input Level	1Vrms
Input Impedance	20kΩ
Bandwidth	100Hz–20kHz ± 0.25dB

A designer must first determine the minimum supply rail to obtain the specified output power. The supply rail can easily be found by extrapolating from the Output Power vs Supply Voltage graphs in the Typical Performance Characteristics section. A second way to determine the minimum supply rail is to calculate the required V_{OPEAK} using Equation 7 and add the dropout voltages. Using this method, the minimum supply voltage is (Vopeak + ($V_{DO\ TOP}$ + ($V_{DO\ BOT}$)), where $V_{DO\ BOT}$ and $V_{DO\ TOP}$ are extrapolated from the Dropout Voltage vs Supply Voltage curve in the Typical Performance Characteristics section.

$$V_{opeak} = \sqrt{(2R_L P_O)} \tag{7}$$

Using the Output Power vs Supply Voltage graph for an 8Ω load, the minimum supply rail just about 5V. Extra supply voltage creates headroom that allows the LM4923 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the Power Dissipation section. Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 8.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \tag{8}$$

$$R_f / R_i = A_{VD} \tag{9}$$

From Equation 8, the minimum A_{VD} is 2.83. Since the desired input impedance was 20kΩ, a ratio of 2.83:1 of R_f to R_i results in an allocation of R_i = 20kΩ for both input resistors and R_f = 60kΩ for both feedback resistors. The final design step is to address the bandwidth requirement which must be stated as a single -3dB frequency point. Five times away from a -3dB point is 0.17dB down from passband response which is better than the required ±0.25dB specified.

$$f_H = 20kHz * 5 = 100kHz \tag{10}$$

The high frequency pole is determined by the product of the desired frequency pole, f_H , and the differential gain, A_{VD} . With a A_{VD} = 2.83 and f_H = 100kHz, the resulting GBWP = 150kHz which is much smaller than the LM4923 GBWP of 10MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LM4923 can still be used without running into bandwidth limitations.

Revision History

Rev	Date	Description
1.0	09/28/07	Added the VSSOP package, then released.
1.01	12/17/07	Updated the mktg outline NGP0008A into the rev B.
1.02	02/19/09	Fixed typo labels on the typical circuit diagram.
E	05/03/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4923LQ/NOPB	Active	Production	WQFN (NGP) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	GB2
LM4923LQ/NOPB.A	Active	Production	WQFN (NGP) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	GB2
LM4923LQX/NOPB	Active	Production	WQFN (NGP) | 8	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	GB2
LM4923LQX/NOPB.A	Active	Production	WQFN (NGP) | 8	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	GB2
LM4923MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	GC8
LM4923MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	GC8

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

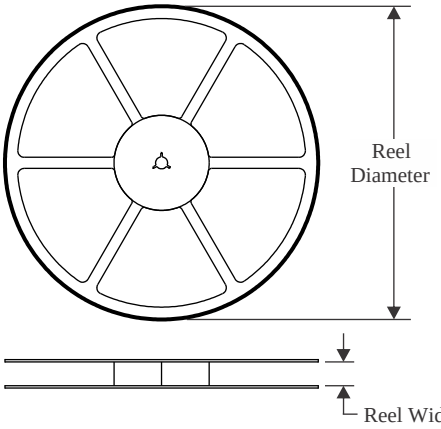
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

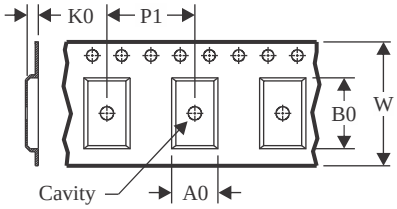
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

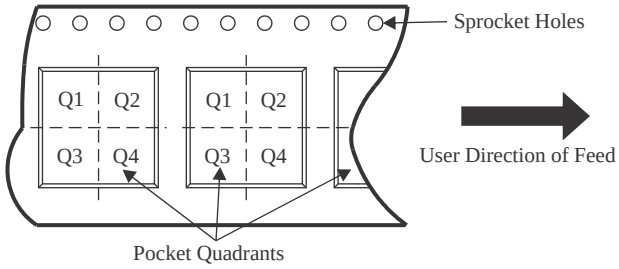


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

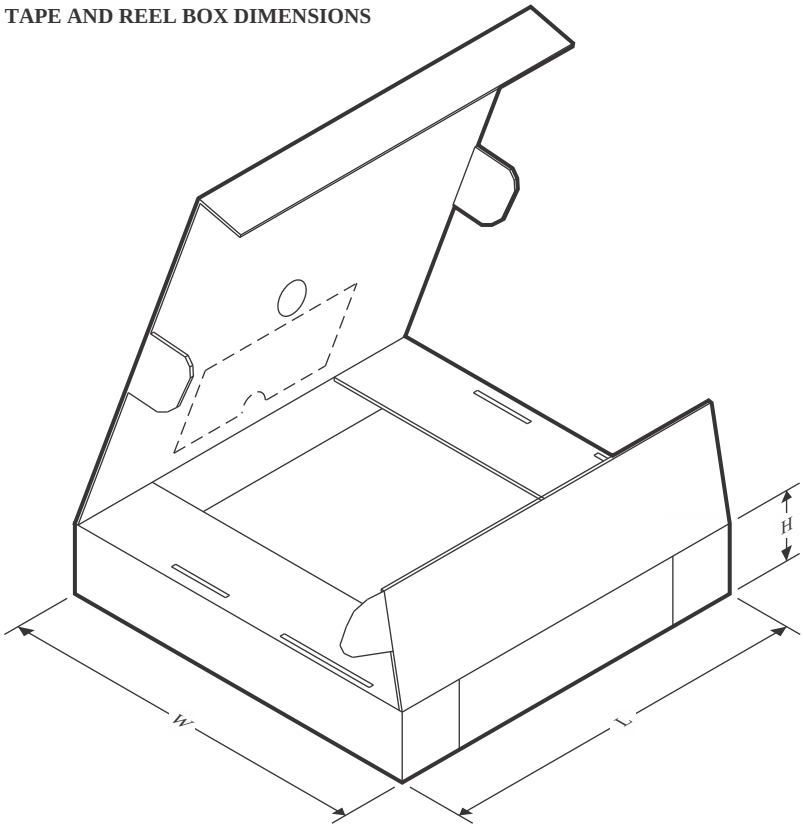
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4923LQ/NOPB	WQFN	NGP	8	1000	177.8	12.4	2.2	2.2	1.0	8.0	12.0	Q1
LM4923LQX/NOPB	WQFN	NGP	8	4500	330.0	12.4	2.2	2.2	1.0	8.0	12.0	Q1
LM4923MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1

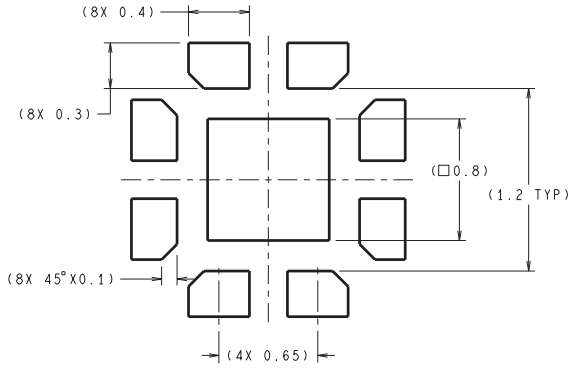
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

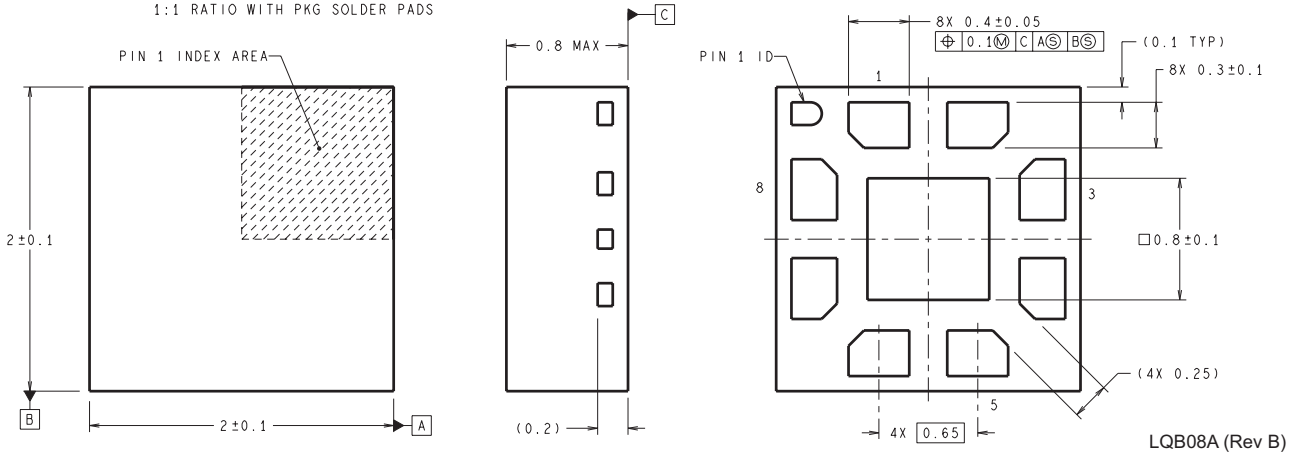
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4923LQ/NOPB	WQFN	NGP	8	1000	208.0	191.0	35.0
LM4923LQX/NOPB	WQFN	NGP	8	4500	356.0	356.0	36.0
LM4923MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0

NGP0008A



RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS



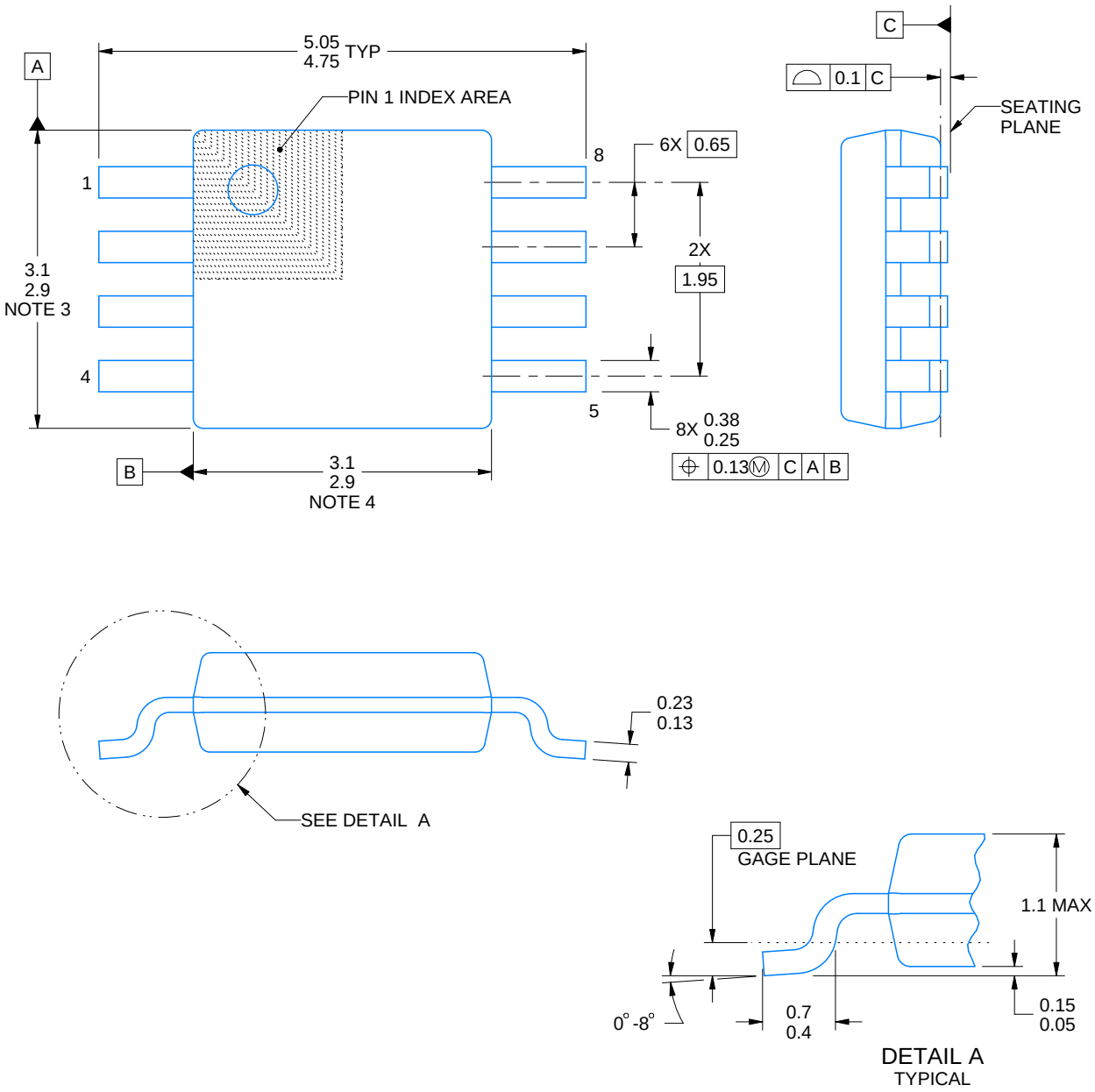
LQB08A (Rev B)

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

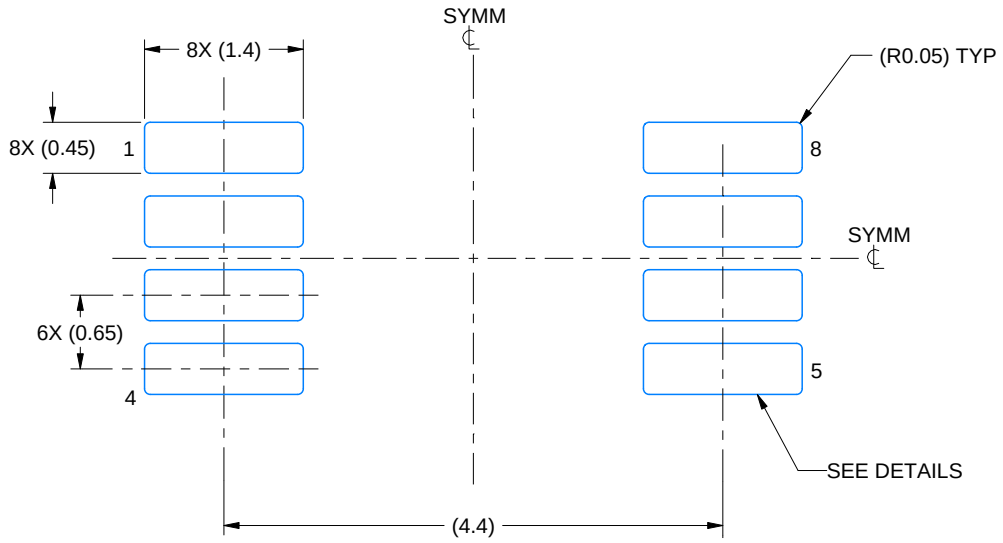
SMALL OUTLINE PACKAGE



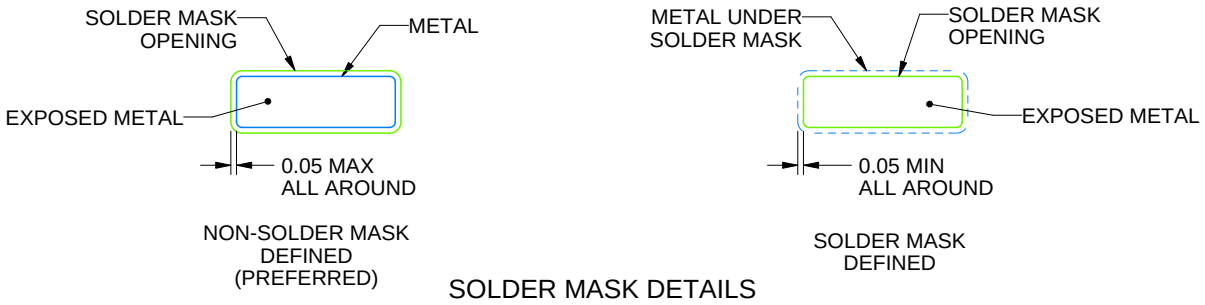
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

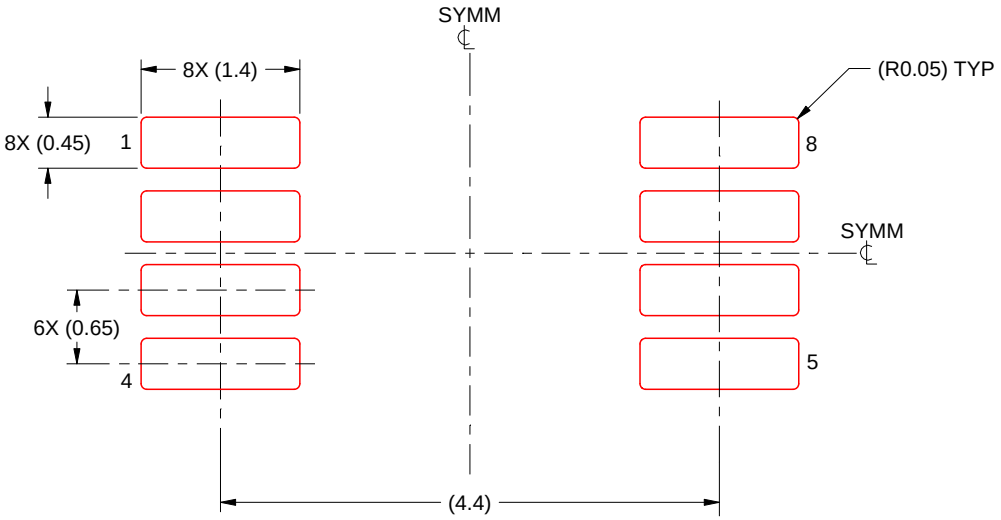


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265