Ordering number : EN*6183

Monolithic Digital IC

LB11847

PWM Current Control Type Stepping Motor Driver

Preliminary

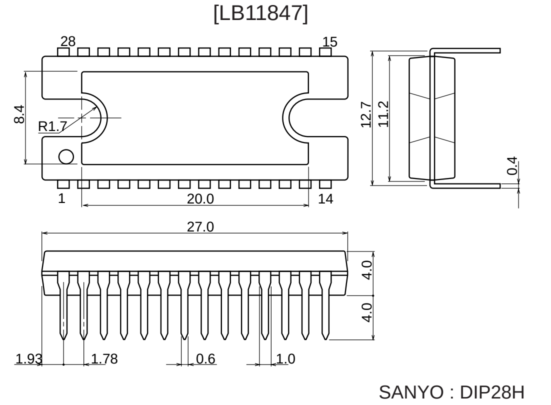
Overview

The LB11847 is a driver IC for stepping motors with PWM current control bipolar drive (fixed OFF time). A special feature of this IC is that V_{REF} voltage is constant while the current can be set in 15 steps, allowing drive of motors ranging from 1-2 phase exciter types to 4W 1-2 phase exciter types. The current decay pattern can also be selected (SLOW DECAY, FAST DECAY, MIX DECAY) to increase the decay of regenerative current at chopping OFF, thereby improving response characteristics. This is especially useful for carriage and paper feed stepping motors in printers and similar applications where high-precision control and low vibrations are required.

Package Dimensions

unit: mm

3147B-DIP28H



Features

- PWM current control (fixed OFF time)
- Load current digital selector (1-2, W1-2, 2W1-2, 4W1-2 phase exciter drive possible)
- Selectable current decay pattern (SLOW DECAY, FAST DECAY, MIX DECAY)
- Simultaneous ON prevention function (feedthrough current prevention)
- Noise canceler
- Built-in thermal shutdown circuit
- Built-in logic low-voltage OFF circuit

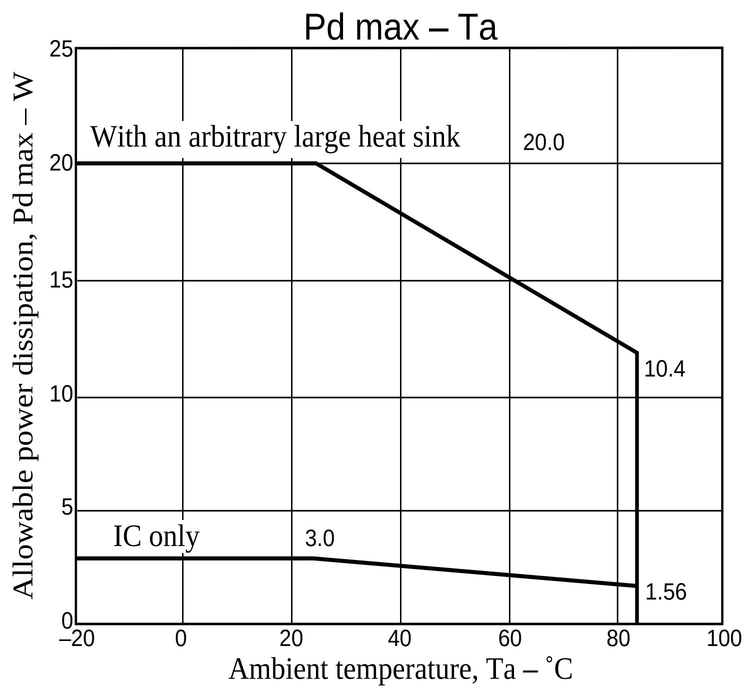
Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	V_{BB}		50	V
Output peak current	I_{OPEAK}	$t_W \leq 20\ \mu s$	1.75	A
Output continuous current	I_O max		1.5	A
Logic supply voltage	V_{CC}		7.0	V
Logic input voltage range	V_{IN}		–0.3 to V_{CC}	V
Emitter output voltage	V_E		1.0	V
Allowable power dissipation	Pd max	Ta = 25°C	3.0	W
		With heat sink	20	W
Operating temperature	Topr		–20 to +85	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage range	V_{BB}		10 to 45	V
Logic supply voltage range	V_{CC}		4.75 to 5.25	V
Reference voltage range	V_{REF}		0.0 to 3.0	V



Electrical Characteristics at Ta = 25°C, V_{BB} = 45V, V_{CC} = 5V, V_{REF} = 1.52V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Output Block]						
Output stage supply voltage	$I_{BB\ ON}$		2.3	3.5	5.0	mA
	$I_{BB\ OFF}$		0.5	0.8	1.1	mA
Output saturation voltage	V_O(sat)1	I_O = +1.0A, sink		1.2	1.6	V
	V_O(sat)2	I_O = +1.5A, sink		1.5	1.9	V
	V_O(sat)3	I_O = –1.0A, source		1.9	2.2	V
	V_O(sat)4	I_O = –1.5A, source		2.2	2.4	V
Output leak current	I_O(leak)1	$V_O = V_{BB}$, sink			50	µA
	I_O(leak)2	V_O = 0V, source	–50			µA
Output sustain voltage	V_{SUS}	L = 15 mH, I_O = 1.5A, Guaranteed design value	45			V
[Logic Block]						
Logic supply voltage	$I_{CC\ ON}$	I_4 = 2.0V, I_3 = 2.0V, I_2 = 2.0V, I_1 = 2.0V	19.5	26	36.5	mA
	$I_{CC\ OFF}$	ENABLE = 2.0V	10.5	15	19.5	mA
Input voltage	V_{IH}		2.0			V
	V_{IL}				0.8	V
Input current	I_{IH}	V_{IH} = 2.0V			100	µA
	I_{IL}	V_{IL} = 0.8V	–10			µA
Sensing voltage	V_E	I_4 = 2.0V, I_3 = 2.0V, I_2 = 2.0V, I_1 = 2.0V	0.470	0.50	0.525	V
		I_4 = 2.0V, I_3 = 2.0V, I_2 = 2.0V, I_1 = 0.8V	0.445	0.48	0.505	V
		I_4 = 2.0V, I_3 = 2.0V, I_2 = 0.8V, I_1 = 2.0V	0.425	0.46	0.485	V
		I_4 = 2.0V, I_3 = 2.0V, I_2 = 0.8V, I_1 = 0.8V	0.410	0.43	0.465	V
		I_4 = 2.0V, I_3 = 0.8V, I_2 = 2.0V, I_1 = 2.0V	0.385	0.41	0.435	V
		I_4 = 2.0V, I_3 = 0.8V, I_2 = 2.0V, I_1 = 0.8V	0.365	0.39	0.415	V
		I_4 = 2.0V, I_3 = 0.8V, I_2 = 0.8V, I_1 = 2.0V	0.345	0.37	0.385	V
		I_4 = 2.0V, I_3 = 0.8V, I_2 = 0.8V, I_1 = 0.8V	0.325	0.35	0.365	V
		I_4 = 0.8V, I_3 = 2.0V, I_2 = 2.0V, I_1 = 2.0V	0.280	0.30	0.325	V
		I_4 = 0.8V, I_3 = 2.0V, I_2 = 2.0V, I_1 = 0.8V	0.240	0.26	0.285	V
		I_4 = 0.8V, I_3 = 2.0V, I_2 = 0.8V, I_1 = 2.0V	0.195	0.22	0.235	V
		I_4 = 0.8V, I_3 = 2.0V, I_2 = 0.8V, I_1 = 0.8V	0.155	0.17	0.190	V
		I_4 = 0.8V, I_3 = 0.8V, I_2 = 2.0V, I_1 = 2.0V	0.115	0.13	0.145	V
		I_4 = 0.8V, I_3 = 0.8V, I_2 = 2.0V, I_1 = 0.8V	0.075	0.09	0.100	V
Reference current	I_{REF}	V_{REF} = 1.5V	–0.5			µA
CR pin current	I_{CR}	CR = 1.0V	–4.6		–1.0	mA
MD pin current	I_{MD}	MD = 1.0V, CR = 4.0V	–5.0			µA
DECAY pin current Low	I_{DECL}	V_{DEC} = 0.8V	–10			µA
DECAY pin current High	I_{DECH}	V_{DEC} = 2.0V			5	µA
Thermal shutdown temperature	TSD			170		°C
Logic ON voltage	$L_{VSD}1$		3.35	3.65	3.95	V
Logic OFF voltage	$L_{VSD}2$		3.20	3.50	3.80	V
L_{VSD} hysteresis width	ΔL_{VSD}		0.065	0.15	0.23	V

Truth Table

PHASE	ENABLE	OUT_A	$OUT_{\bar{A}}$
H	L	H	L
L	L	L	H
—	H	OFF	OFF

Set Current Truth Table

I_A4	I_A3	I_A2	I_A1	Set current I_{OUT}	Current ratio (%)
1	1	1	1	$11.5/11.5 \times V_{REF}/3.04RE = I_{OUT}$	100
1	1	1	0	$11.0/11.5 \times V_{REF}/3.04RE = I_{OUT}$	95.65
1	1	0	1	$10.5/11.5 \times V_{REF}/3.04RE = I_{OUT}$	91.30
1	1	0	0	$10.0/11.5 \times V_{REF}/3.04RE = I_{OUT}$	86.95
1	0	1	1	$9.5/11.5 \times V_{REF}/3.04RE = I_{OUT}$	82.61
1	0	1	0	$9.0/11.5 \times V_{REF}/3.04RE = I_{OUT}$	78.26
1	0	0	1	$8.5/11.5 \times V_{REF}/3.04RE = I_{OUT}$	73.91
1	0	0	0	$8.0/11.5 \times V_{REF}/3.04RE = I_{OUT}$	69.56
0	1	1	1	$7.0/11.5 \times V_{REF}/3.04RE = I_{OUT}$	60.87
0	1	1	0	$6.0/11.5 \times V_{REF}/3.04RE = I_{OUT}$	52.17
0	1	0	1	$5.0/11.5 \times V_{REF}/3.04RE = I_{OUT}$	43.48
0	1	0	0	$4.0/11.5 \times V_{REF}/3.04RE = I_{OUT}$	34.78
0	0	1	1	$3.0/11.5 \times V_{REF}/3.04RE = I_{OUT}$	26.08
0	0	1	0	$2.0/11.5 \times V_{REF}/3.04RE = I_{OUT}$	17.39

* Current ratio (%) is the calculated set current value.

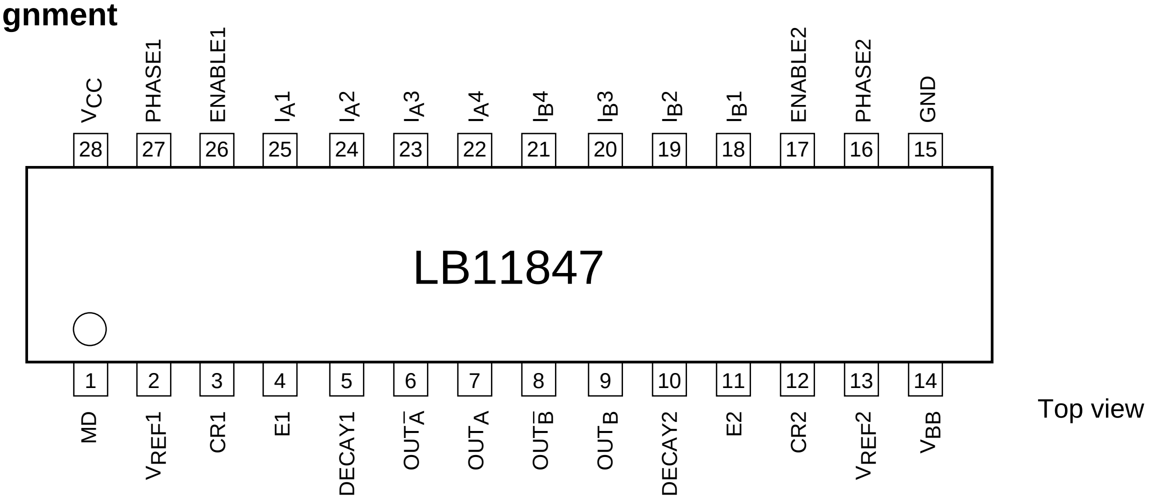
Current Decay Switching Truth Table

Current decay mode	DECAY pin	MD pin	Output chopping
SLOW DECAY	H	L	Upper-side chopping
FAST DECAY	L	L	Dual-side chopping
MIX DECAY	L	4V to 1.5V input voltage setting	CR voltage > MD : dual-side chopping CR voltage < MD : upper-side chopping

Pin Function

Pin number	Pin name	Function description
1	MD	Sets the OFF time for FAST mode and SLOW mode in MIX DECAY Setting input range: 4V to 1.5V
2 13	$V_{REF}1$ $V_{REF}2$	Output set current reference supply pins Setting voltage range: 0V to 3V
3 12	CR1 CR2	Output OFF time setting pins for switching operation
4 11	E1 E2	Pins for controlling the set current with sensing resistor RE
5 10	DECAY1 DECAY2	SLOW mode/FAST mode selector pins SLOW DECAY: H FAST DECAY: L
6 7 8 9	$OUT_{\bar{A}}$ OUT_{A} $OUT_{\bar{B}}$ OUT_{B}	Output pins
14	V_{BB}	Output stage supply voltage pin
15	GND	Ground pin
27 16	PHASE1 PHASE2	Output phase selector input pins
26 17	ENABLE1 ENABLE2	Output ON/OFF setting input pins
22, 23 24, 25 21, 20 19, 18	I_A4, I_A3 I_A2, I_A1 I_B4, I_B3 I_B2, I_B1	Output set current digital input pins 15-stage voltage setting
28	V_{CC}	Logic block supply voltage pin

Pin Assignment



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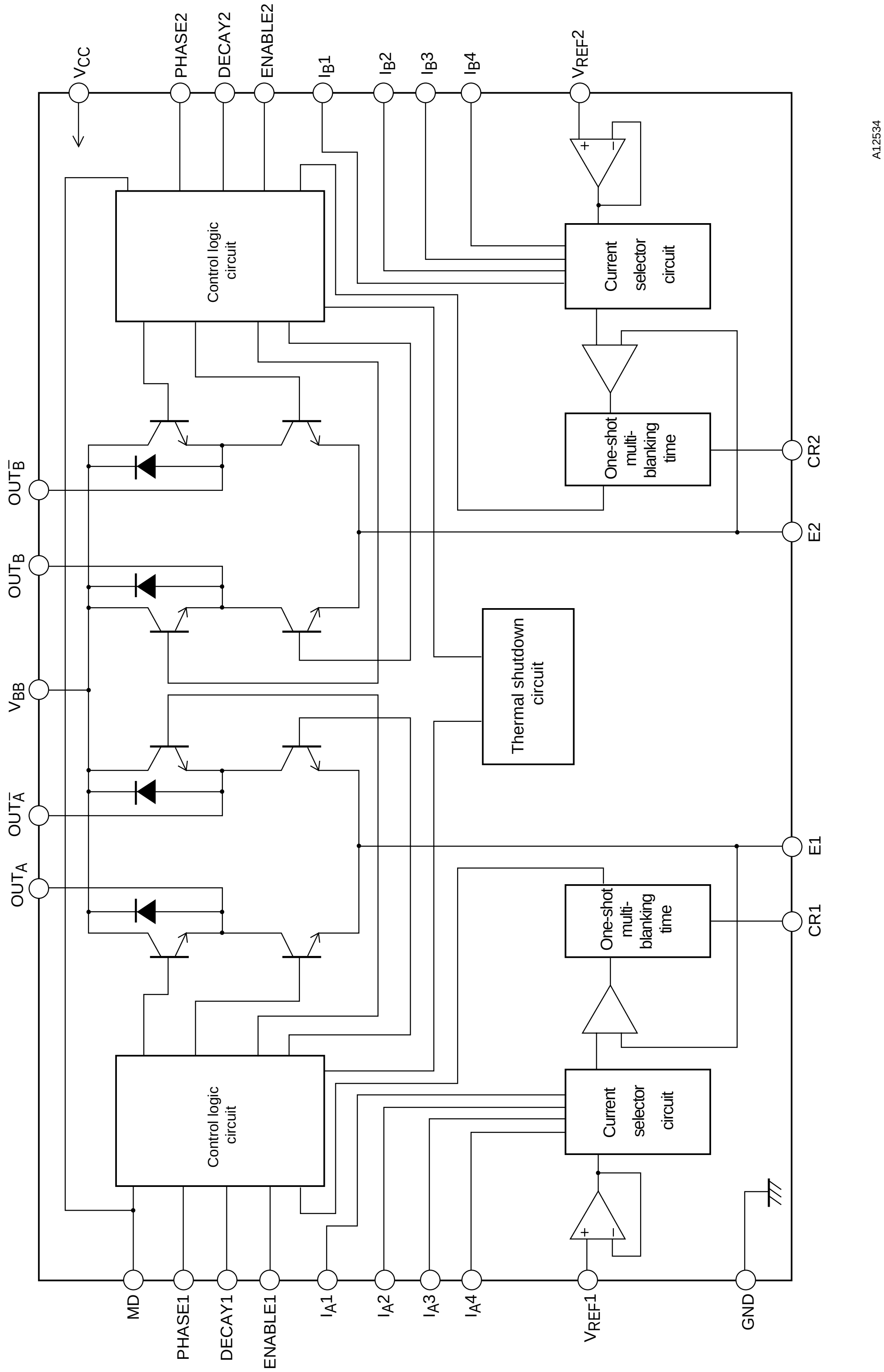
Block Diagram

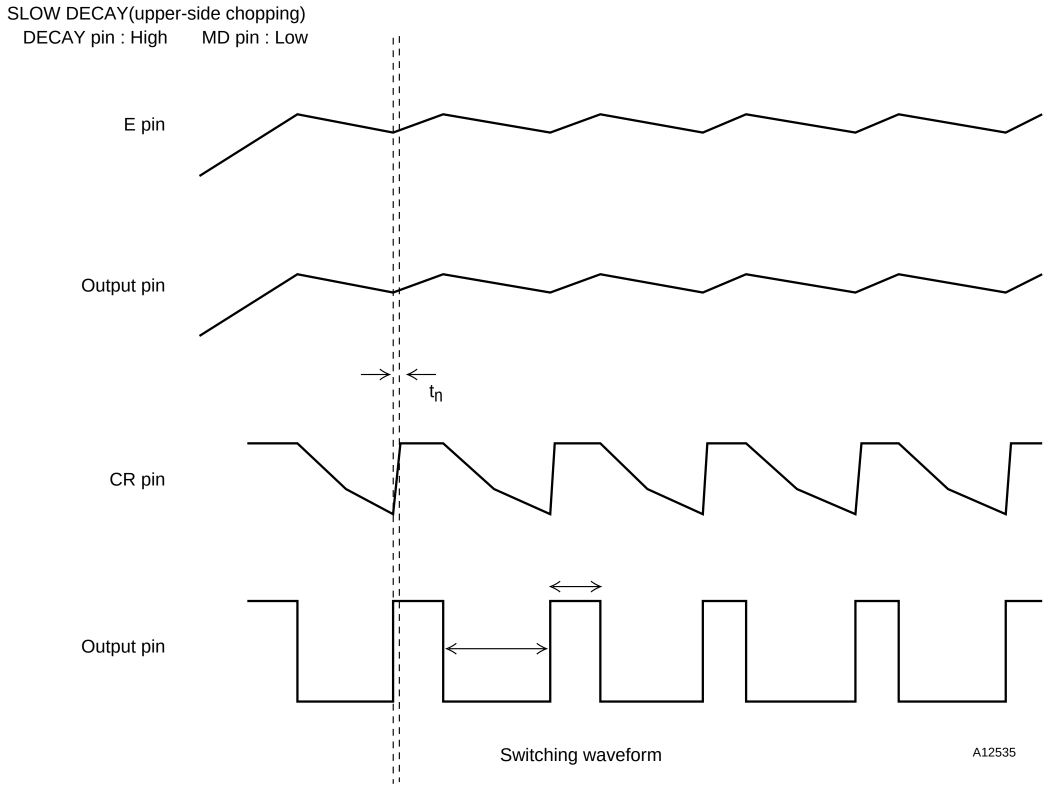


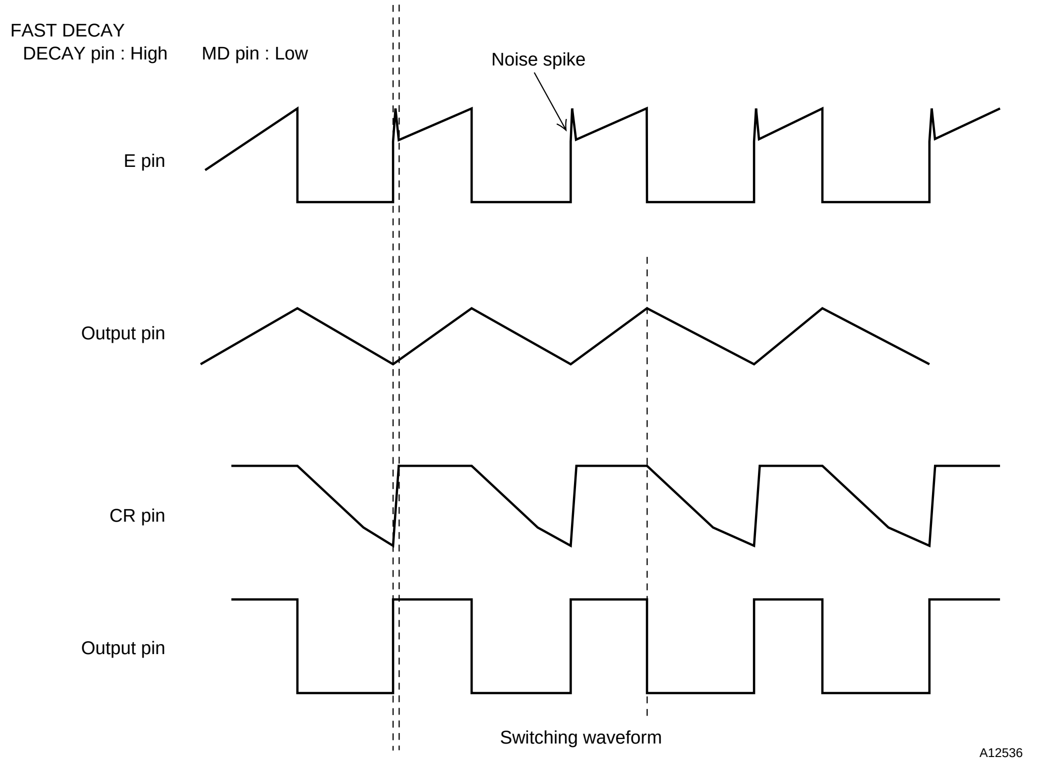
Sequence Table

	Phase A							Phase B							Phase 1-2	Phase W1-2	Phase 2W1-2	Phase 4W1-2
No.	I_A4	I_A3	I_A2	I_A1	ENA1	PHA1	I_{OUT}	I_B4	I_B3	I_B2	I_B1	ENA2	PHA2	I_{OUT}				
0	1	1	1	1	0	0	100%	0	0	1	0	1	*	0%	√	√	√	√
1	1	1	1	1	0	0	100	0	0	1	0	0	0	17.39				√
2	1	1	1	1	0	0	100	0	0	1	1	0	0	26.08			√	√
3	1	1	1	0	0	0	96.65	0	1	0	0	0	0	34.78				√
4	1	1	0	1	0	0	91.30	0	1	0	1	0	0	43.48		√	√	√
5	1	1	0	0	0	0	86.95	0	1	1	0	0	0	52.17				√
6	1	0	1	1	0	0	82.61	0	1	1	1	0	0	60.87			√	√
7	1	0	1	0	0	0	78.26	1	0	0	0	0	0	69.56				√
8	1	0	0	1	0	0	73.91	1	0	0	1	0	0	73.91	√	√	√	√
9	1	0	0	0	0	0	69.56	1	0	1	0	0	0	78.26				√
10	0	1	1	1	0	0	60.87	1	0	1	1	0	0	82.61			√	√
11	0	1	1	0	0	0	52.17	1	1	0	0	0	0	86.95				√
12	0	1	0	1	0	0	43.48	1	1	0	1	0	0	91.30		√	√	√
13	0	1	0	0	0	0	34.78	1	1	1	0	0	0	96.65				√
14	0	0	1	1	0	0	26.08	1	1	1	1	0	0	100			√	√
15	0	0	1	0	0	0	17.39	1	1	1	1	0	0	100				√
16	0	0	0	1	1	*	0	1	1	1	1	0	0	100	√	√	√	√
17	0	0	1	0	0	1	17.39	1	1	1	1	0	0	100				√
18	0	0	1	1	0	1	26.08	1	1	1	1	0	0	100			√	√
19	0	1	0	0	0	1	34.78	1	1	1	0	0	0	95.65				√
20	0	1	0	1	0	1	43.48	1	1	0	1	0	0	91.30		√	√	√
21	0	1	1	0	0	1	52.17	1	1	0	0	0	0	86.95				√
22	0	1	1	1	0	1	60.87	1	0	1	1	0	0	82.61			√	√
23	1	0	0	0	0	1	69.56	1	0	1	0	0	0	78.26				√
24	1	0	0	1	0	1	73.91	1	0	0	1	0	0	73.91	√	√	√	√
25	1	0	1	0	0	1	78.26	1	0	0	0	0	0	69.56				√
26	1	0	1	1	0	1	82.61	0	1	1	1	0	0	60.87			√	√
27	1	1	0	0	0	1	86.95	0	1	1	0	0	0	52.17				√
28	1	1	0	1	0	1	91.30	0	1	0	1	0	0	43.48		√	√	√
29	1	1	1	0	0	1	95.65	0	1	0	0	0	0	34.78				√
30	1	1	1	1	0	1	100	0	0	1	1	0	0	26.08			√	√
31	1	1	1	1	0	1	100	0	0	1	0	0	0	17.39				√

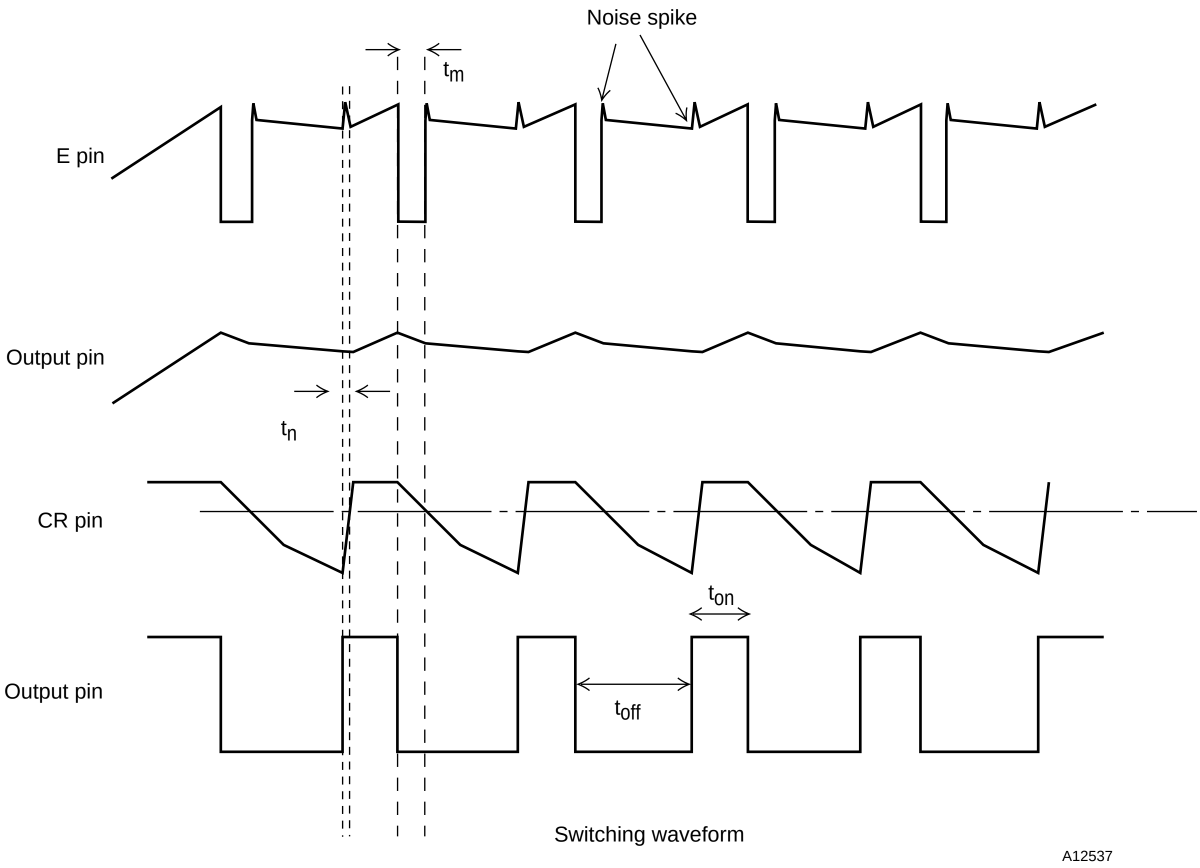
* : Iout percentage (%) is the calculated setting value.

Switch Timing Chart during PWM Drive





MIX DECAY

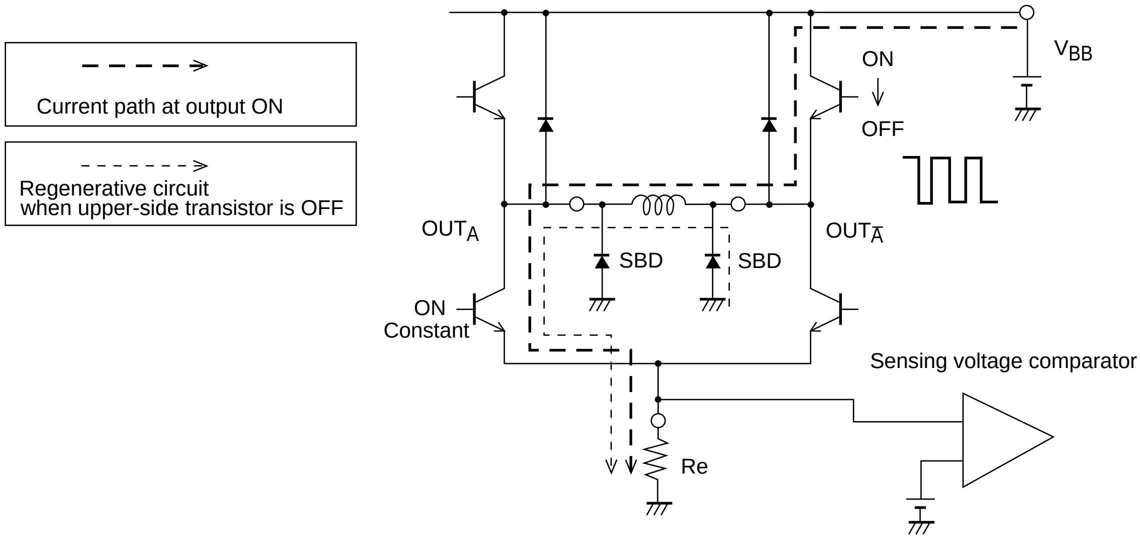


t_{on} : Output ON time
t_{off} : Output OFF time
t_m : FAST DECAY time in MIX DECAY mode
t_n : Noise cancelling time

MIX DECAY logic setting

DECAY pin : L
MD pin : 1.5V to 4.0V voltage setting
CR voltage and MD pin voltage are compared to select dual-side chopping or upper-side chopping.
CR voltage > MD pin voltage: dual-side chopping
CR voltage < MD pin voltage: top-side choppinng

SLOW DECAY current path
Regenerative current during upper-side transistor switching operation



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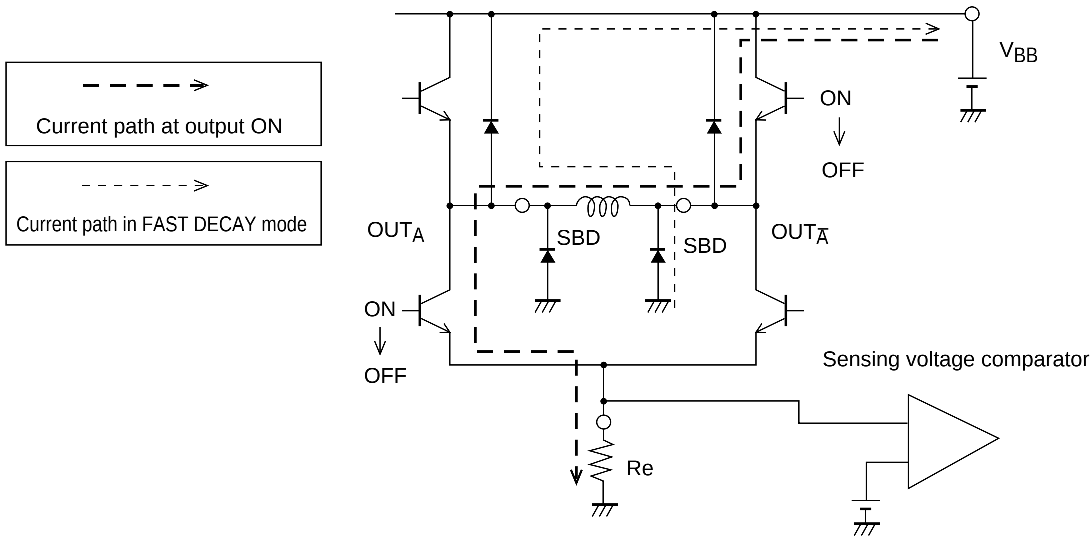
Current path in FAST DECAY mode



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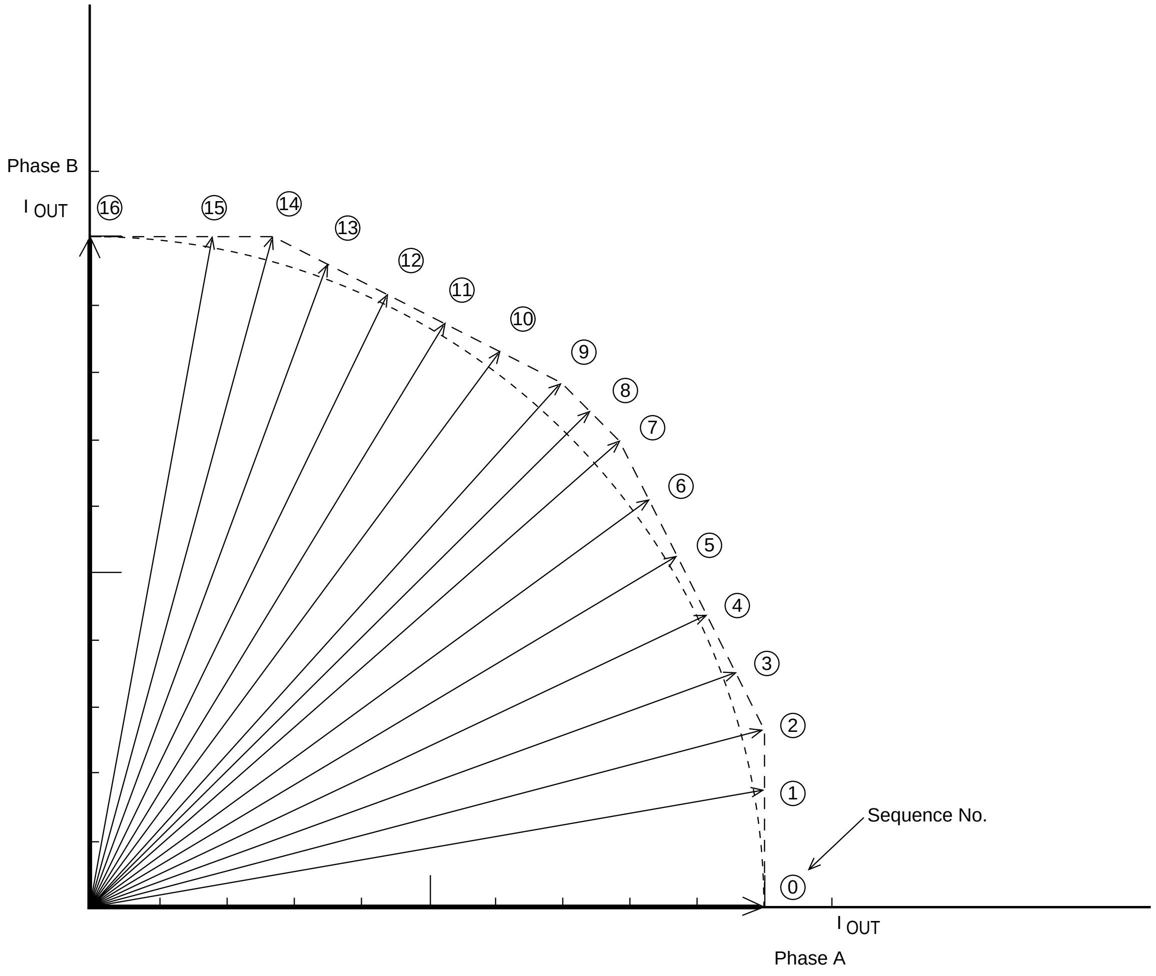
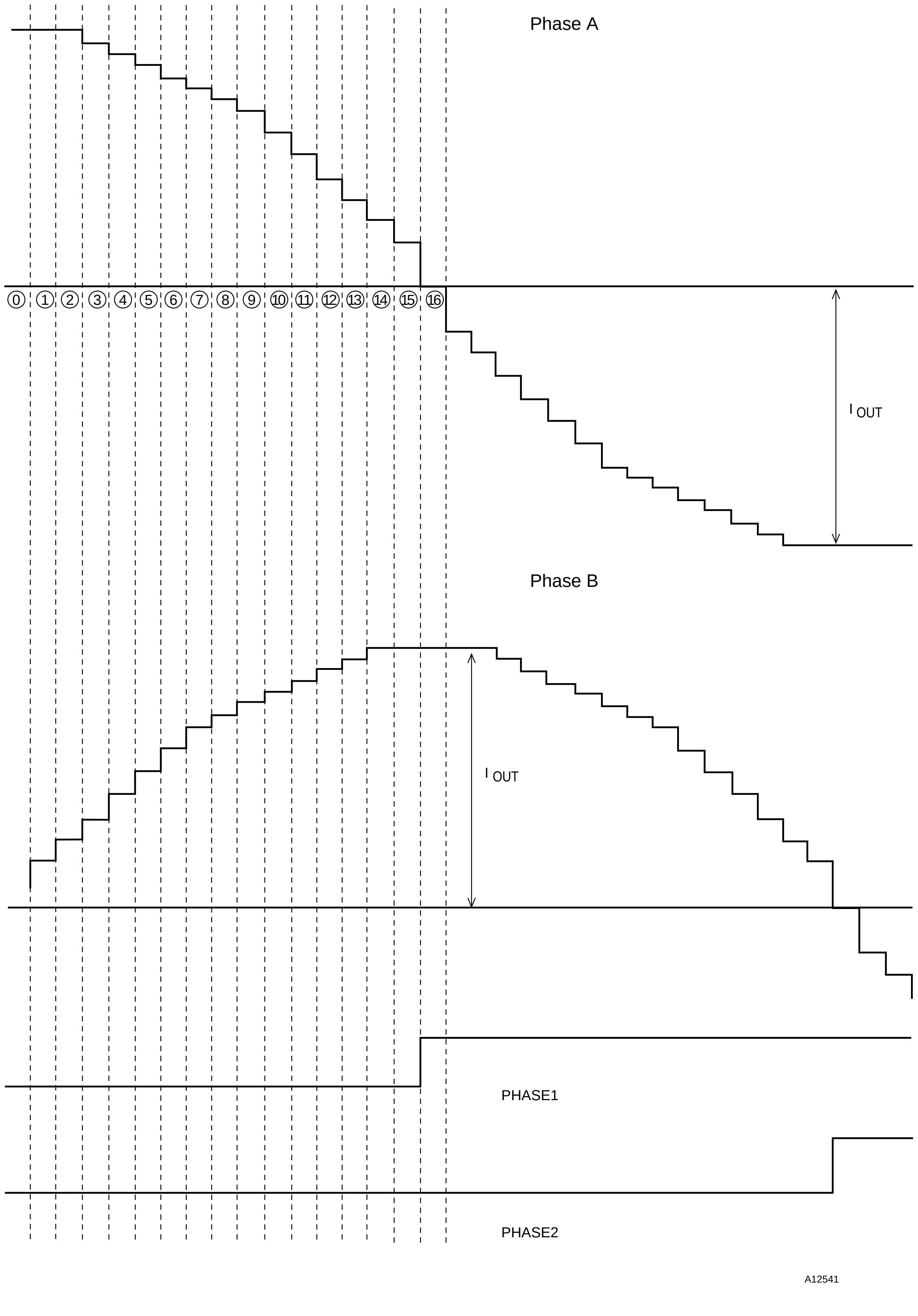
Composite Vectors of Set Current (1 step normalized to 90°)



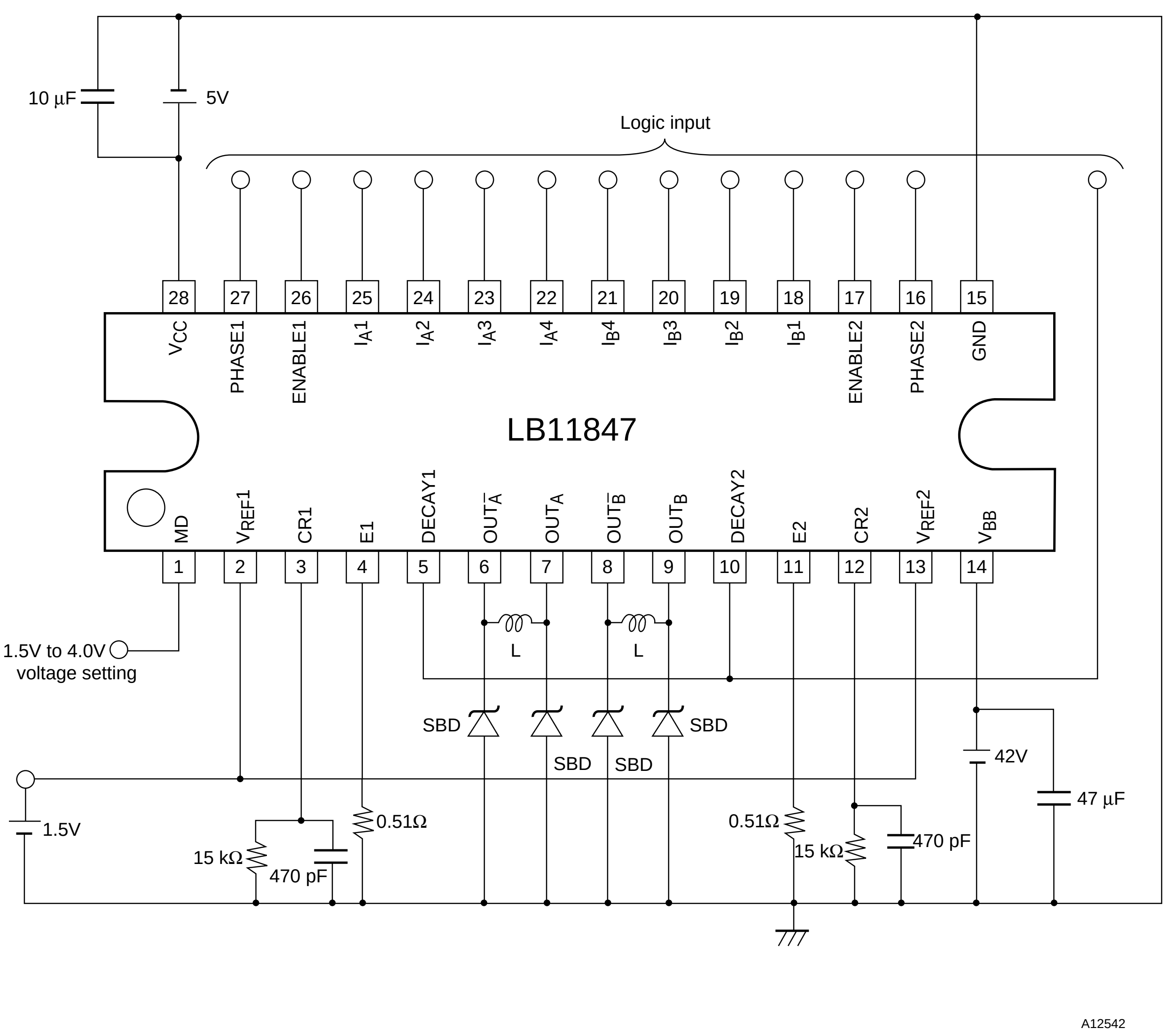
No.	θ	Rotation angles	Composite vectors
0	θ0	0°	100.0
1	θ1	9.87°	101.5
2	θ2	14.6°	103.35
3	θ3	20.0°	101.78
4	θ4	25.5°	101.12
5	θ5	30.96°	101.4
6	θ6	36.38°	102.61
7	θ7	41.63°	104.7
8	θ8	45.0°	104.5
9	θ9	48.37°	104.7
10	θ10	53.62°	102.61
11	θ11	59.04°	101.4
12	θ12	64.5°	101.12
13	θ13	70.0°	101.78
14	θ14	75.4°	103.35
15	θ15	80.13°	101.5
16	θ16	90.0°	100.0

* Rotation angle and composite spectrum are calculated values.

Set Current Waveform Model



Sample Application Circuit



Notes on Usage

1. External diodes

Because this IC uses upper-side transistor switching in SLOW DECAY mode and dual-side transistor switching in FAST DECAY mode, it requires external diodes between the OUT pins and ground for the regenerative current during switching OFF. Use Schottky barrier diodes with low VF.

2. V_{REF} pin

Because the V_{REF} pin serves for input of the set current reference voltage, precautions against noise must be taken. The input voltage range is 0 to 3.0V.

3. GND pin

The ground circuit for this IC must be designed so as to allow for high-current switching. Blocks where high current flows must use low-impedance patterns and must be removed from small-signal lines. Especially the ground connection for the sensing resistor RE at pin E, and the ground connection for the Schottky barrier diodes should be in close proximity to the IC ground.

The capacitors between V_{CC} and ground, and V_{BB} and ground should be placed close to the V_{CC} and V_{BB} pins, respectively.

4. Simultaneous ON prevention function

This IC incorporates a circuit to prevent feedthrough current when phase switching. For reference, the output ON and OFF delay times at PHASE and ENABLE switching are given below.

Reference data * typical value

		Sink side	Source side
PHASE switching (Low -> High)	ON delay time	1.9 µs	2.2 µs
	OFF delay time	0.8 µs	1.8 µs
PHASE switching (High -> Low)	ON delay time	1.4 µs	1.7 µs
	OFF delay time	0.9 µs	1.35 µs
ENABLE switching	ON delay time	2.15 µs	2.75 µs
	OFF delay time	1.2 µs	5.8 µs

5. Noise canceler

This IC has a noise canceling function to prevent malfunction due to noise spikes generated when switching ON. The noise cancel time t_n is determined by internal resistance of the CR pin and the constant of the externally connected CR components. The constant also determines the switching OFF time.

Figure 1 shows the internal configuration at the CR pin, and Figure 2 shows the CR pin constant setting range.

Equation when logic voltage $V_{CC} = 5$ V

CR pin voltage $E1 = V_{CC} \cdot R/(R1+R2+R)$ [V]

Noise cancel time $t_n \fallingdotseq (R1+R2) \cdot C \cdot 1n\{(E1-1.5)/(E1-4.0)\}$ [s]

Switching OFF time $t_{off} \fallingdotseq -R \cdot C \cdot 1n(1.5/E1)$ [s]

Internal resistance at CR pin : R1 = 1 kΩ, R2 = 300Ω (typ.)

*The CR constant setting range in Figure 2 on page 15 is given for reference. It applies to a switching OFF time in the range from 8 to 100 µs. The switching time can also be made higher than 100 µs. However, a capacitor value of more than several thousand pF will result in longer noise canceling time, which can cause the output current to become higher than the set current. The longer switching OFF time results in higher output current ripple, causing a drop in average current and rotation efficiency. When keeping the switching OFF time within 100 µs, it is recommended to stay within the CR constant range shown in Figure 2.

Internal configuration at CR pin

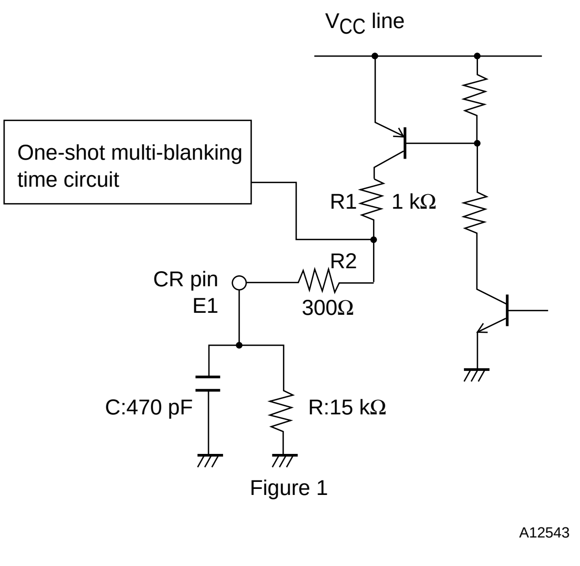


Figure 1

Switching OFF Time and CR Setting Range
(t_{off} time : approx. 8 to 100 µs)

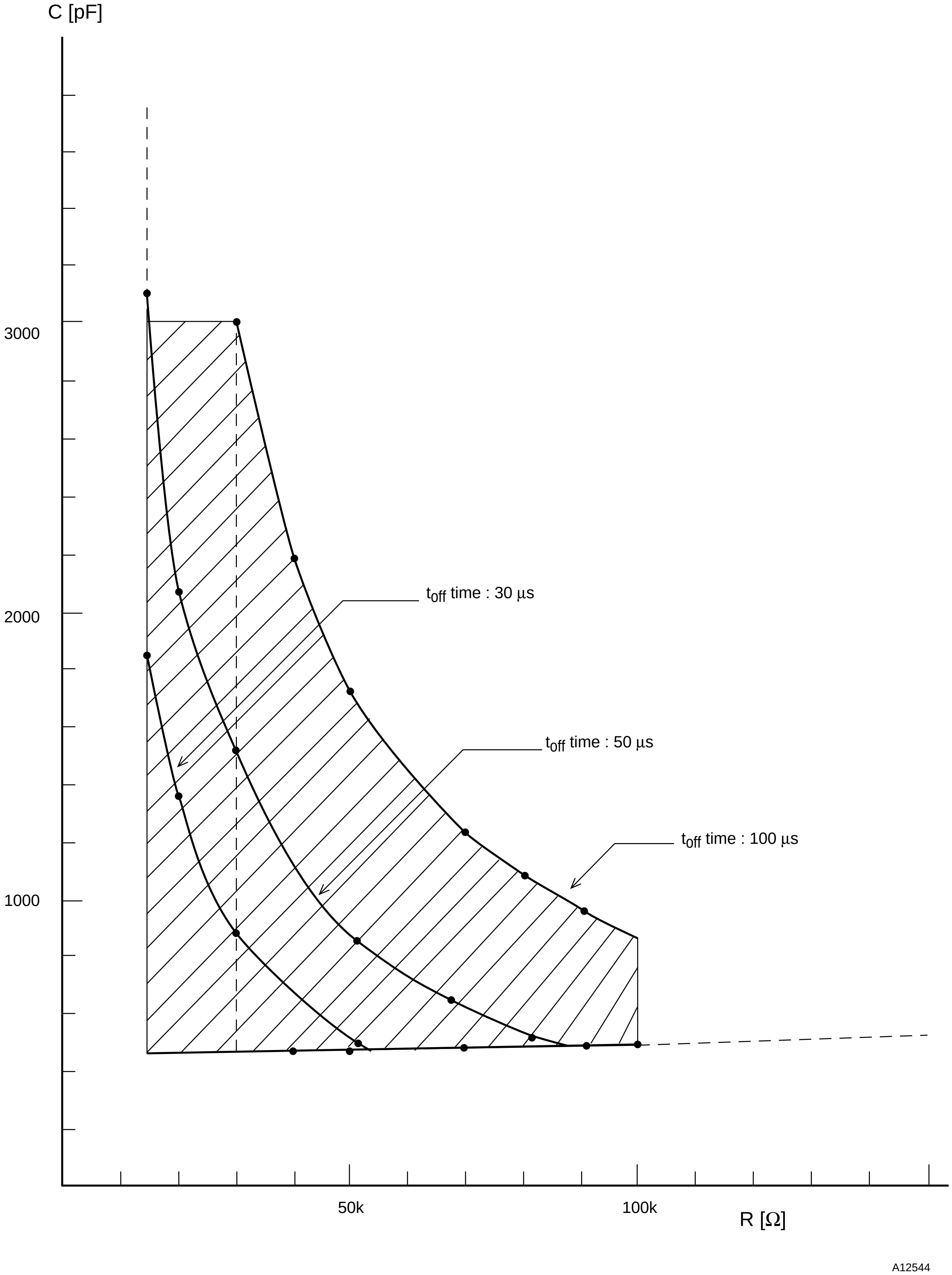


Figure 2

This catalog provides information as of June, 1999. Specifications and information herein are subject to change without notice.