FAIRCHILD SEMICONDUCTOR®

February 2008

FDMC4435BZ

P-Channel Power Trench® MOSFET

-30V, -18A, 20.0mΩ

Features

- Max $r_{DS(on)}$ = 20.0mΩ at V_{GS} = -10V, I_D = -8.5A
- Max $r_{DS(on)}$ = 37.0mΩ at V_{GS} = -4.5V, I_D = -6.3A
- Extended V_{GSS} range (-25V) for battery applications
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability
- HBM ESD protection level >7kV typical (Note 4)
- 100% UIL Tested
- Termination is Lead-free and RoHS Compliant

General Description

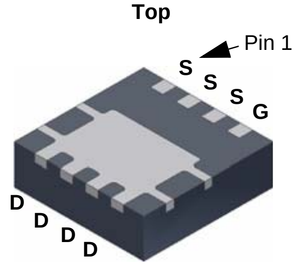
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance. This devie is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Applications

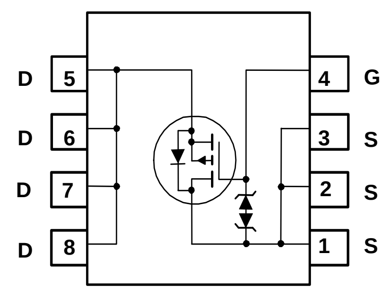
- High side in DC - DC Buck Converters
- Notebook battery power management
- Load switch in Notebook

Bottom

Top



Power 33



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-30	V
V_{GS}	Gate to Source Voltage	±25	V
I_D	Drain Current -Continuous (Package limited) T_C = 25°C	-18	A
	-Continuous (Silicon limited) T_C = 25°C	-31	
	-Continuous T_A = 25°C (Note 1a)	-8.5	
	-Pulsed	-50	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	24	mJ
P_D	Power Dissipation T_C = 25°C	31	W
	Power Dissipation T_A = 25°C (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

Package Marking and Ordering Information

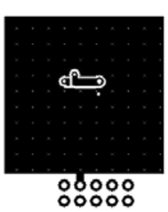
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC4435BZ	FDMC4435BZ	Power 33	13''	12mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250μA, V_{GS} = 0V	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250μA, referenced to 25°C		22		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24V, V_{GS} = 0V,			-1	μA
		V_{DS} = -24V, V_{GS} = 0V, T_J = 125°C			-100	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25V, V_{DS} = 0V			±10	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = -250μA	-1.0	-1.9	-3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250μA, referenced to 25°C		-5.3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -10V, I_D = -8.5A		14.6	20.0	mΩ
		V_{GS} = -4.5V, I_D = -6.3A		23.1	37.0	mΩ
		V_{GS} = -10V, I_D = -8.5A, T_J = 125°C		20.7	28.0	mΩ
g_{FS}	Forward Transconductance	V_{DD} = -5V, I_D = -8.5A		24		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1MHz		1540	2045	pF
C_{oss}	Output Capacitance			295	395	pF
C_{rss}	Reverse Transfer Capacitance			260	385	pF
R_g	Gate Resistance	f = 1MHz		5.1		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -15V, I_D = -8.5A, V_{GS} = -10V, R_{GEN} = 6Ω		10	20	ns
t_r	Rise Time			6	12	ns
$t_{d(off)}$	Turn-Off Delay Time			34	55	ns
t_f	Fall Time			20	36	ns
Q_g	Total Gate Charge	V_{GS}=0V to -10V, V_{DD} = -15V, I_D = -8.5A		33	46	nC
Q_g	Total Gate Charge	V_{GS} = 0V to -4.5V, V_{DD} = -15V, I_D = -8.5A		17	24	nC
Q_{gs}	Gate to Source Charge	V_{DD} = -15V, I_D = -8.5A		5		nC
Q_{gd}	Gate to Drain "Miller" Charge			9		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = -8.5A (Note 2)		0.92	1.5	V
		V_{GS} = 0V, I_S = -1.9A (Note 2)		0.75	1.2	V
t_{rr}	Reverse Recovery Time	I_F = -8.5A, di/dt = 100A/μs		22		ns
Q_{rr}	Reverse Recovery Charge			11		nC

NOTES:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1 in² pad of 2 oz copper

b. 125°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3. Starting T_J = 25°C, L = 1mH, I_{AS} = -7A, V_{DD} = -27V, V_{GS} = -10V.

4. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25°C$ unless otherwise noted

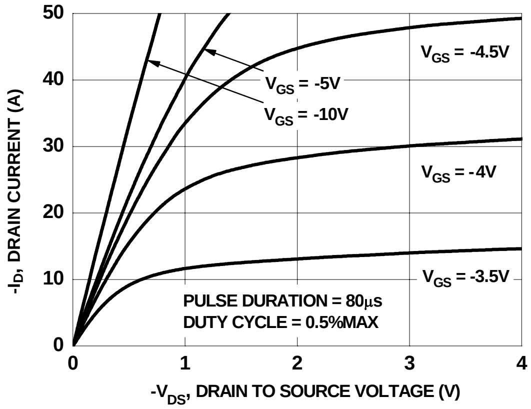


Figure 1. On-Region Characteristics

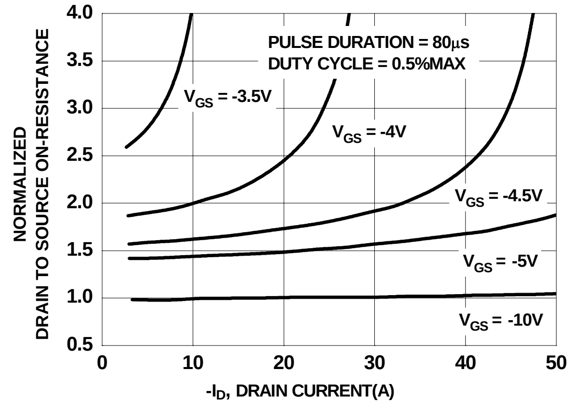


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

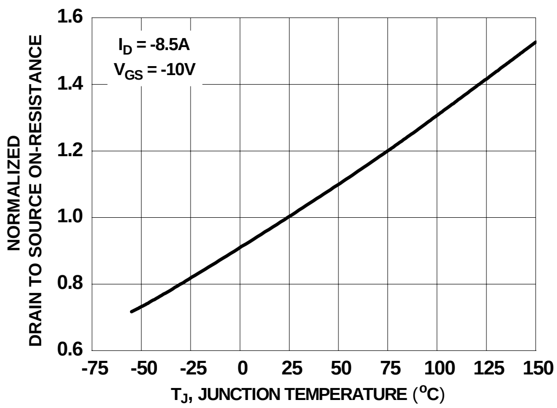


Figure 3. Normalized On-Resistance vs Junction Temperature

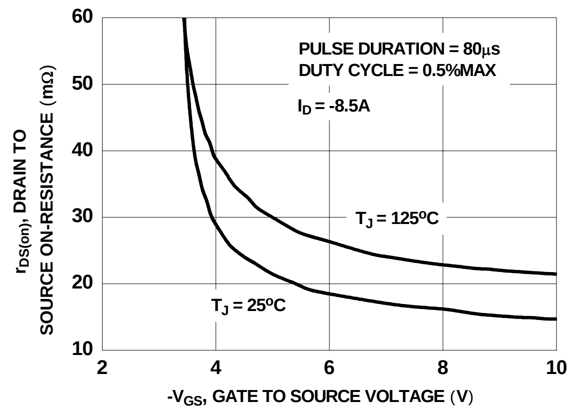


Figure 4. On-Resistance vs Gate to Source Voltage

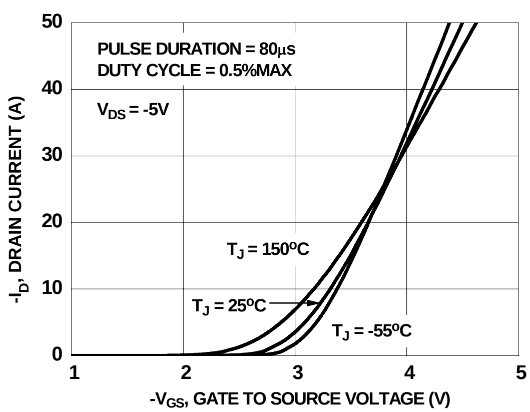


Figure 5. Transfer Characteristics

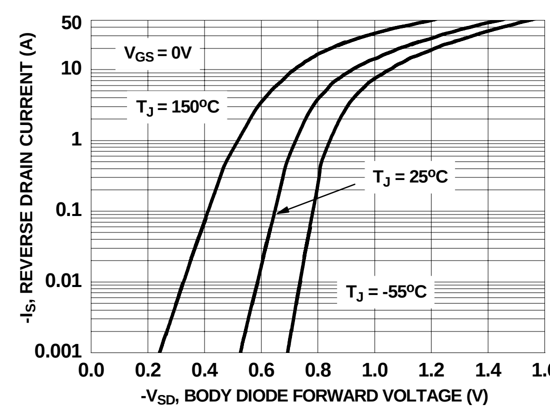


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

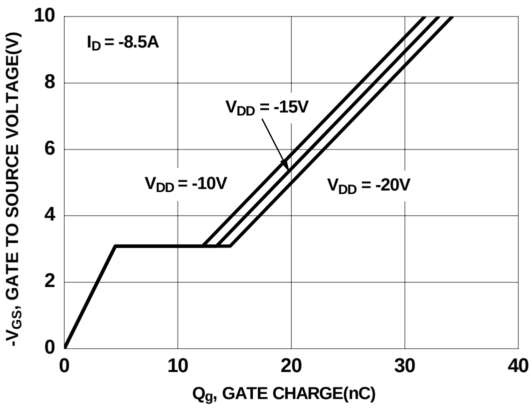


Figure 7. Gate Charge Characteristics

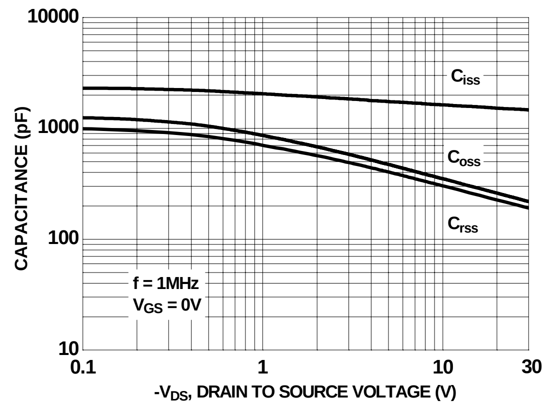


Figure 8. Capacitance vs Drain to Source Voltage

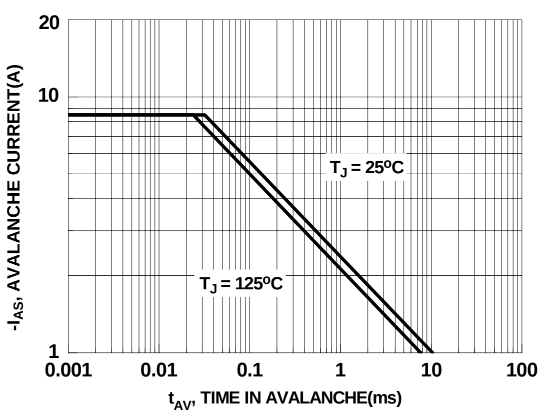


Figure 9. Unclamped Inductive Switching Capability

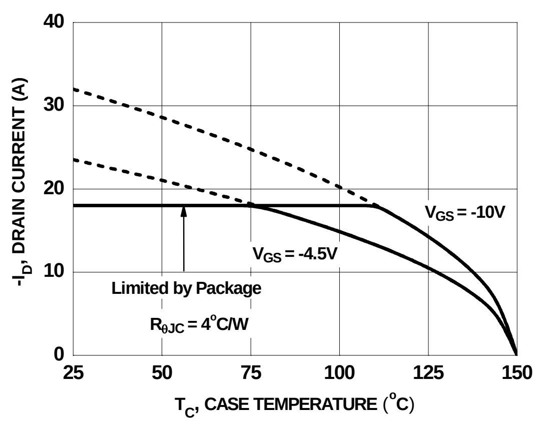


Figure 10. Maximum Continuous Drain Current vs Case Temperature

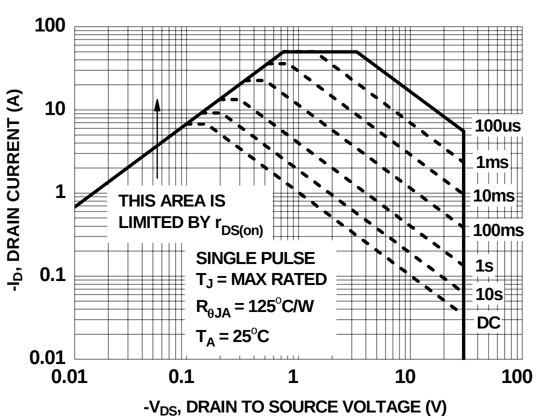


Figure 11. Forward Bias Safe Operating Area

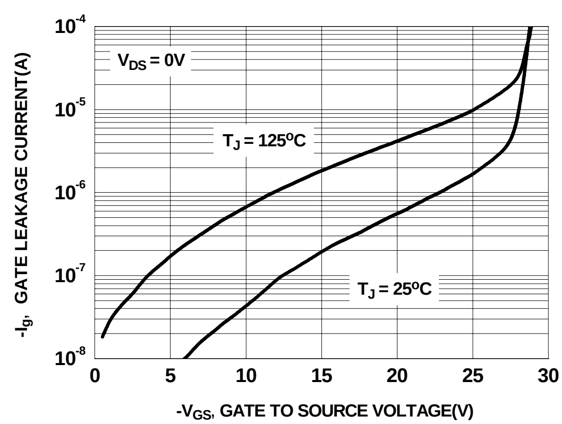


Figure 12. Igss vs Vgss

Typical Characteristics T_J = 25°C unless otherwise noted

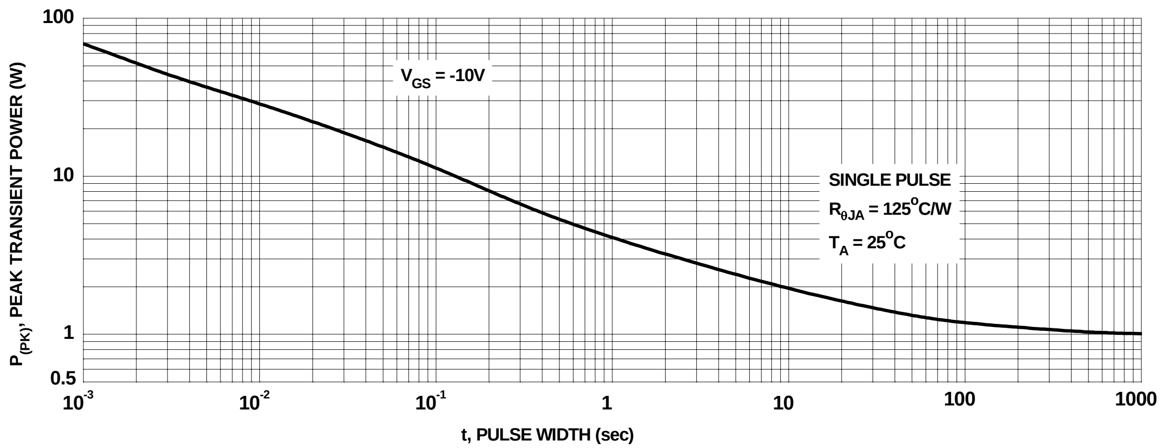


Figure 13. Single Pulse Maximum Power Dissipation

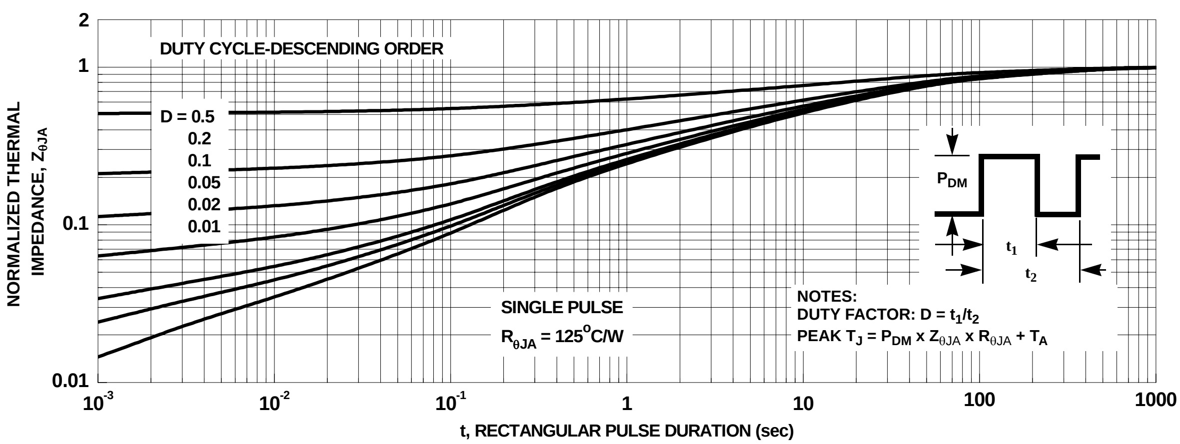
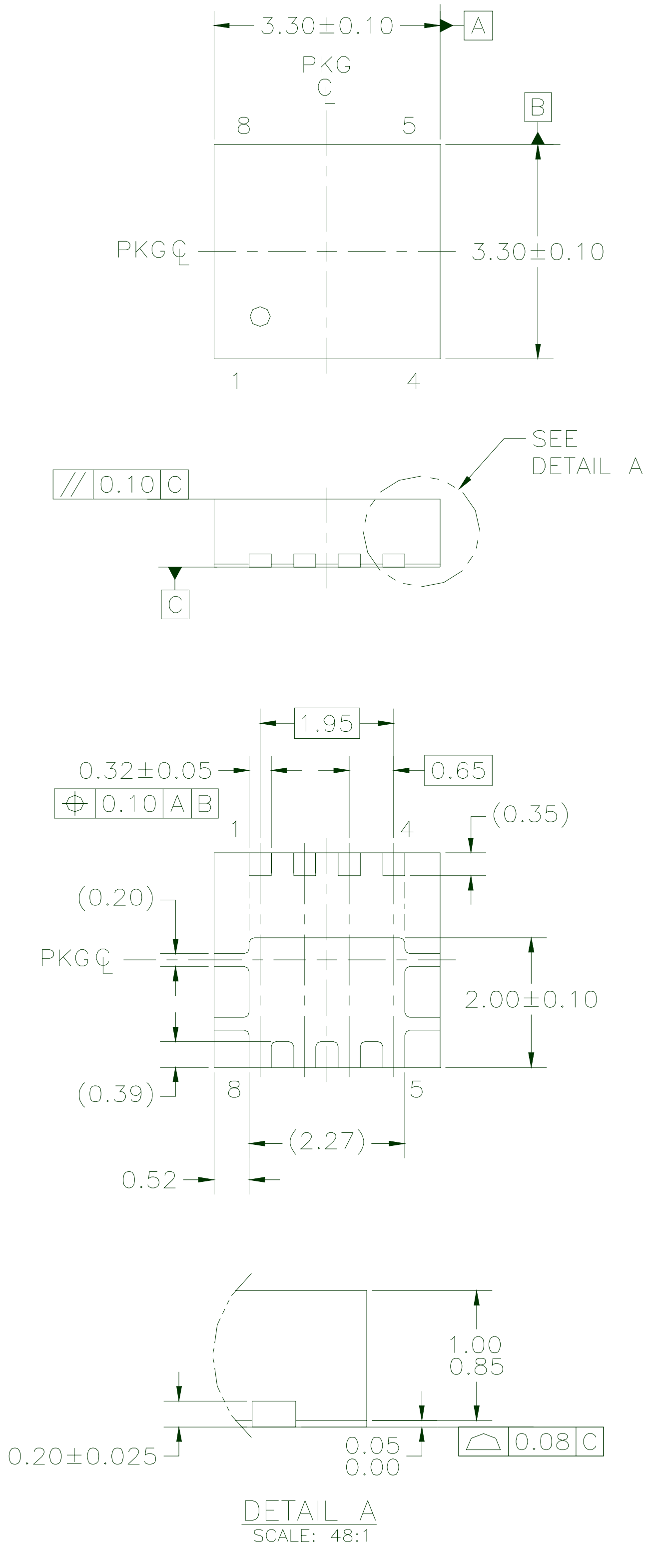
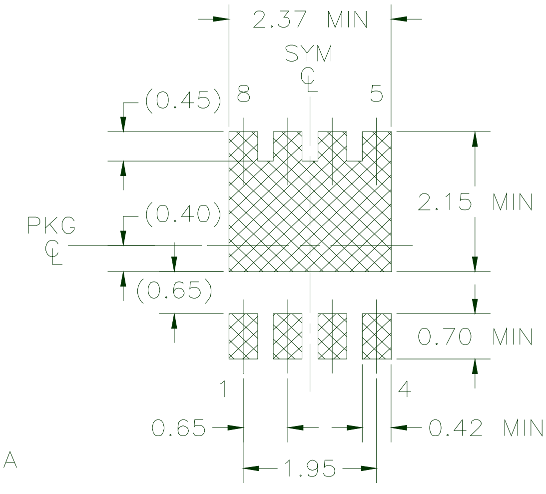


Figure 14. Transient Thermal Response Curve

Dimensional Outline and Pad Layout





LAND PATTERN RECOMMENDATION

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO229, ISSUE B, VEEC, DATED NOVEMBER 2001.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

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Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I34