To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M35044-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

The M35044-XXXSP/FP is a TV screen display control IC. It uses a silicon gate CMOS process and is housed in a 20-pin shrink DIP package (M35044-XXXSP) or a 20-pin shrink SOP package (M35044-XXXFP).

For M35044-001SP/FP that is a standard ROM version of M35044-XXXSP/FP respectively, the character pattern is also mentioned.

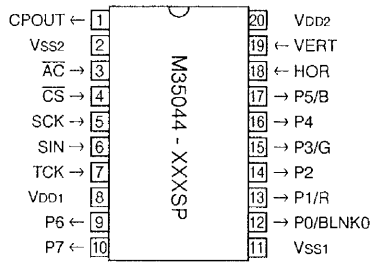
FEATURES

- Screen composition ..... 24 columns × 12 lines
- Number of characters displayed ..... 288 (Max.)
- Character composition ..... 12 × 18 dot matrix
- Characters available ..... 128 characters
- Character sizes available ..... 4 (horizontal) × 4 (vertical)
- Display locations available
  - Horizontal direction ..... 1000 locations
  - Vertical direction ..... 1023 locations
- Blinking ..... Character units
  - Cycle : division of vertical synchronization signal into 64 or 32
  - Duty : 25%, 50%, or 75%
- Data input ..... By the 16-bit serial input function
- Coloring
  - Character color ..... Character unit
  - Background coloring ..... Character unit
  - Matrix-outline (shadow) coloring ..... 8 colors (RGB output) Specified by register
  - Border coloring ..... 8 colors (RGB output) Specified by register
  - Raster coloring ..... 8 colors (RGB output) Specified by register
- Blanking
  - Blanking off
  - Character size blanking
  - Border size blanking
  - Matrix-outline blanking
  - All blanking (all raster area)
- Output ports
  - 4 shared output ports (toggled between RGB output)
  - 4 dedicated output ports
- Display RAM erase function
- Display input frequency range ..... Fosc = 20MHz-80MHz

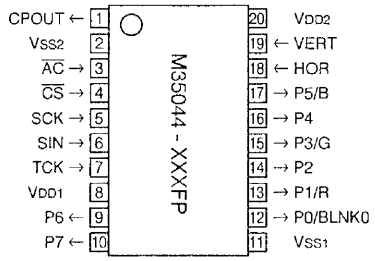
APPLICATION

Monitor

PIN CONFIGURATION (TOP VIEW)

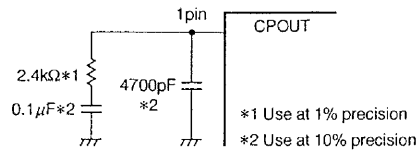


Outline 20P4B

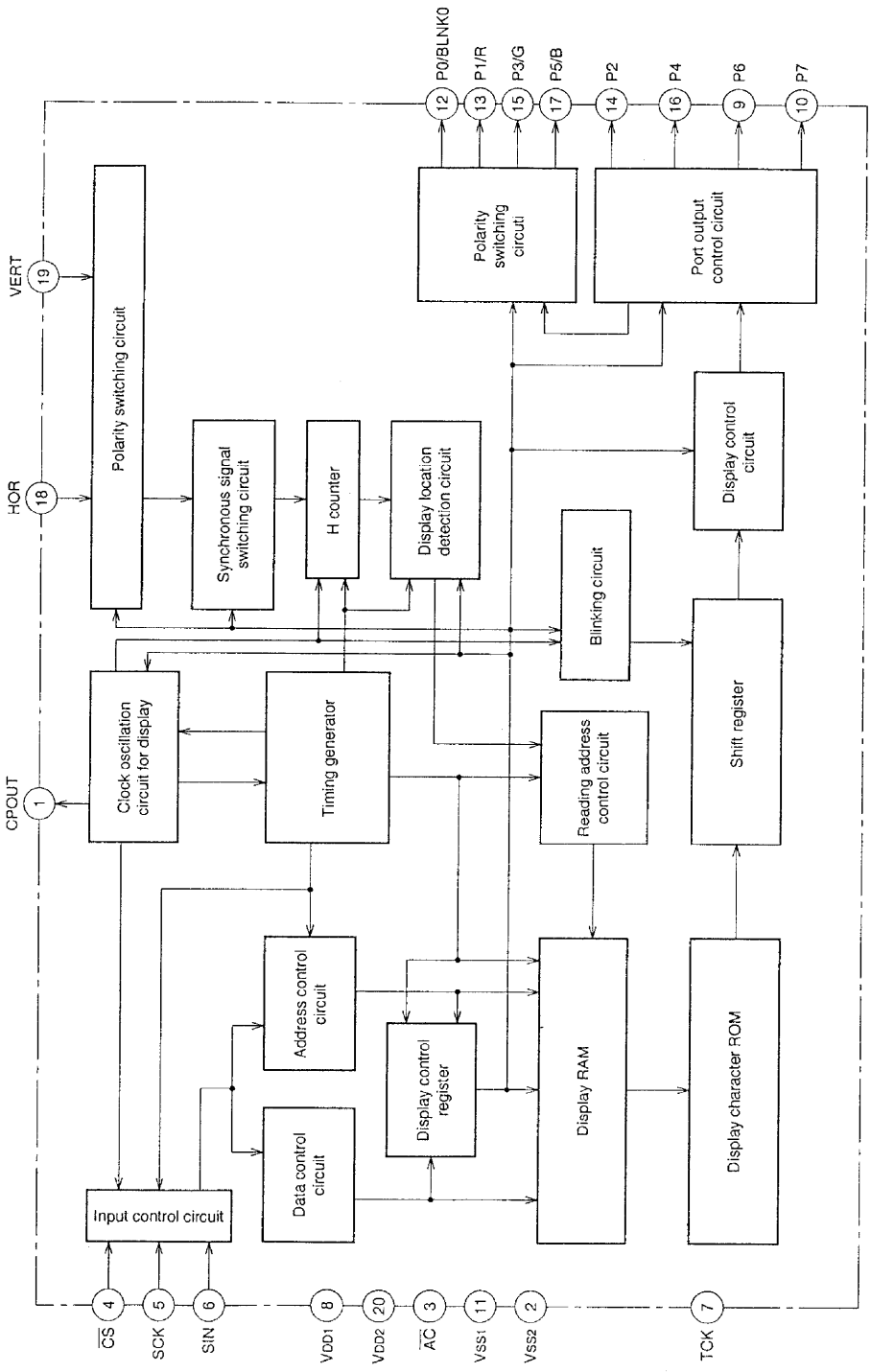


Outline 20P2Q-A

PIN DESCRIPTION

Pin Number	Symbol	Pin name	Input/ Output	Function
1	CPOUT	Phase difference	Output	Connect loop filter to this pin. 
2	VSS2	Earthing pin	–	Please connect to GND using circuit earthing pin.
3	$\overline{AC}$	Auto-clear input	Input	When "L", this pin resets the internal IC circuit. Hysteresis input. Includes built-in pull-up resistor.
4	$\overline{CS}$	Chip select input	Input	This is the chip select pin, and when serial data transmission is being carried out, it goes to "L". Hysteresis input. Includes built-in pull-up resistor.
5	SCK	Serial clock input	Input	When $\overline{CS}$ pin is "L", SIN serial data is taken in when SCK rises. Hysteresis input. Built-in pull-up resistor is included.
6	SIN	Serial data input	Input	This is the pin for serial input of data and addresses for the display control register and the display data memory. Hysteresis input. Includes built-in pull-up resistor.
7	TCK	Test clock	Input	Input for test. Please connect to GND using circuit earthing pin.
8	VDD1	Power pin	–	Please connect to +5V with the power pin.
9	P6	Port P6 output	Output	This is the output port. Port data is set by PTD6.
10	P7	Port P7 output	Output	This is the output port. Port data is set by PTD7.
11	VSS1	Earthing pin	–	Please connect to GND using circuit earthing pin.
12	P0/BLNK0	Port P0 output	Output	This pin can be toggled between port pin output and BLNK0 signal output.
13	P1/R	Port P1 output	Output	This pin can be toggled between port pin output and R signal output.
14	P2	Port P2 output	Output	This is the output port. Port data is set by PTD2.
15	P3/G	Port P3 output	Output	This pin can be toggled between port pin output and G signal output.
16	P4	Port P4 output	Output	This is the output port. Port data is set by PTD4.
17	P5/B	Port P5 output	Output	This pin can be toggled between port pin output and B signal output.
18	HOR	Horizontal synchronization signal input	Input	This pin inputs the horizontal synchronization signal. Hysteresis input.
19	VERT	Vertical synchronization signal input	Input	This pin inputs the vertical synchronization signal. Hysteresis input.
20	VDD2	Power pin	–	Please connect to +5V with the power pin.

BLOCK DIAGRAM



MEMORY CONSTITUTION

Address 000₁₆ to 11F₁₆ are assigned to the display RAM, address 120₁₆ to 128₁₆ are assigned to the display control registers. The internal circuit is reset and all display control registers (address 120₁₆ to 128₁₆) are set to "0" and display RAM (address 000₁₆ to 11F₁₆) are set to "FF₁₆" when the $\overline{AC}$ pin level is "L".
Memory constitution is shown in Figure 1.

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM. The screen constitution is shown in Figure 2.

	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
000₁₆	0	BB	BG	BR	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0
⋮	⋮	Background coloring			Blinking	Character color			⋮	Character code						
11F₁₆	0	BB	BG	BR	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0
120₁₆	0	0	VJT	DIVS1	DIVS0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
121₁₆	0	0	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
122₁₆	0	0	SPACE2	SPACE1	SPACE0	TEST9	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
123₁₆	0	0	TEST3	TEST2	TEST1	TEST0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
124₁₆	0	0	TEST5	TEST4	DSP11	DSP10	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0
125₁₆	0	0	VSZ1H1	VSZ1H0	VSZ1L1	VSZ1L0	V1SZ1	V1SZ0	LIN9	LIN8	LIN7	LIN6	LIN5	LIN4	LIN3	LIN2
126₁₆	0	0	VSZ2H1	VSZ2H0	VSZ2L1	VSZ2L0	V18SZ1	V18SZ0	LIN17	LIN16	LIN15	LIN14	LIN13	LIN12	LIN11	LIN10
127₁₆	0	0	HSZ21	HSZ20	HSZ11	HSZ10	BETA14	TEST8	TEST7	TEST6	FB	FG	FR	RB	RG	RR
128₁₆	0	0	BLINK2	BLINK1	BLINK0	DSPON	STOP	RAMERS	SYAD	BLK1	BLK0	POLH	POLV	VMASK	B/$\overline{F}$	BCOL

Fig. 1 Memory constitution

Line \ Row	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	000₁₆	001₁₆	002₁₆	003₁₆	004₁₆	005₁₆	006₁₆	007₁₆	008₁₆	009₁₆	00A₁₆	00B₁₆	00C₁₆	00D₁₆	00E₁₆	00F₁₆	010₁₆	011₁₆	012₁₆	013₁₆	014₁₆	015₁₆	016₁₆	017₁₆
2	018₁₆	019₁₆	01A₁₆	01B₁₆	01C₁₆	01D₁₆	01E₁₆	01F₁₆	020₁₆	021₁₆	022₁₆	023₁₆	024₁₆	025₁₆	026₁₆	027₁₆	028₁₆	029₁₆	02A₁₆	02B₁₆	02C₁₆	02D₁₆	02E₁₆	02F₁₆
3	030₁₆	031₁₆	032₁₆	033₁₆	034₁₆	035₁₆	036₁₆	037₁₆	038₁₆	039₁₆	03A₁₆	03B₁₆	03C₁₆	03D₁₆	03E₁₆	03F₁₆	040₁₆	041₁₆	042₁₆	043₁₆	044₁₆	045₁₆	046₁₆	047₁₆
4	048₁₆	049₁₆	04A₁₆	04B₁₆	04C₁₆	04D₁₆	04E₁₆	04F₁₆	050₁₆	051₁₆	052₁₆	053₁₆	054₁₆	055₁₆	056₁₆	057₁₆	058₁₆	059₁₆	05A₁₆	05B₁₆	05C₁₆	05D₁₆	05E₁₆	05F₁₆
5	060₁₆	061₁₆	062₁₆	063₁₆	064₁₆	065₁₆	066₁₆	067₁₆	068₁₆	069₁₆	06A₁₆	06B₁₆	06C₁₆	06D₁₆	06E₁₆	06F₁₆	070₁₆	071₁₆	072₁₆	073₁₆	074₁₆	075₁₆	076₁₆	077₁₆
6	078₁₆	079₁₆	07A₁₆	07B₁₆	07C₁₆	07D₁₆	07E₁₆	07F₁₆	080₁₆	081₁₆	082₁₆	083₁₆	084₁₆	085₁₆	086₁₆	087₁₆	088₁₆	089₁₆	08A₁₆	08B₁₆	08C₁₆	08D₁₆	08E₁₆	08F₁₆
7	090₁₆	091₁₆	092₁₆	093₁₆	094₁₆	095₁₆	096₁₆	097₁₆	098₁₆	099₁₆	09A₁₆	09B₁₆	09C₁₆	09D₁₆	09E₁₆	09F₁₆	0A0₁₆	0A1₁₆	0A2₁₆	0A3₁₆	0A4₁₆	0A5₁₆	0A6₁₆	0A7₁₆
8	0A8₁₆	0A9₁₆	0AA₁₆	0AB₁₆	0AC₁₆	0AD₁₆	0AE₁₆	0AF₁₆	0B0₁₆	0B1₁₆	0B2₁₆	0B3₁₆	0B4₁₆	0B5₁₆	0B6₁₆	0B7₁₆	0B8₁₆	0B9₁₆	0BA₁₆	0BB₁₆	0BC₁₆	0BD₁₆	0BE₁₆	0BF₁₆
9	0C0₁₆	0C1₁₆	0C2₁₆	0C3₁₆	0C4₁₆	0C5₁₆	0C6₁₆	0C7₁₆	0C8₁₆	0C9₁₆	0CA₁₆	0CB₁₆	0CC₁₆	0CD₁₆	0CE₁₆	0CF₁₆	0D0₁₆	0D1₁₆	0D2₁₆	0D3₁₆	0D4₁₆	0D5₁₆	0D6₁₆	0D7₁₆
10	0D8₁₆	0D9₁₆	0DA₁₆	0DB₁₆	0DC₁₆	0DD₁₆	0DE₁₆	0DF₁₆	0E0₁₆	0E1₁₆	0E2₁₆	0E3₁₆	0E4₁₆	0E5₁₆	0E6₁₆	0E7₁₆	0E8₁₆	0E9₁₆	0EA₁₆	0EB₁₆	0EC₁₆	0ED₁₆	0EE₁₆	0EF₁₆
11	0F0₁₆	0F1₁₆	0F2₁₆	0F3₁₆	0F4₁₆	0F5₁₆	0F6₁₆	0F7₁₆	0F8₁₆	0F9₁₆	0FA₁₆	0FB₁₆	0FC₁₆	0FD₁₆	0FE₁₆	0FF₁₆	100₁₆	101₁₆	102₁₆	103₁₆	104₁₆	105₁₆	106₁₆	107₁₆
12	108₁₆	109₁₆	10A₁₆	10B₁₆	10C₁₆	10D₁₆	10E₁₆	10F₁₆	110₁₆	111₁₆	112₁₆	113₁₆	114₁₆	115₁₆	116₁₆	117₁₆	118₁₆	119₁₆	11A₁₆	11B₁₆	11C₁₆	11D₁₆	11E₁₆	11F₁₆

※ The hexadecimal numbers in the boxes show the display RAM address.

Fig. 2 Screen constitution

REGISTERS DESCRIPTION

(1) Address 120_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>DIV0</td><td>◎
1</td><td rowspan="13">Set multiply value (frequency value) of horizontal synchronous frequency.

$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$

N1: frequency value</td><td rowspan="13">Display frequency is computed as shown below.

$Fosc = fH \times N1$

Fosc [MHz] : Display frequency
fH [kHz] : Horizontal synchronous signal frequency to HOR pin.
N1 : Shown left

Set display frequency Fosc to within 20MHz to 80MHz range.
When display frequency Fosc, set frequency value N2 in association with DIVS0 and DIVS1.</td></tr>
<tr><td>1</td><td>DIV1</td><td>◎
1</td></tr>
<tr><td>2</td><td>DIV2</td><td>◎
1</td></tr>
<tr><td>3</td><td>DIV3</td><td>◎
1</td></tr>
<tr><td>4</td><td>DIV4</td><td>◎
1</td></tr>
<tr><td>5</td><td>DIV5</td><td>◎
1</td></tr>
<tr><td>6</td><td>DIV6</td><td>◎
1</td></tr>
<tr><td>7</td><td>DIV7</td><td>◎
1</td></tr>
<tr><td>8</td><td>DIV8</td><td>◎
1</td></tr>
<tr><td>9</td><td>DIV9</td><td>◎
1</td></tr>
<tr><td>A</td><td>DIV10</td><td>◎
1</td></tr>
<tr><td>B</td><td>DIVS0</td><td>◎
1</td><td>Set frequency value N2
<table><tr><th colspan="2">DIVS</th><th rowspan="2">Frequency value N2</th></tr><tr><th>1</th><th>0</th></tr><tr><td>0</td><td>0</td><td>Division into 2</td></tr><tr><td>0</td><td>1</td><td>Division into 3</td></tr><tr><td>1</td><td>0</td><td>Division into 4</td></tr><tr><td>1</td><td>1</td><td>Division into 6</td></tr></table></td><td>Set frequency value N2 in association with display frequency range.
<table><tr><th>Display frequency</th><th>Frequency value N2</th></tr><tr><td>55 ~ 80MHz</td><td>Division into 2</td></tr><tr><td>40 ~ 55MHz</td><td>Division into 3</td></tr><tr><td>27.5 ~ 40MHz</td><td>Division into 4</td></tr><tr><td>20 ~ 27.5MHz</td><td>Division into 6</td></tr></table></td></tr>
<tr><td>C</td><td>DIVS1</td><td>◎
1</td></tr>
<tr><td>D</td><td>VJT</td><td>◎</td><td>Normally set to "0".</td><td rowspan="2">The continuous jitter occurrence of display character vertical direction which is generated by overlapping of horizontal synchronous signal phase and vertical synchronous signal phase is able to be reduced.</td></tr>
<tr><td></td><td>1</td><td>Reduce the continuous jitter of vertical direction.</td></tr>
</table>

Note: The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

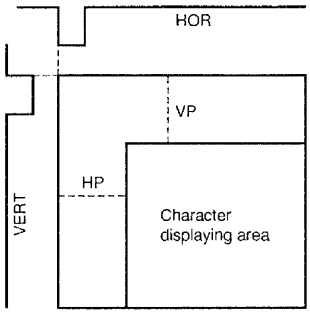
(2) Address 121_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	PTC0	0	P0 output (port P0). Port data is set by PTD0.	BLNK0 outputs blanking signal. Blanking status is determined by BLK0, BLK1, and DSP0 to DSP11 settings.
		1	BLNK0 output. Polarity is set by PTD0.	
1	PTC1	0	P1 output (port P1). Port data is set by PTD1.	
		1	R signal output. Polarity is set by PTD1.	
2	PTC2	0	P2 output (port P2). Port data is set by PTD2.	
		1	Do not set.	
3	PTC3	0	P3 output (port P3). Port data is set by PTD3.	
		1	G signal output. Polarity is set by PTD3.	
4	PTC4	0	P4 output (port P4). Port data is set by PTD4.	
		1	Do not set.	
5	PTC5	0	P5 output (port P5). Port data is set by PTD5.	
		1	B signal output. Polarity is set by PTD5.	
6	PTD0	0	"L" output (P0 output) or negative polarity output (BLNK0 output).	P0 pin data control.
		1	"H" output (P0 output) or positive polarity output (BLNK0 output).	
7	PTD1	0	"L" output (P1 output) or negative polarity output (R signal output).	P1 pin data control.
		1	"H" output (P1 output) or positive polarity output (R signal output).	
8	PTD2	0	"L" output (P2 output).	P2 pin exclusive port output state control.
		1	"H" output (P2 output).	
9	PTD3	0	"L" output (P3 output) or negative polarity output (G signal output).	P3 pin data control.
		1	"H" output (P3 output) or positive polarity output (G signal output).	
A	PTD4	0	"L" output (P2 output).	P4 pin exclusive port output state control.
		1	"H" output (P2 output).	
B	PTD5	0	"L" output (P5 output) or negative polarity output (B signal output).	P5 pin data control.
		1	"H" output (P5 output) or positive polarity output (B signal output).	
C	PTD6	0	"L" output (P6 output).	P6 pin exclusive port output state control.
		1	"H" output (P6 output).	
D	PTD7	0	"L" output (P7 output).	P7 pin exclusive port output state control.
		1	"H" output (P7 output).	

(3) Address 122_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">HP0
(LSB)</td><td>0</td><td rowspan="11">If HS is the horizontal display start location,
$HS = T \times (\sum_{n=0}^{9} 2^n HPn + N)$.
T: The cycle of display frequency
<table><tr><th>HSZ11
HSZ21</th><th>HSZ10
HSZ20</th><th>N</th></tr><tr><td>0</td><td>0</td><td>6</td></tr><tr><td>0</td><td>1</td><td>7</td></tr><tr><td>1</td><td>0</td><td>8</td></tr><tr><td>1</td><td>1</td><td>9</td></tr></table>1000 settings are possible.</td><td rowspan="11">Horizontal display start location is specified using the 10 bits from HP9 to HP0.
Note: HP9 to 0 = (0000000000₂) to (0000010111₂) setting is forbidden</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">HP1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">HP2</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">HP3</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">HP4</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">HP5</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">HP6</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">HP7</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">HP8</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">HP9
(MSB)</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">TEST9</td><td>0</td><td>Must be cleared to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Do not set.</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">SPACE0</td><td>0</td><td rowspan="2"><table><tr><th colspan="3">SPACE</th><th>Number of Lines and Space
(S represents space)</th></tr><tr><td>2</td><td>1</td><td>0</td><td></td></tr><tr><td>0</td><td>0</td><td>0</td><td>12</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1 S 10 S 1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2 S 8 S 2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>3 S 6 S 3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>4 S 4 S 4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>5 S 2 S 5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>6 S 6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>6 S S 6</td></tr></table>S represents one line worth of spaces.</td><td rowspan="2">Leave one line worth of space in the vertical direction.
For example, 6 S 6 indicates two sets of 6 lines with a line of spaces between lines 6 and 7.
A line is 18 × N horizontal scan lines.
N is determined by the character size in the vertical direction as follows:
×1 N = 1 ×2 N = 2
×3 N = 3 ×4 N = 4</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">SPACE1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">SPACE2</td><td>0</td></tr>
<tr><td>1</td></tr>
</table>

(4) Address 123_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	VP0 (LSB)	0	If VS is the vertical display start location, $VS = H \times (\sum_{n=0}^{9} 2^n VP_n)$. H: Cycle with the horizontal synchronizing pulse 1023 settings are possible.  	The vertical start location is specified using the 10 bits from VP9 to VP0. VP9 to VP0 = (0000000000$_2$) setting is forbidden. Note 1: In case of B/$\overline{F}$ register is "0".
		1		
1	VP1	0		
		1		
2	VP2	0		
		1		
3	VP3	0		
		1		
4	VP4	0		
		1		
5	VP5	0		
		1		
6	VP6	0		
		1		
7	VP7	0		
		1		
8	VP8	0		
		1		
9	VP9 (MSB)	0		
		1		
A	TEST0	0	Must be cleared to "0".	
		1	Do not set.	
B	TEST1	0	Must be cleared to "0".	
		1	Do not set.	
C	TEST2	0	Must be cleared to "0".	
		1	Do not set.	
D	TEST3	0	Must be cleared to "0".	
		1	Do not set.	

(5) Address 124_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	DSP0	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 1.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
1	DSP1	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 2.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
2	DSP2	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 3.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
3	DSP3	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 4.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
4	DSP4	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 5.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
5	DSP5	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 6.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
6	DSP6	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 7.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
7	DSP7	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 8.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
8	DSP8	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 9.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
9	DSP9	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 10.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
A	DSP10	0	Blanking is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 11.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
B	DSP11	0	Blanking is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 12.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
C	TEST4	0	Must be cleared to "0".	
		1	Do not set.	
D	TEST5	0	Must be cleared to "0".	
		1	Do not set.	

Note: Refer to DISPLAY FORM1.

(6) Address 125$_{16}$

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>LIN2</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 2nd line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>1</td><td>LIN3</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 3rd line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>2</td><td>LIN4</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 4th line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>3</td><td>LIN5</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 5th line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>4</td><td>LIN6</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 6th line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>5</td><td>LIN7</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 7th line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>6</td><td>LIN8</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 8th line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>7</td><td>LIN9</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 9th line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>8</td><td>V1SZ0</td><td>0</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>V1SZ1</th><th>V1SZ0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction for the 1st line.
(display monitor 1 ~ 12 line)</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>9</td><td>V1SZ1</td><td>0</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse</td><td rowspan="2">Character size setting in the vertical direction (display monitor 1 line) at "0" state in register LIN2 ~ LIN17.</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>A</td><td>VSZ1L0</td><td>0</td><td rowspan="2"><table><tr><th>VSZ1L1</th><th>VSZ1L0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2"></td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>B</td><td>VSZ1L1</td><td>0</td><td rowspan="2"></td><td rowspan="2"></td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>C</td><td>VSZ1H0</td><td>0</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse</td><td rowspan="2">Character size setting in the vertical direction (display monitor 1 line) at "1" state in register LIN2 ~ LIN17.</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D</td><td>VSZ1H1</td><td>0</td><td rowspan="2"><table><tr><th>VSZ1H1</th><th>VSZ1H0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2"></td></tr>
<tr><td></td><td>1</td></tr>
</table>

(7) Address 126₁₆

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>LIN10</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 10th line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>1</td><td>LIN11</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 11th line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>2</td><td>LIN12</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 12th line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>3</td><td>LIN13</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 13th line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>4</td><td>LIN14</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 14th line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>5</td><td>LIN15</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 15th line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>6</td><td>LIN16</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 16th line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>7</td><td>LIN17</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 17th line.</td></tr>
<tr><td></td><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td>8</td><td>V18SZ0</td><td>0</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>V18SZ1</th><th>V18SZ0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction for the 18th line.
(display monitor 1 ~ 12 line)</td></tr>
<tr><td>9</td><td>V18SZ1</td><td>0</td></tr>
<tr><td>A</td><td>VSZ2L0</td><td>0</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ2L1</th><th>VSZ2L0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction (display monitor for 2 ~ 12 line) at "0" state in register LIN2 ~ LIN17.</td></tr>
<tr><td>B</td><td>VSZ2L1</td><td>0</td></tr>
<tr><td>C</td><td>VSZ2H0</td><td>0</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ2H1</th><th>VSZ2H0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction (display monitor for 2 ~ 12 line) at "1" state in register LIN2 ~ LIN17.</td></tr>
<tr><td>D</td><td>VSZ2H1</td><td>0</td></tr>
</table>

(8) Address 127_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">RR</td><td>0</td><td rowspan="2"><table><tr><th>RB</th><th>RG</th><th>RR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table></td><td rowspan="2">Sets the color of all blankings.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">RG</td><td>0</td><td rowspan="2"></td><td rowspan="2"></td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">RB</td><td>0</td><td rowspan="2"></td><td rowspan="2"></td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">FR</td><td>0</td><td rowspan="2"><table><tr><th>BB</th><th>BG</th><th>BR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table></td><td rowspan="2">Sets the blanking color of the Border size, or the shadow size.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">FG</td><td>0</td><td rowspan="2"></td><td rowspan="2"></td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">FB</td><td>0</td><td rowspan="2"></td><td rowspan="2"></td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">TEST6</td><td>0</td><td>Must be cleared to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Do not set.</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">TEST7</td><td>0</td><td>Must be cleared to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Do not set.</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">TEST8</td><td>0</td><td>Must be cleared to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Do not set.</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">BETA14</td><td>0</td><td>Matrix-outline display (12 × 18 dot)</td><td rowspan="2">Set this register to the character font set by display RAM BR, BG and BB.</td></tr>
<tr><td>1</td><td>Matrix-outline display (14 × 18 dot)</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">HSZ10</td><td>0</td><td rowspan="2">T: Display frequency cycle<table><tr><th>HSZ11</th><th>HSZ10</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction for the first line.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">HSZ11</td><td>0</td><td rowspan="2"></td><td rowspan="2"></td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">HSZ20</td><td>0</td><td rowspan="2">T: Display frequency cycle<table><tr><th>VSZ21</th><th>HSZ20</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction for the 2nd line to 12th line.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">HSZ21</td><td>0</td><td rowspan="2"></td><td rowspan="2"></td></tr>
<tr><td>1</td></tr>
</table>

(9) Address 128_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">BCOL</td><td>0</td><td>Blanking of BLK0, BLK1</td><td rowspan="2">Sets all raster blanking</td></tr>
<tr><td>1</td><td>All raster blanking</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">B/$\overline{F}$</td><td>0</td><td>Synchronize with the leading edge of horizontal synchronization.</td><td rowspan="2">Synchronize with the front porch or back porch of the horizontal synchronazation signal.</td></tr>
<tr><td>1</td><td>Synchronize with the trailing edge of horizontal synchronization.</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">VMASK</td><td>0</td><td>Do not mask by VERT input signal</td><td rowspan="2">This register has or do not have mask at phase comparison operating.</td></tr>
<tr><td>1</td><td>Mask by VERT input signal</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">POLV</td><td>0</td><td>VERT pin polarity is negative electrode</td><td rowspan="2">Set VERT pin polarity.</td></tr>
<tr><td>1</td><td>VERT pin polarity is positive electrode</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">POLH</td><td>0</td><td>HOR pin polarity is negative electrode</td><td rowspan="2">Set HOR pin polarity.</td></tr>
<tr><td>1</td><td>HOR pin polarity is positive electrode</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">BLK0</td><td>0</td><td rowspan="3"><table><tr><th colspan="2">BLK</th><th rowspan="2">Blanking mode</th></tr><tr><th>1</th><th>0</th></tr><tr><td>0</td><td>0</td><td>Matrix-outline size</td></tr><tr><td>0</td><td>1</td><td>Character size</td></tr><tr><td>1</td><td>0</td><td>Border size</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline size</td></tr></table></td><td rowspan="3">Set blanking mode. (Note 1)
An example of blanking mode at BCOL = "0", DSPn = "0" (n = 0 ~ 11) shown left.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">BLK1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">SYAD</td><td>0</td><td>Border display of character</td><td rowspan="2">(Note 2)</td></tr>
<tr><td>1</td><td>Shadow display of character</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">RAMERS</td><td>0</td><td>RAM not erased</td><td rowspan="2">There is no need to reset because there is no register for this bit.</td></tr>
<tr><td>1</td><td>RAM erased</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">STOP</td><td>0</td><td>Oscillation of clock for display</td><td rowspan="2">R, G, B and BLNK0 output can be altered.</td></tr>
<tr><td>1</td><td>Stop the oscillation of clock for display</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">DSPON</td><td>0</td><td>Display OFF</td><td rowspan="2">Display can be altered.</td></tr>
<tr><td>1</td><td>Display ON</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">BLINK0</td><td>0</td><td rowspan="3"><table><tr><th colspan="2">BLINK</th><th rowspan="2">Duty</th></tr><tr><th>1</th><th>0</th></tr><tr><td>0</td><td>0</td><td>Blinking OFF</td></tr><tr><td>0</td><td>1</td><td>25%</td></tr><tr><td>1</td><td>0</td><td>50%</td></tr><tr><td>1</td><td>1</td><td>75%</td></tr></table></td><td rowspan="3">Blinking duty ratio can be altered.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">BLINK1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">BLINK2</td><td>0</td><td>Divided into 64 of vertical synchronous signal</td><td rowspan="2">Blinking frequency can be altered.</td></tr>
<tr><td>1</td><td>Divided into 32 of vertical synchronous signal</td></tr>
</table>

Notes 1: Refer to DISPLAY FORM 1
2: Refer to DISPLAY FORM 3

DISPLAY FORM1

Table 1 shows display form of blanking.

Table 1. Display mode

BCOL	Standard blanking		When the all of registers DSPn (Note 2) are set to "0"	When some of registers DSPi are set to "1"		BLNK0 output
	BLK1	BLK0		DSPn = 0	DSPn = 1	
0	0	0	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline display color set: display RAM (Note 3)	DSPn = "0" line, DSPn = "1" line → Matrix-outline size
	0	1	Character	Character	Border display color set: display RAM (Note 3)	DSPn = "0" line→Character size DSPn = "1" line→Border size
	1	0	Border display color set: display RAM (Note 3)	Border display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	DSPn = "0" line→Border size DSPn = "1" line→Matrix-outline size
	1	1	Matrix-outline display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	Character	DSPn = "0" line→Matrix-outline size DSPn = "1" line→Character size
1 (Note 1)	0	0	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline display color set: display RAM (Note 3)	All blanking size
	0	1	Character	Character	Border display color set: display RAM (Note 3)	
	1	0	Border display color set: display RAM (Note 3)	Border display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	
	1	1	Matrix-outline display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	Character	

Notes 1: Color setting of raster area is set by register RR, RG and RB.
2: DSPn (n = 0 ~ 11)
3: Set by BR, BG and BB of display RAM.
4: Set border by register FR, FG and FB. Set matrix-outline by BR, BG and BB of display RAM.

Display form 2

M35044-XXXSP/FP has the following four display forms.

(1) Character size
: Blanking same as the character size.

(2) Border size
: Blanking the background as a size from character.

(3) Matrix-outline size
: Blanking the background 12 × 18 dot.
When set register BETA14 to "1", setting of blanking the background 14 × 18 dot is possible.

(4) All blanking size
: When set register BCOL to "1", all raster area is blanking.

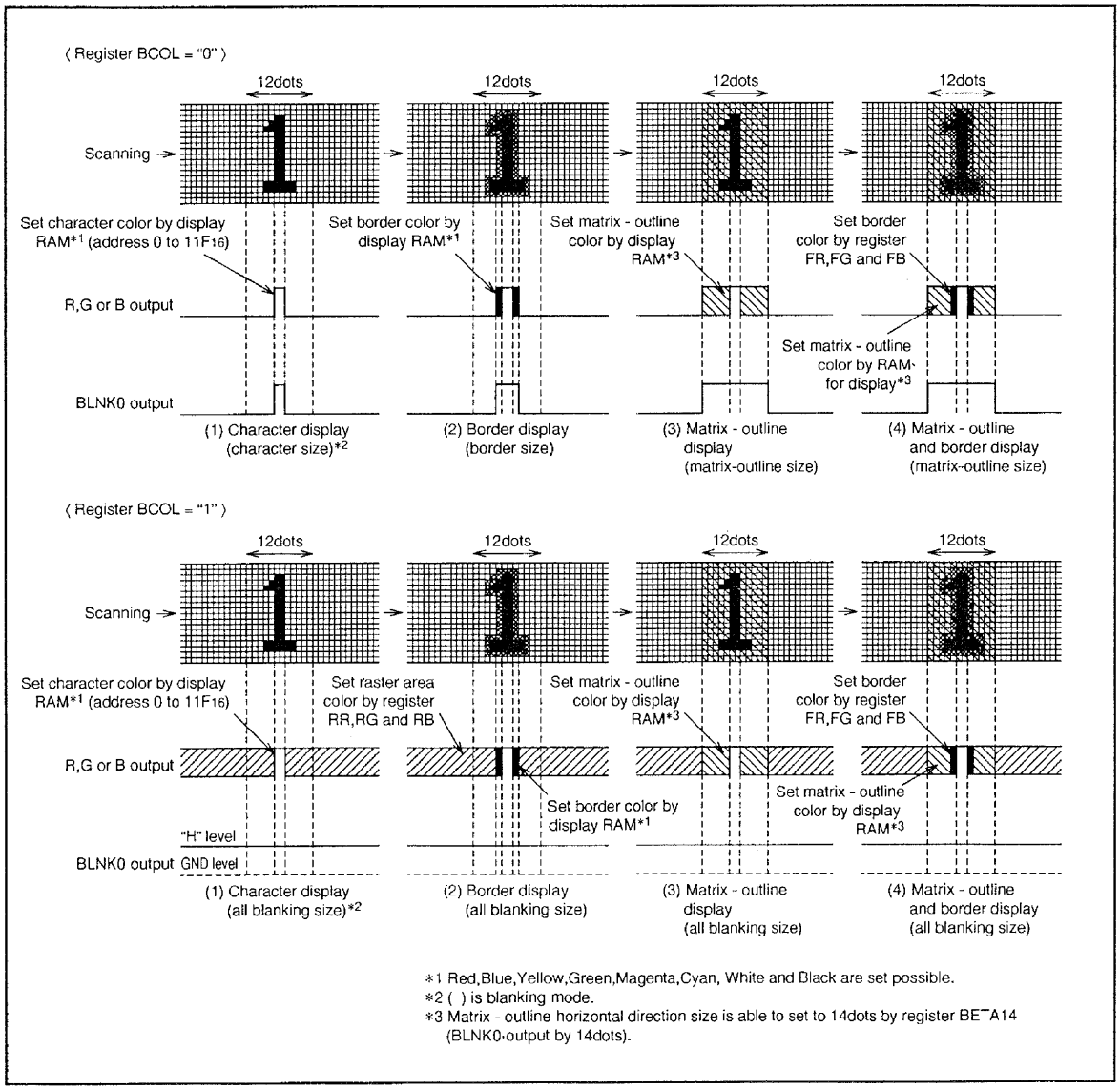


Fig. 3 Display form

Display form 3

When border display mode, if set SYAD = "0" to "1", it change to shadow display mode.
Border and shadow display are shown below.

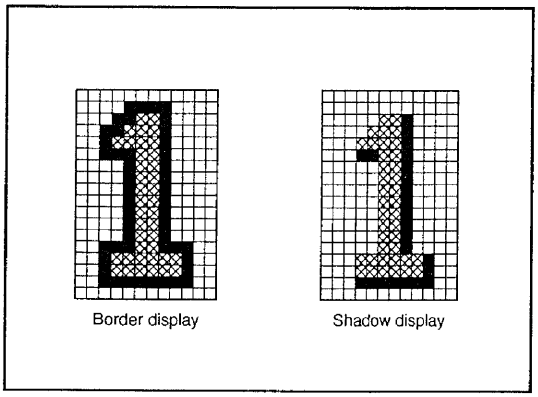


Fig. 4 Border and shadow display

Set shadow display color by display RAM or register FR, FG and FB.

DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by the serial input function. Example of data setting is shown in Figure 5.

Example of data setting by the serial input function (M35044-XXXSP/FP)

No.	Address/Data	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Addition
		200 msec hold																System set-up
1	address 120_{16}	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	Address set
2	data 120_{16}	0	0	1	DIVS1	DIVS0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	Setting frequency dividing value (Note 1)
3	data 121_{16}	0	0	PTD7	PTD6	1	PTD4	1	PTD2	1	1	1	0	1	0	1	1	Output setting
4	data 122_{16}	0	0	0	0	0	0	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display location setting
5	data 123_{16}	0	0	0	0	0	0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display location setting
6	data 124_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Display form setting
7	data 125_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
8	data 126_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
9	data 127_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Color, character size setting
10	data 128_{16}	0	0	0	0	0	0	0	1	0	1	1	POLH	POLV	0	0	0	Display OFF, display form (Note 2)
		200 msec hold																
11	data 000_{16}	0	BB	BG	BR	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0	Character setting
12 ⋮ 297	⋮	⋮	Character background color			Blinking	Character color			⋮	Character code							
298	data $11F_{16}$	0	BB	BG	BR	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0	
299	address 128_{16}	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	Address setting
300	data 128_{16}	0	0	0	0	0	1	0	0	0	1	1	POLH	POLV	0	0	0	Display ON, display form (Note 2)

Notes 1: Input horizontal synchronous signal to HOR pin.
2: Matrix-outline display in this data.

Fig. 5 Example of data setting by the serial input function

SERIAL DATA INPUT TIMING

(1) Serial data should be input with the LSB first.
(2) The address consists of 16 bits.
(3) The data consists of 16 bits.
(4) The 16 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits.

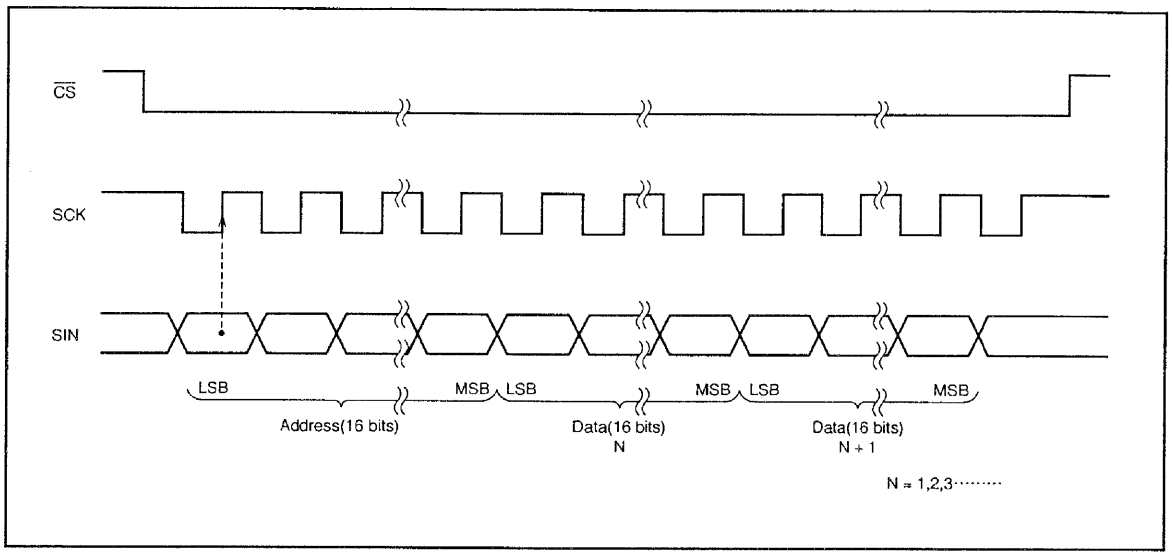


Fig. 6 Serial input timing

CHARACTER FONT

Images are composed on a 12 × 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

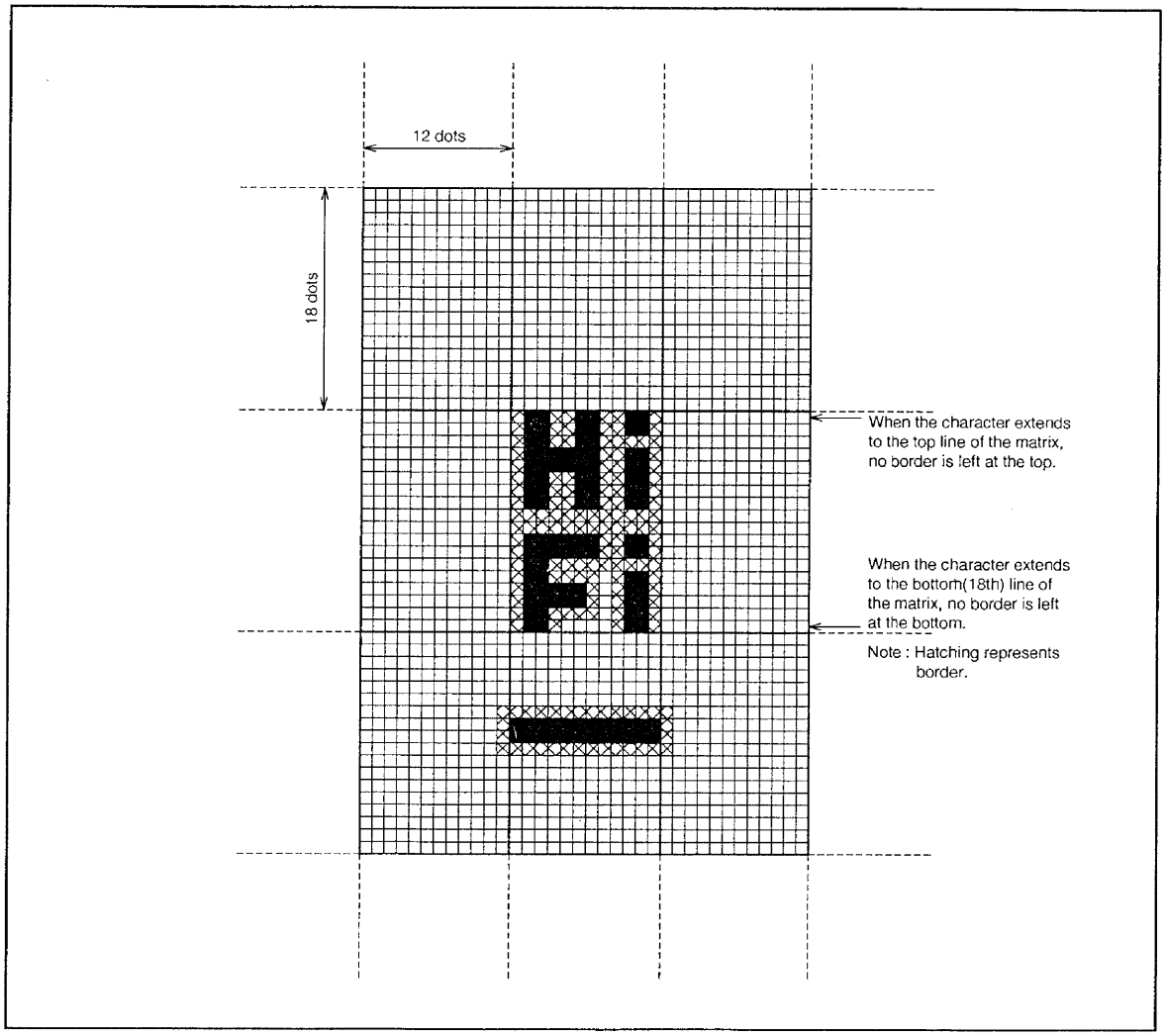


Fig. 7 Example for displaying a continuous pattern after combining characters in the horizontal or vertical direction

Character code FF_{16} is fixed as a blank without background.
Therefore, you cannot register a character font in this code.

TIMING REQUIREMENTS (Ta = –20°C to + 85°C, V_{DD} = 5±0.25V, unless otherwise noted)

Symbol	Parameter	Limits			Unit	Remarks
		Min.	Typ.	Max.		
tw(SCK)	SCK width	200	—	—	ns	See Figure 8
tsu($\overline{CS}$)	$\overline{CS}$ setup time	200	—	—	ns	
th($\overline{CS}$)	$\overline{CS}$ hold time	2	—	—	μs	
tsu(SIN)	SIN setup time	200	—	—	ns	
th(SIN)	SIN hold time	200	—	—	ns	
tword	1 word writing time	10	—	—	μs	

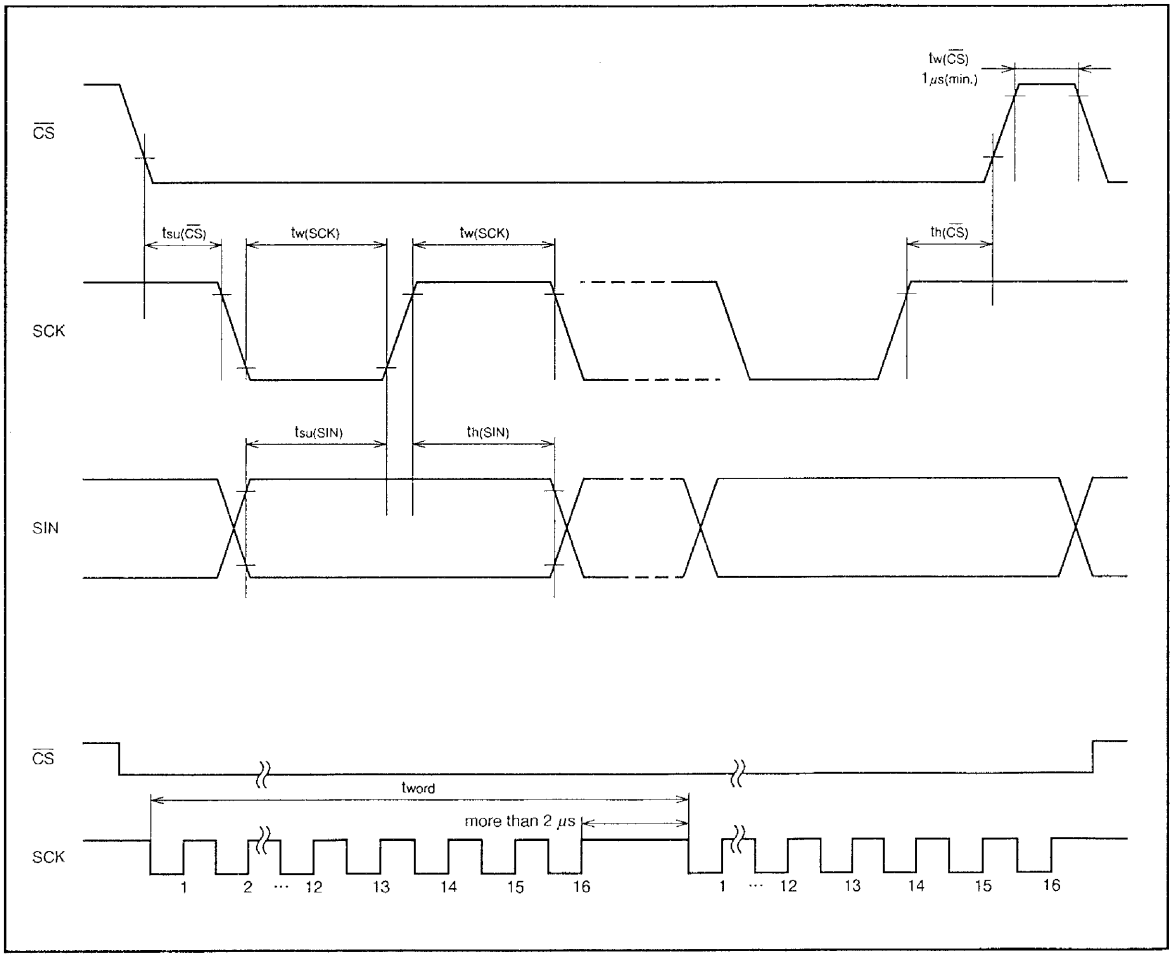


Fig. 8 Serial input timing requirements

EXAMPLE OF THE M35044-XXXSP/FP PERIPHERAL CIRCUIT

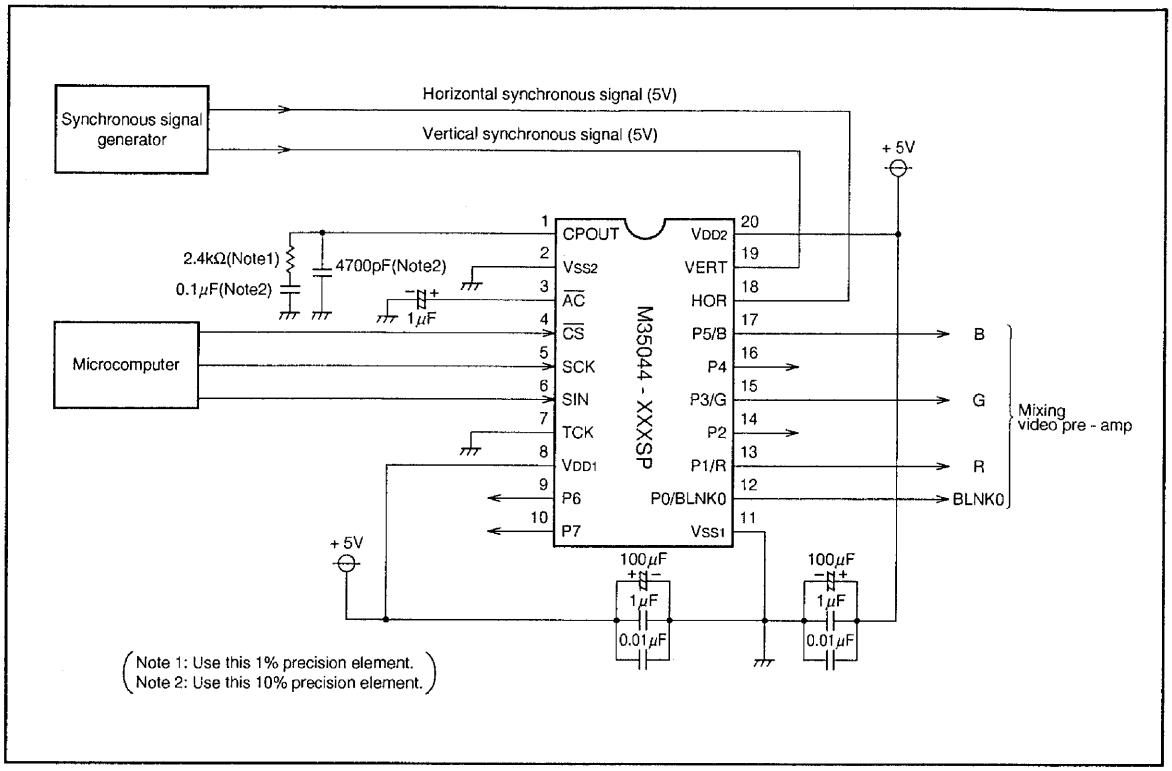


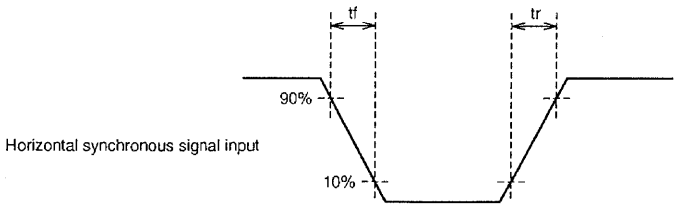
Fig. 9 Example of the M35044-XXXSP peripheral circuit (M35044-XXXFP peripheral circuit is same as that of M35044-XXXSP)

Note for waveform timing of the horizontal signals to the HOR pin.

Set horizontal synchronous signal edge* waveform timing to under 5ns and input to HOR pin.

Set only the side which set by B/$\overline{F}$ register waveform timing under 5ns and input to HOR pin.

*: Set front porch edge or back porch edge by B/$\overline{F}$ register.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to Vss.	−0.3 to +6.0	V
V_I	Input voltage		V_{SS} −0.3 ≦ V_I ≦ V_{DD} +0.3	V
V_O	Output voltage		V_{SS} ≦ V_O ≦ V_{DD}	V
P_d	Power dissipation	Ta = 25°C	300	mW
T_{opr}	Operating temperature		−20 to +85	°C
T_{stg}	Storage temperature		−40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (V_{DD} = 5V, Ta = −20 to +85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{DD}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	"H" level input voltage SIN, SCK, $\overline{CS}$, $\overline{AC}$ HOR, VERT	0.8V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	"L" level input voltage SIN, SCK, $\overline{CS}$, $\overline{AC}$ HOR, VERT	0	0	0.2V_{DD}	V
F_{OSC}	Oscillating frequency for display	20.0	—	80.0	MHz

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply voltage		Ta = −20 to +85°C	4.75	5.0	5.25	V
I_{DD}	Supply current		V_{DD} = 5.25V	—	30	50	mA
V_{OH}	"H" level output voltage	P0 ~ P7	V_{DD} = 4.75V, I_{OH} = 0.4mA	3.5	—	—	V
		CPOUT	V_{DD} = 4.75V, I_{OH} = 0.05mA				
V_{OL}	"L" level output voltage	P0 ~ P7	V_{DD} = 4.75V, I_{OL} = 0.4mA	—	—	0.4	V
		CPOUT	V_{DD} = 4.75V, I_{OL} = 0.05mA				
R_I	Pull-up resistance SCK, $\overline{AC}$, $\overline{CS}$, SIN		V_{DD} = 5.0V	10	30	100	kΩ

Note for Supplying Power

Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35044-XXXSP/FP is reset when the level of the auto clear input pin $\overline{AC}$ is "L". This pin in hysteresis input with the pull-up resistor. The timing about power supplying of $\overline{AC}$ pin is shown in Figure 10.

Timing of power supplying to V_{DD1} and V_{DD2}.

Supply power to V_{DD1} and V_{DD2} at the same time.

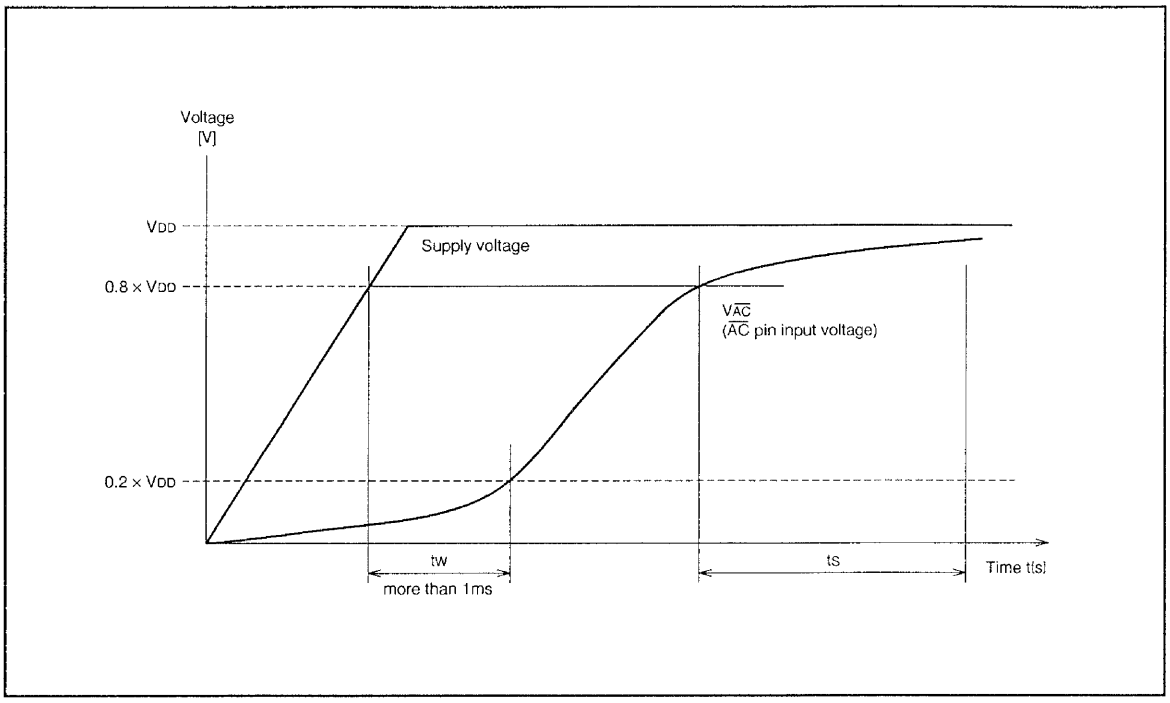


Fig. 10 Timing of power supplying to $\overline{AC}$ pin

After supplying the power (V_{DD} and V_{SS}) to M35044-XXXSP/FP and the supply voltage becomes more than 0.8 × V_{DD}, it needs to keep V_{IL} time; tw of the $\overline{AC}$ pin for more than 1ms.

Start inputting from microcomputer after $\overline{AC}$ pin supply voltage becomes more than 0.8 × V_{DD} and keeping 200ms wait time.

PRECAUTION FOR USE

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor (≈0.1 μF) directly between the V_{DD1} pin and V_{SS} pin, and the V_{DD2} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

(1) M35044-XXXSP/FP mask ROM order confirmation form
(2) Mask specification form
(3) ROM data (EPROM 3 sets)
(4) Floppy disks containing the character font generating program + character data

STANDARD ROM TYPE : M35044-001SP/FP

M35044-001SP/FP is a standard ROM type of M35044-XXXSP/FP.
The character patterns are fixed to the contents of Figure 11 to 13.

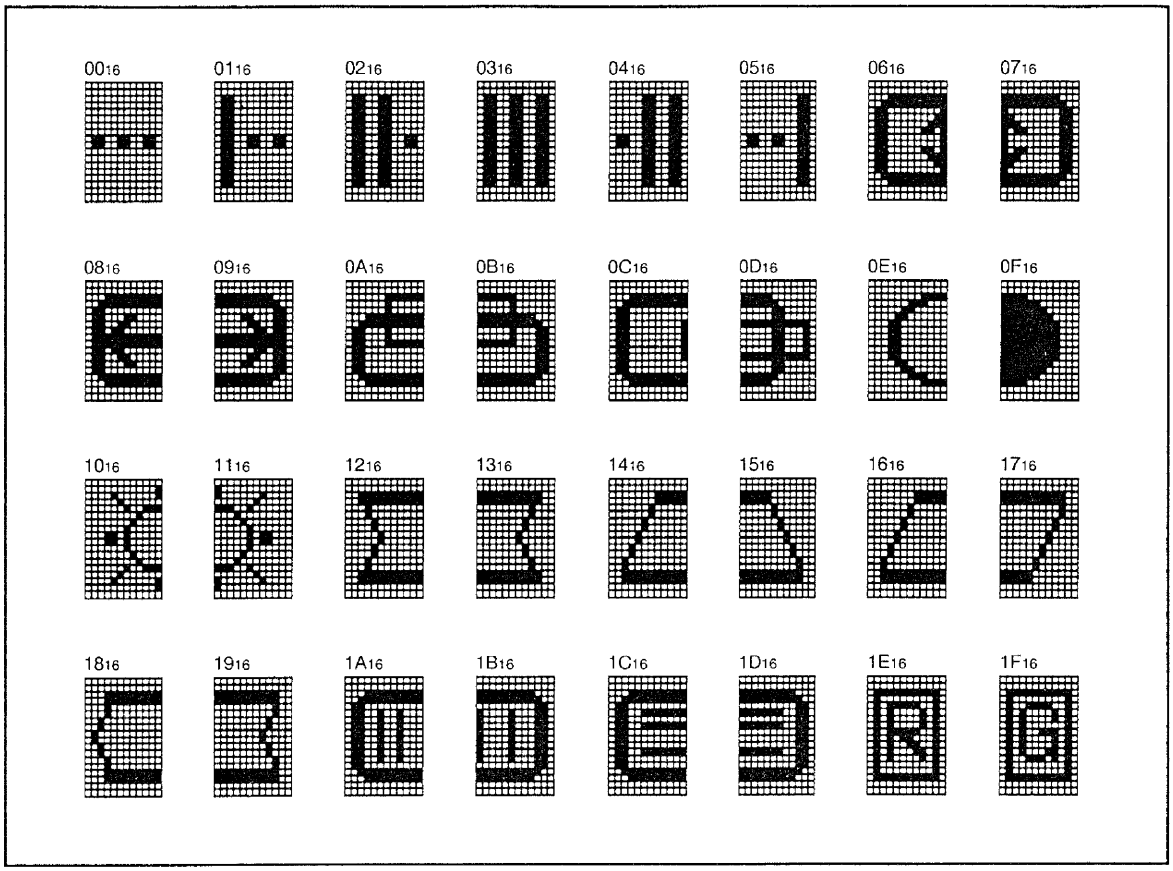


Fig. 11 M35044-001SP/FP character patterns (1)

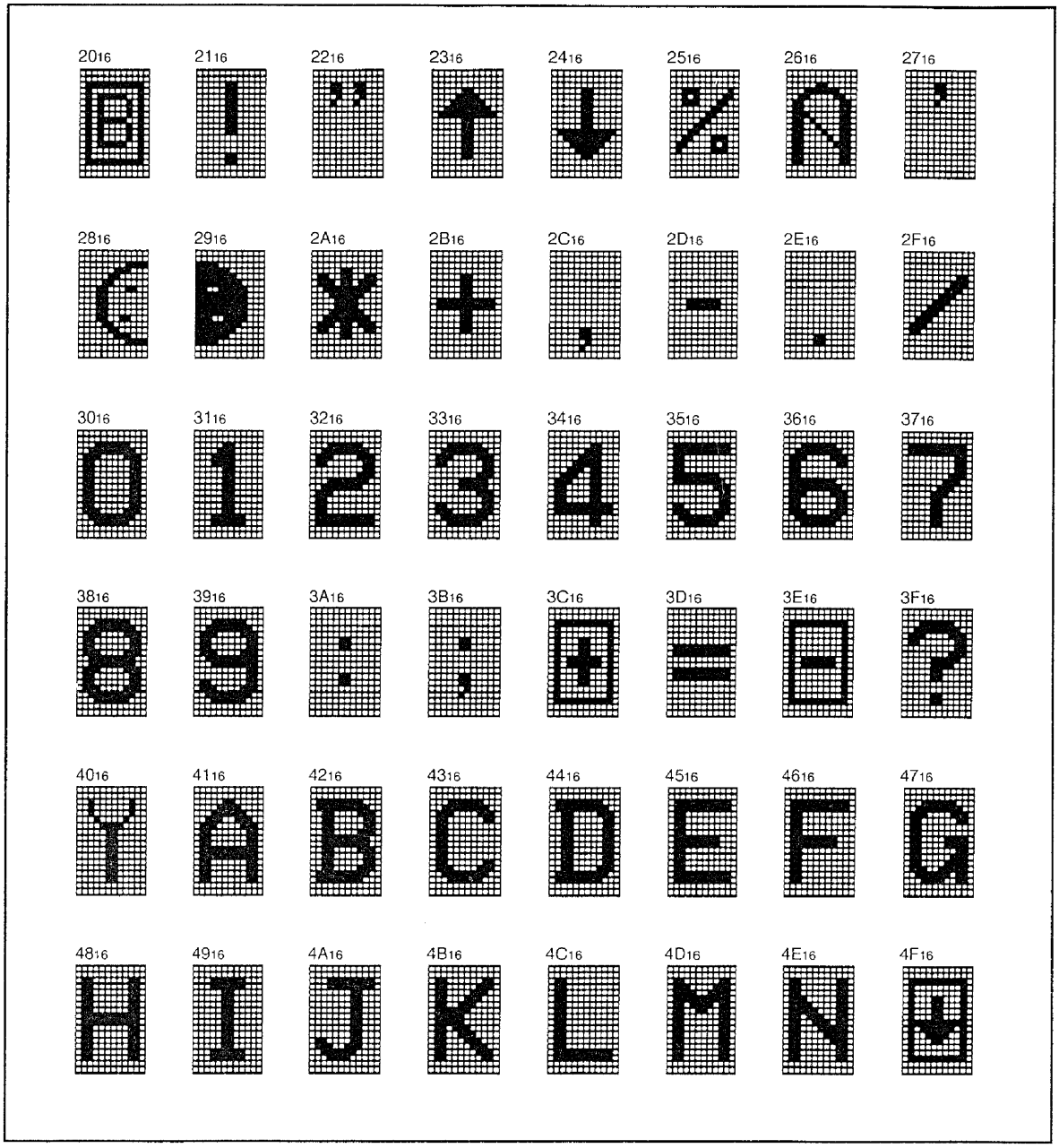


Fig. 12 M35044-001SP/FP character patterns (2)

Fig. 13 M35044-001SP/FP character patterns (3)