

Am25LS2535

Eight-Input Multiplexer with Control Register

DISTINCTIVE CHARACTERISTICS

- High speed eight-input multiplexer
- On-chip Multiplexer Select and Polarity Control Register
- Output polarity control for inverting or non-inverting output
- Common register enable
- Asynchronous register clear
- Three-state output for expansion
- Am25LS features improved noise margin, higher drive, and faster operation

GENERAL DESCRIPTION

The Am25LS2535 is an eight-input Multiplexer with Control Register. The device features high speed from clock to output and is intended for use in high speed computer control units or structured state machine designs.

The Am25LS2535 contains an internal register which holds the A, B, and C multiplexer select lines as well as the POL (polarity) control bit. When the Register Enable input (RE) is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock. When RE is HIGH, the register retains its current data. An asynchronous clear input (CLR) is used to reset the register to a logic LOW level.

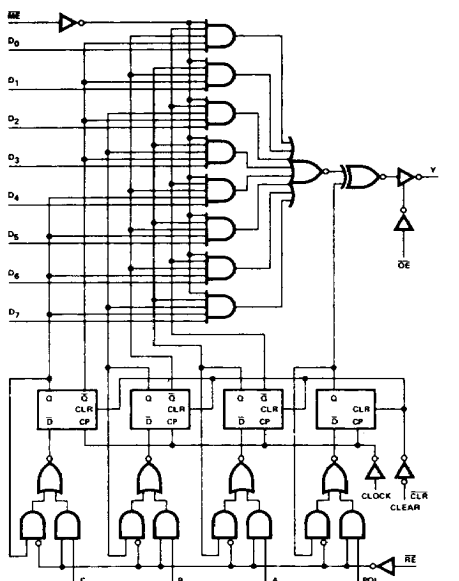
The A, B and C register outputs select one of eight multiplexer data inputs. A HIGH on the Polarity Control flip-

flop output causes a true (non-inverting) multiplexer output, and a LOW causes the output to be inverted. In a computer control unit, this allows testing of either true or complemented flag data at the microprogram sequencer test input.

An active LOW Multiplexer Enable input (\overline{ME}) allows the selected multiplexer input to be passed to the output. When \overline{ME} is HIGH, the output is determined only by the Polarity Control bit.

The Am25LS2535 also features a three-state Output Enable control (\overline{OE}) for expansion. When \overline{OE} is LOW, the output is enabled. When \overline{OE} is HIGH, the output is in the high impedance state.

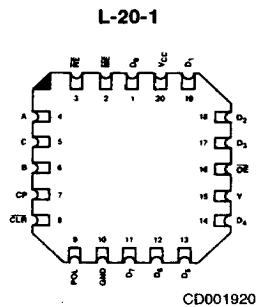
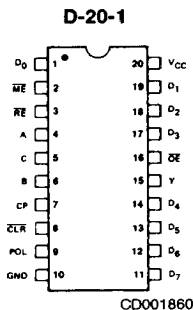
BLOCK DIAGRAM



BD001620

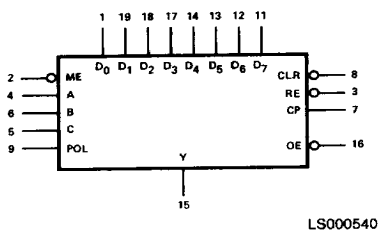
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CONNECTION DIAGRAM Top View

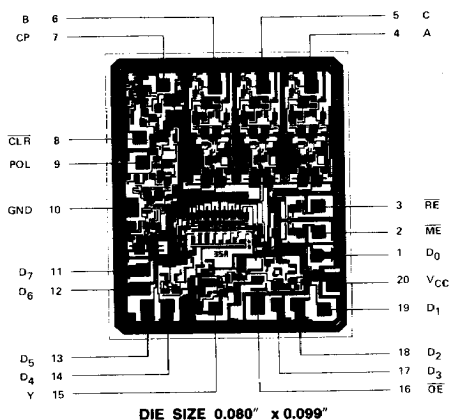


Note: Pin 1 is marked for orientation

LOGIC SYMBOL



METALLIZATION AND PAD LAYOUT



ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2535

D — Screening Option
Blank — Standard processing
B — Burn-in

C — Temperature (See Operating Range)
C — Commercial (0°C to +70°C)
M — Military (-55°C to +125°C)

B — Package
D — 20-pin Cerdip
F — 20-pin flatpak
L — 20-pin leadless chip carrier
P — 20-pin plastic DIP
X — Dice

Device type
8-Input Multiplexer

Valid Combinations

Valid Combinations	
Am25LS2535	PC DC, DM FM LC, LM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
4, 6, 5	A, B, C	O	Multiplexer Select Lines. One of eight multiplexer data inputs is selected by the A, B and C register outputs.
9	POL	O	Polarity Control Bit. A HIGH register output causes a true (non-inverted) output and a LOW causes the output to be inverted.
2	ME		Multiplexer Enable. When LOW, it enabled the 8-input multiplexer. When HIGH, the Y output is determined by only the Polarity Control bit.
3	RE		Register Enable. When LOW, the Multiplexer Select and Polarity Control Register is enabled for loading. When HIGH, the register holds its current data.
8	CLR		Clear. A LOW asynchronously resets the Multiplexer Select and Polarity Control Register.
	D ₁ -D ₈	I	Data inputs to the 8-input multiplexer.
7	CP		Clock Pulse. When RE is LOW, the Multiplexer Select and Polarity Control Register changes state on the LOW-to-HIGH transition of CP.
16	OE	O	Output Enable. When LOW, the output is enabled. When HIGH, the output is in the high-impedance state.
15	Y	O	The chip output.

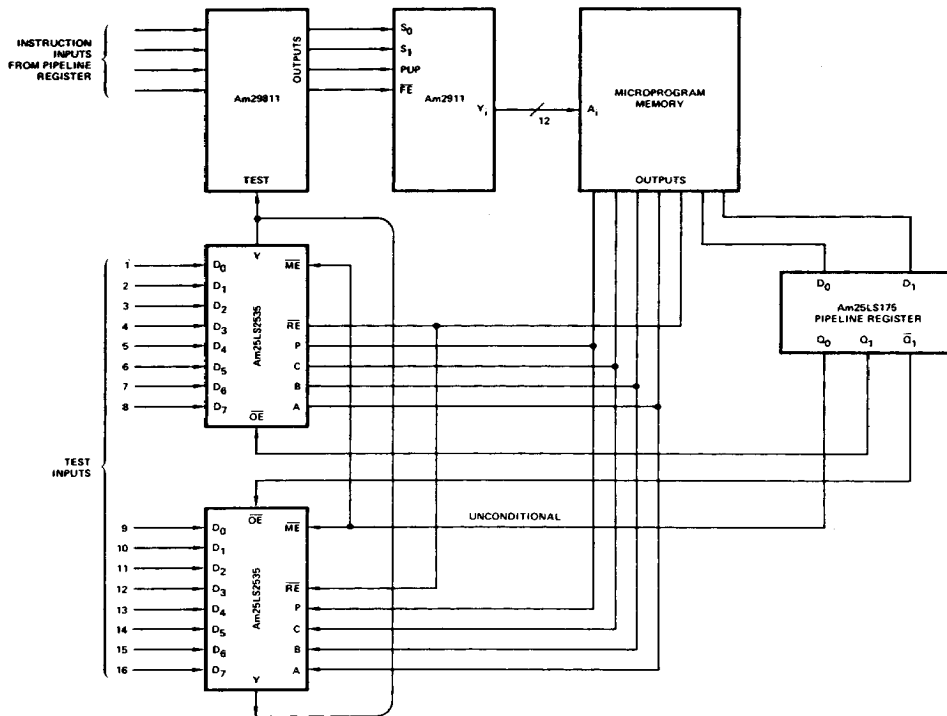
FUNCTION TABLE

MODE	INPUTS							INTERNAL				INPUTS		OUTPUT
	C	B	A	POL	RE	CLR	CP	Q _C	Q _B	Q _A	Q _{POL}	ME	OE	Y
Clear	X ↓	X ↓	X ↓	X ↓	X ↓	L ↓	X ↓	L ↓	L ↓	L ↓	L ↓	H L X	L L H	H D ₀ Z
Reg. Disable	X	X	X	X	H	H	X	NC	NC	NC	NC	L	L	D _i /D _i (Note 1)
Select (Multiplex)	L L L L H H H H	L L H H L L H H	L H L L H L H H	L/H ↓	L ↓	H ↓	I ↓	L L L L H H H H	L L H H L L H H	L H L L H L H H	L/H ↓	L ↓	L ↓	D ₀ /D ₀ D ₁ /D ₁ D ₂ /D ₂ D ₃ /D ₃ D ₄ /D ₄ D ₅ /D ₅ D ₆ /D ₆ D ₇ /D ₇
Multiplexer Disable	X ↓	X ↓	X ↓	X ↓	X ↓	H ↓	X ↓	X X	X X	X X	L H	H H	L L	H L
Tri-state Output Disable	↓	↓	↓	↓	↓	↓	↓	X	X	X	X	X	H	Z

NC = No Change
X = Don't Care

Note 1: The output will follow the selected input, D_i, or its complement depending on the state of the POL flip-flop.

APPLICATION



AF001980

A versatile one-of-sixteen Test Select with Polarity Control and Test Select Hold.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65°C to +150°C
 (Ambient) Temperature Under Bias -55°C to +125°C
 Supply Voltage to Ground Potential
 Continuous -0.5V to +7.0V
 DC Voltage Applied to Outputs For
 High Output State -0.5V to +V_{CC} max
 DC Input Voltage -0.5V to +5.5V
 DC Output Current, Into Outputs 30mA
 DC Input Current -30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature 0°C to +70°C
 Supply Voltage +4.75V to +5.25V

Military (M) Devices

Temperature -55°C to +125°C
 Supply Voltage +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V _{OH}	Output HIGH Voltage	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	MIL, I _{OH} = -2.0mA COM'L, I _{OH} = -6.5mA	2.4	3.4		Volts
V _{OL}	Output LOW Voltage	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	I _{OL} = 4.0 mA I _{OL} = 8.0mA I _{OL} = 20mA			0.4 0.45 0.5	Volts
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.				0.7 0.8	Volts
V _I	Input Clamp Voltage	V _{CC} = MIN, I _{IN} = -18mA				-1.5	Volts
I _{IL}	Input LOW Current	V _{CC} = MAX V _{IN} = 0.4V	ME, OE, RE D _N , A, B, C, POL, CP, CLR			-0.72 -2.0	mA
I _{IH}	Input HIGH Current	V _{CC} = MAX V _{IN} = 2.7V	ME, OE, RE D _N , A, B, C, POL, CP, CLR			40 50	μA
I _I	Input HIGH Current	V _{CC} = MAX V _{IN} = 5.5V	ME, OE, RE D _N , A, B, C, POL, CP, CLR			0.1 1.0	mA
I _{OZ}	Off-State (High-Impedance) Output Current	V _{CC} = MAX	V _O = 0.4V V _O = 2.4V			-50 50	μA
I _{SC}	Output Short Circuit Current (Note 3)	V _{CC} = MAX		-40		-100	mA
I _{CC}	Power Supply Current (Note 4)	V _{CC} = MAX			97	148	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.

3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

4. D₁-D₇, A, B, C, POL, ME, CLR at GND. All other inputs and outputs open.

Measured after a momentary ground then 4.5 V applied to clock input.

SWITCHING CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)

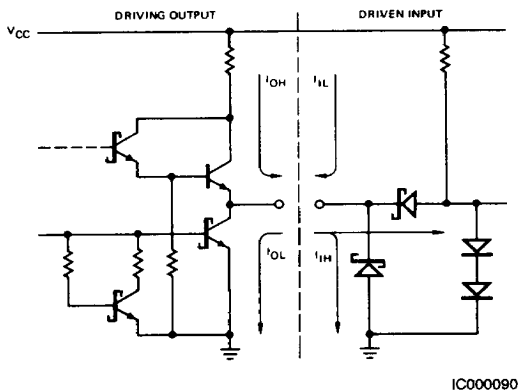
Parameters	Description	Test Conditions	Min	Typ	Max	Units
tPLH	Clock to Y POL - LOW	CL = 15pF RL = 2.0kΩ		21	32	ns
tPHL				19	29	
tPLH	Clock to Y POL - HIGH			16	24	ns
tPHL				19	29	
tPLH	Dn to Y			10	16	ns
tPHL				13	19	
tPLH	CLR to Y			22	33	ns
tPHL				22	33	
tPLH	ME to Y			12	18	ns
tPHL				12	18	
tZL	OE to Y			8	14	ns
tZH				8	14	
tLZ		CL = 5.0pF RL = 2.0kΩ		10	17	ns
tHZ				10	17	
ts	A, B, C, POL	CL = 15pF RL = 2.0kΩ	10			ns
	RE		15			
ts	CLR Recovery		5			ns
tpw	Clock		10			ns
	Clear (LOW)		10			
th	A, B, C, POL, RE			0		

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL		MILITARY		Units
			Am25LS2535		Am25LS2535		
			Min	Max	Min	Max	
tPLH	Clock to Y, POL-L	CL = 50pF RL = 2.0kΩ		40		47	ns
tPHL				34		38	
tPLH	Clock to Y, POL-H			29		33	
tPHL				35		41	
tPLH	DN to Y			19		21	ns
tPHL				22		24	
tPLH	CLR to Y			39		45	ns
tPHL				39		45	
tPLH	ME to Y			22		26	ns
tPHL				19		20	
tZL	OE to Y			19		24	ns
tZH				22		29	
tLZ	OE to Y	CL = 5.0pF RL = 2.0kΩ		24		30	ns
tHZ				24		30	
ts	A, B, C POL	CL = 50pF RL = 2.0kΩ	11		12		ns
	RE		18		20		
ts	CLR Recovery		6		7		ns
tpw	Clock		11		12		ns
	Clear (LOW)		11		12		
th	A, B, C, POL, RE			3		3	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS2535 **LOW-POWER SCHOTTKY INPUT/OUTPUT** **CURRENT INTERFACE CONDITIONS**



Note: Actual current flow direction shown.

RELATED PRODUCTS

Part No.	Description
Am2922	8 Input Multiplexer
Am2923	8 Input Multiplexer