

N-channel 800 V, 2.8 Ω typ., 2 A MDmesh™ K5 Power MOSFET in a PowerFLAT™ 5x6 VHV package

Datasheet - production data

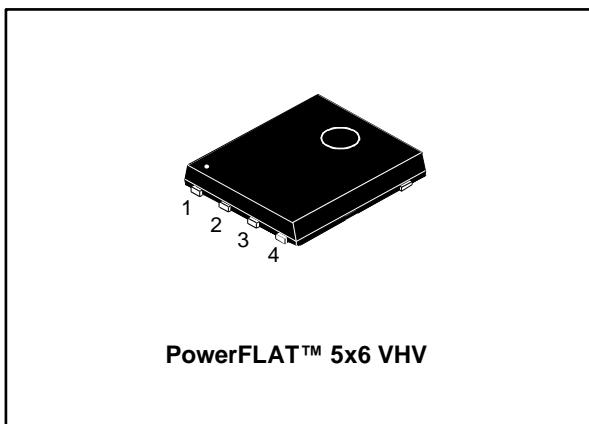
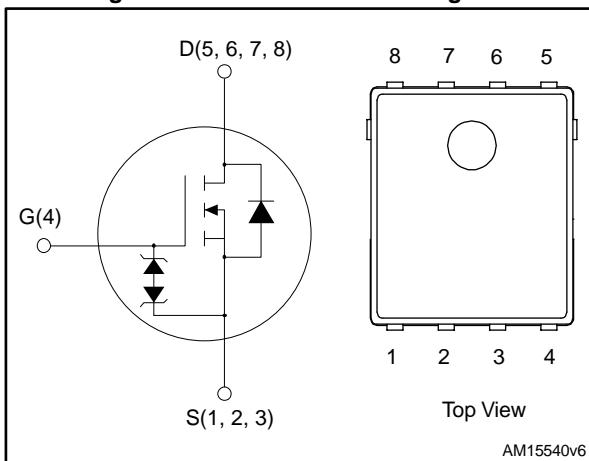


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STL3N80K5	800 V	3.5 Ω	2 A	38 W

- Industry's lowest R_{DS(on)} x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STL3N80K5	3N80K5	PowerFLAT™ 5x6 VHV	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	2	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	1.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	8	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	38	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_j	Operating junction temperature range	- 55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature range		

Notes:

(1) Pulse width limited by safe operating area.

(2) $I_{SD} \leq 2$ A, $di/dt = 100$ A/ μs ; V_{DS} peak $< V_{(BR)DSS}$ (3) $V_{DS} \leq 640$ V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	3.3	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	59	$^\circ\text{C}/\text{W}$

Notes:(1) When mounted on FR-4 board of 1 inch², 2 oz Cu

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50$ V)	65	mJ

2 Electrical characteristics

$T_c = 25^\circ\text{C}$ unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0 \text{ V}$, $I_D = 1 \text{ mA}$	800			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0 \text{ V}$, $V_{\text{DS}} = 800 \text{ V}$			1	μA
		$V_{\text{GS}} = 0 \text{ V}$, $V_{\text{DS}} = 800 \text{ V}$ $T_c = 125^\circ\text{C}$ ⁽¹⁾			50	μA
I_{GSS}	Gate body leakage current	$V_{\text{DS}} = 0 \text{ V}$, $V_{\text{GS}} = \pm 20 \text{ V}$			± 10	μA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 100 \mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10 \text{ V}$, $I_D = 1 \text{ A}$		2.8	3.5	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 100 \text{ V}$, $f = 1 \text{ MHz}$, $V_{\text{GS}} = 0 \text{ V}$	-	130	-	pF
C_{oss}	Output capacitance		-	14	-	pF
C_{rss}	Reverse transfer capacitance		-	0.6	-	pF
$C_{\text{o(tr)}}^{(1)}$	Equivalent capacitance time related	$V_{\text{DS}} = 0 \text{ to } 640 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$	-	20	-	pF
$C_{\text{o(er)}}^{(2)}$	Equivalent capacitance energy related		-	9	-	pF
R_g	Intrinsic gate resistance	$f = 1 \text{ MHz}$, $I_D = 0 \text{ A}$	-	15.5	-	Ω
Q_g	Total gate charge	$V_{\text{DD}} = 640 \text{ V}$, $I_D = 2.5 \text{ A}$ $V_{\text{GS}} = 0 \text{ to } 10 \text{ V}$ (see Figure 15: "Test circuit for gate charge behavior")	-	9.5	-	nC
Q_{gs}	Gate-source charge		-	1.5	-	nC
Q_{gd}	Gate-drain charge		-	7.5	-	nC

Notes:

⁽¹⁾Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400 \text{ V}$, $I_D = 1.25 \text{ A}$, $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	8.5	-	ns
t_r	Rise time		-	7.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	20.5	-	ns
t_f	Fall time		-	25	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		8	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 2 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	265		ns
Q_{rr}	Reverse recovery charge		-	1.2		μC
I_{RRM}	Reverse recovery current		-	9.2		A
t_{rr}	Reverse recovery time	$I_{SD} = 2 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	430		ns
Q_{rr}	Reverse recovery charge		-	1.9		μC
I_{RRM}	Reverse recovery current		-	8.8		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0 \text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

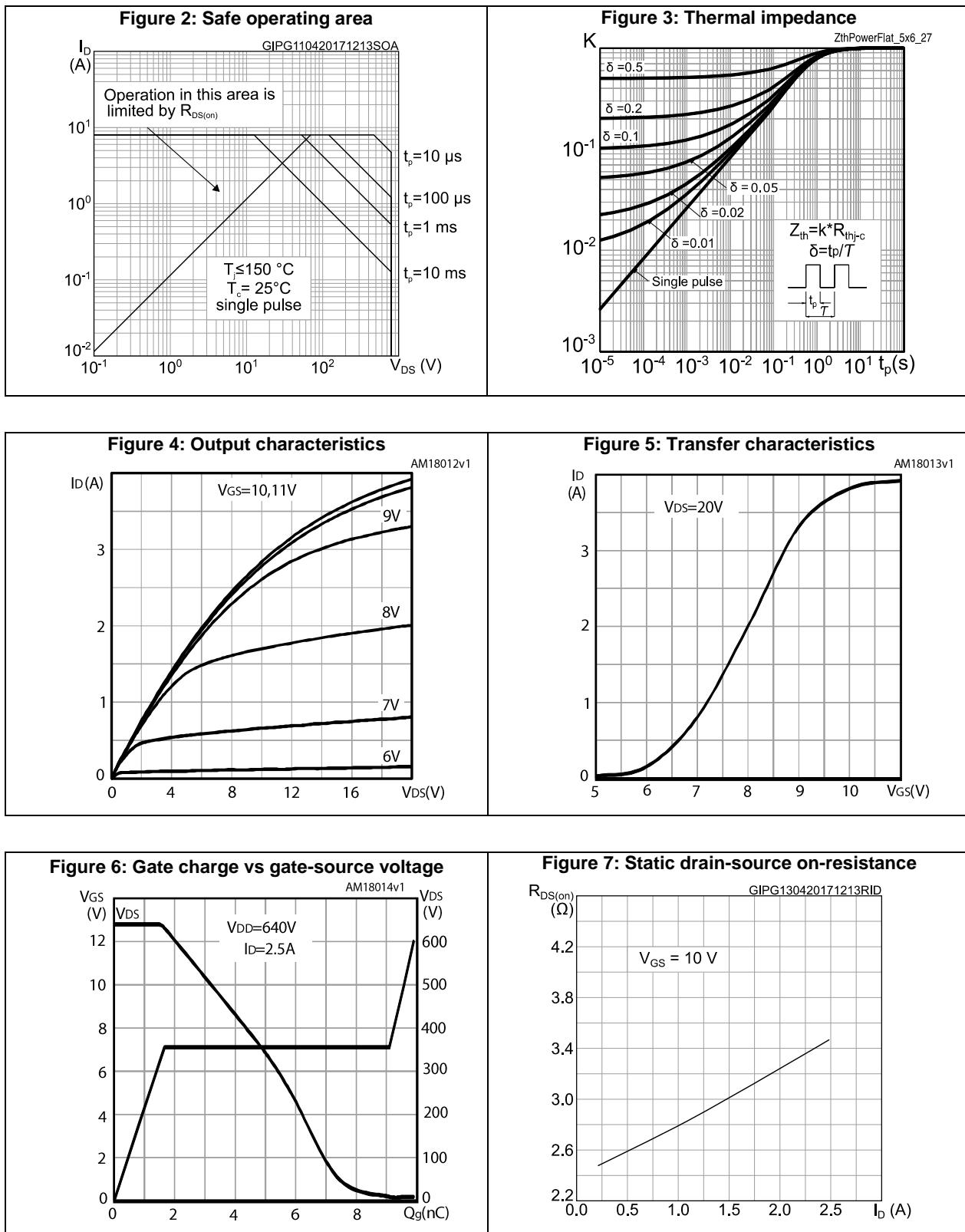


Figure 8: Capacitance variations

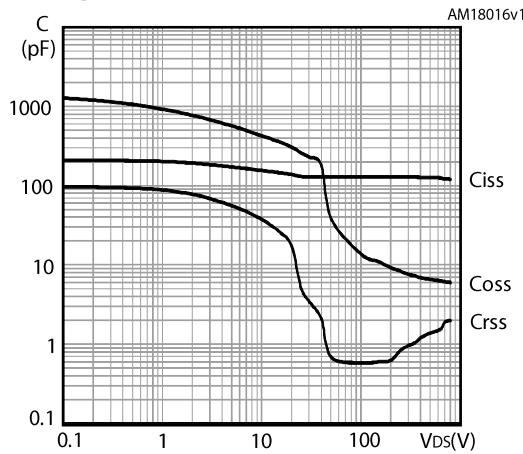


Figure 9: Output capacitance stored energy

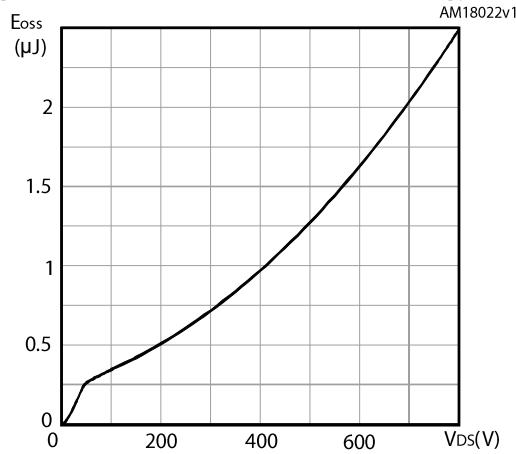


Figure 10: Normalized gate threshold voltage vs temperature

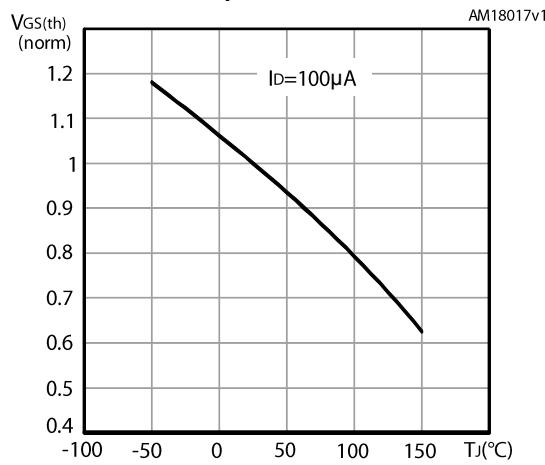


Figure 11: Normalized on-resistance vs temperature

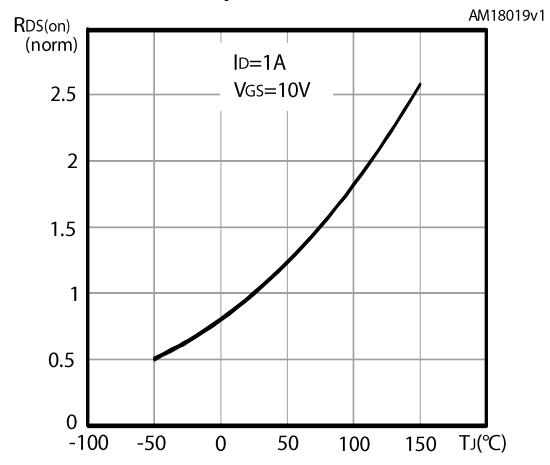
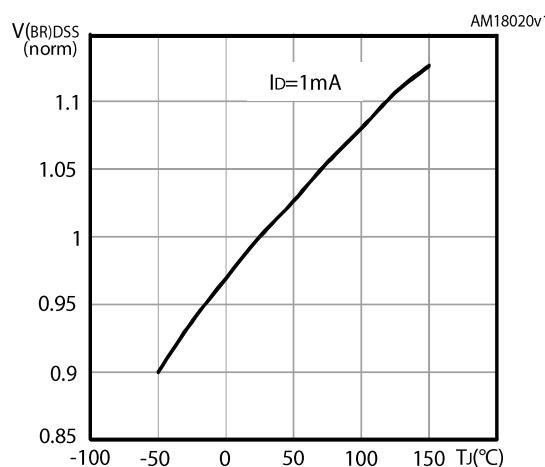
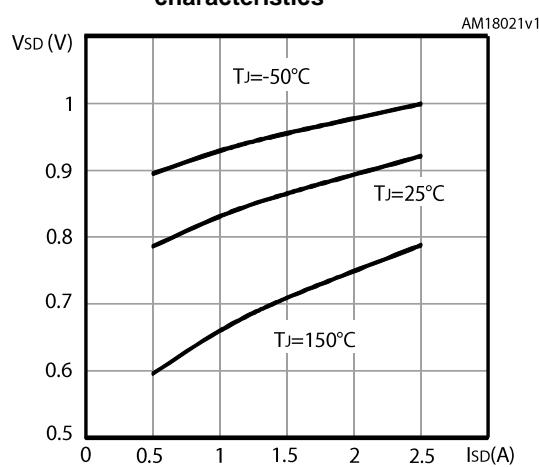
Figure 12: Normalized $V_{(BR)DSS}$ vs temperature

Figure 13: Source-drain diode forward characteristics



3 Test circuits

Figure 14: Test circuit for resistive load switching times

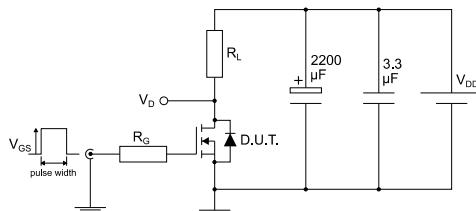
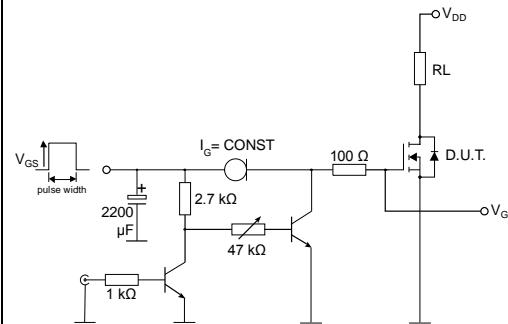


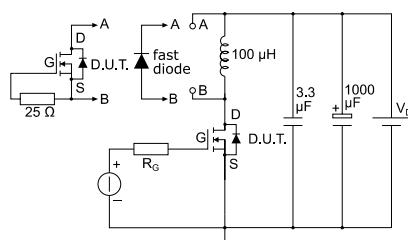
Figure 15: Test circuit for gate charge behavior



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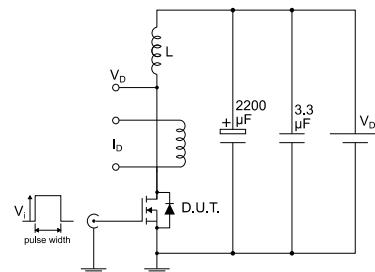
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Figure 16: Test circuit for inductive load switching and diode recovery times



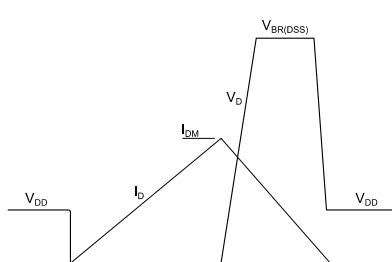
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Figure 17: Unclamped inductive load test circuit



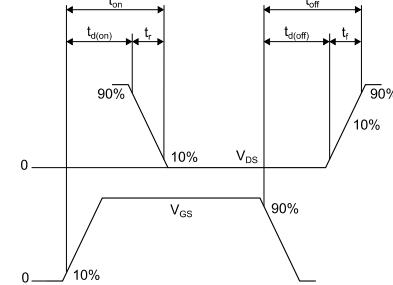
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Figure 18: Unclamped inductive waveform



AM01472v1

Figure 19: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 VHV package information

Figure 20: PowerFLAT™ 5x6 VHV package outline

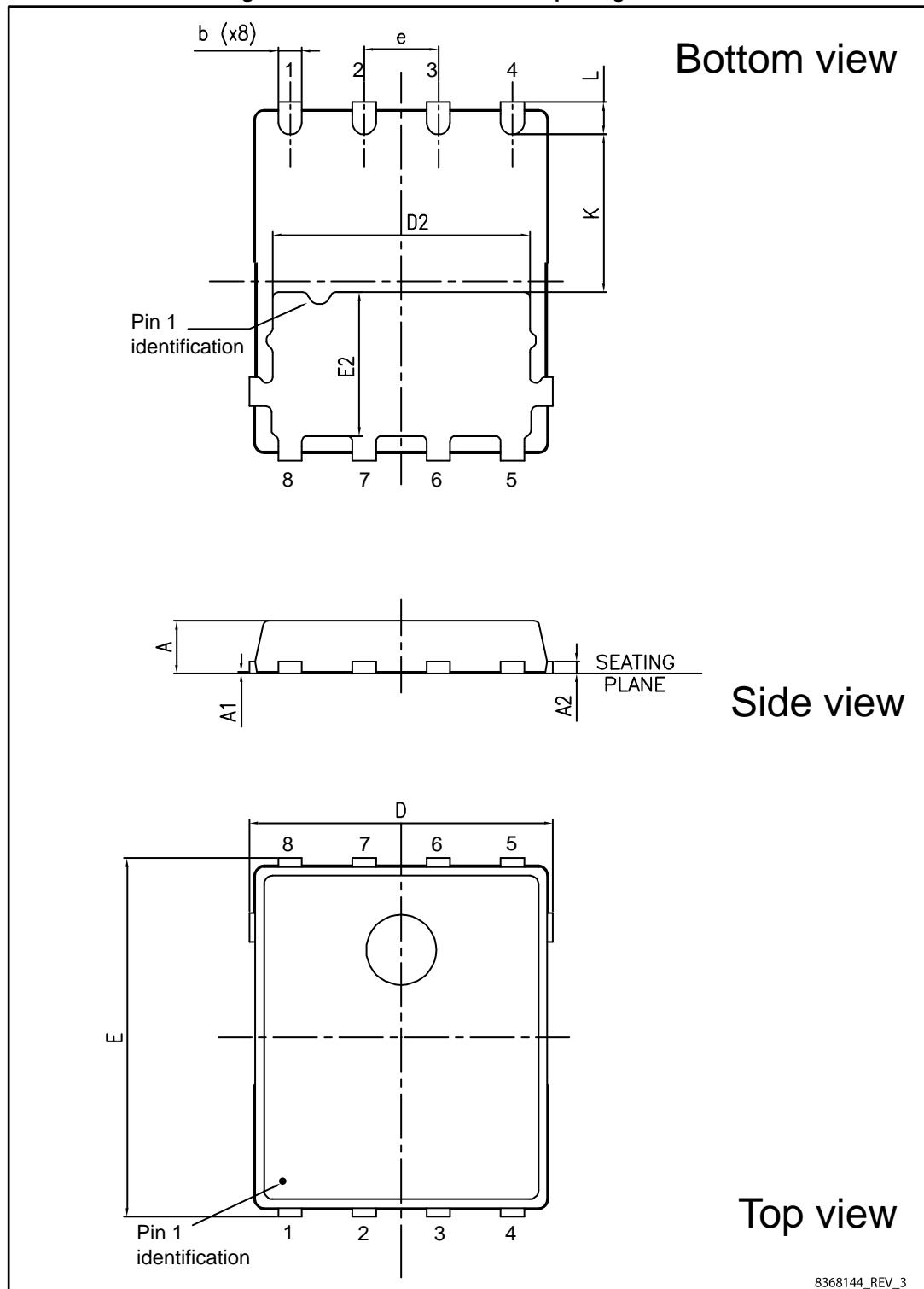
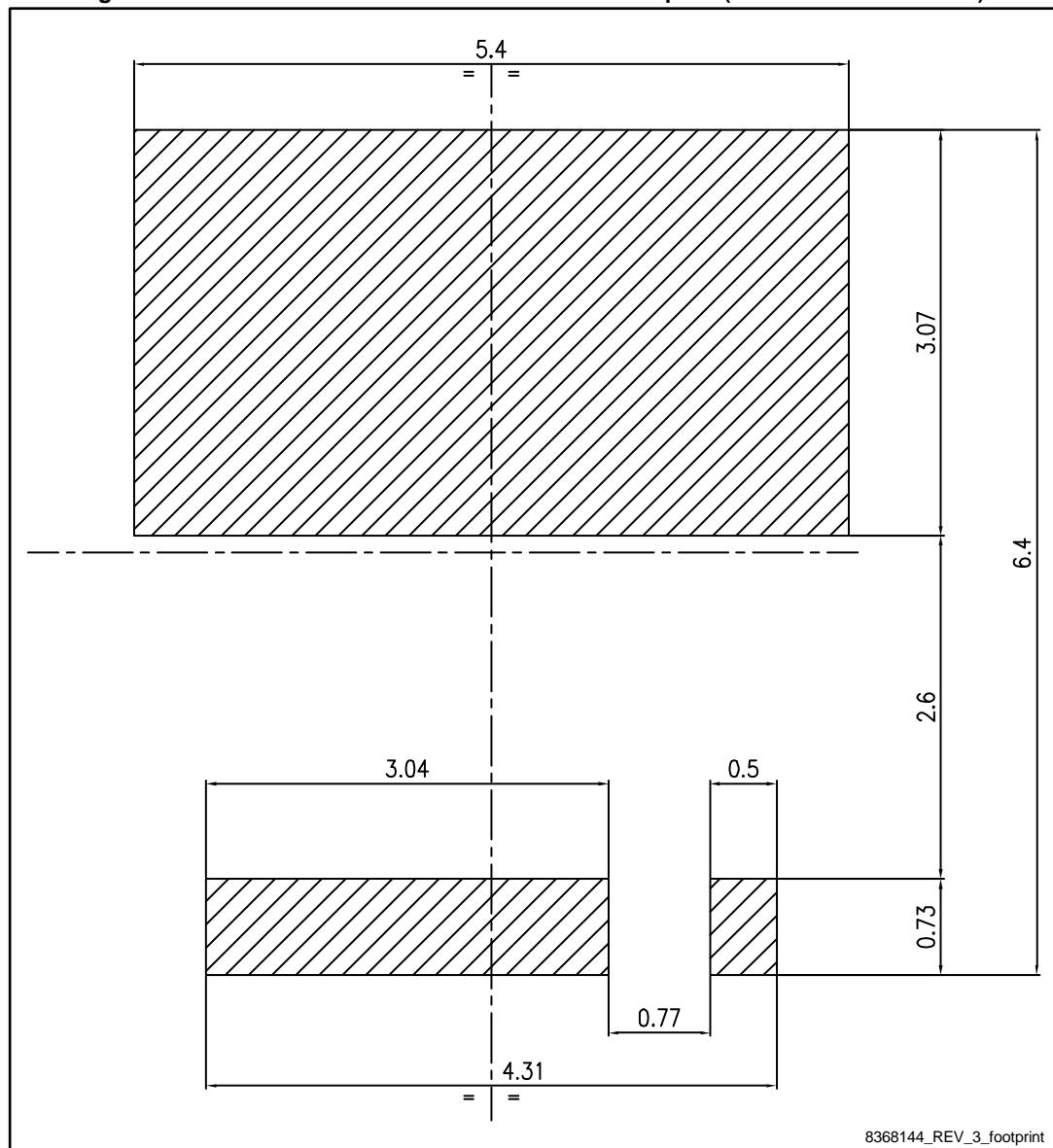


Table 10: PowerFLAT™ 5x6 VHV package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.30	4.40	4.50
E2	2.40	2.50	2.60
e		1.27	
L	0.50	0.55	0.60
K	2.60	2.70	2.80

Figure 21: PowerFLAT™ 5x6 VHV recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 VHV packing information

Figure 22: PowerFLAT™ 5x6 tape (dimensions are in mm)

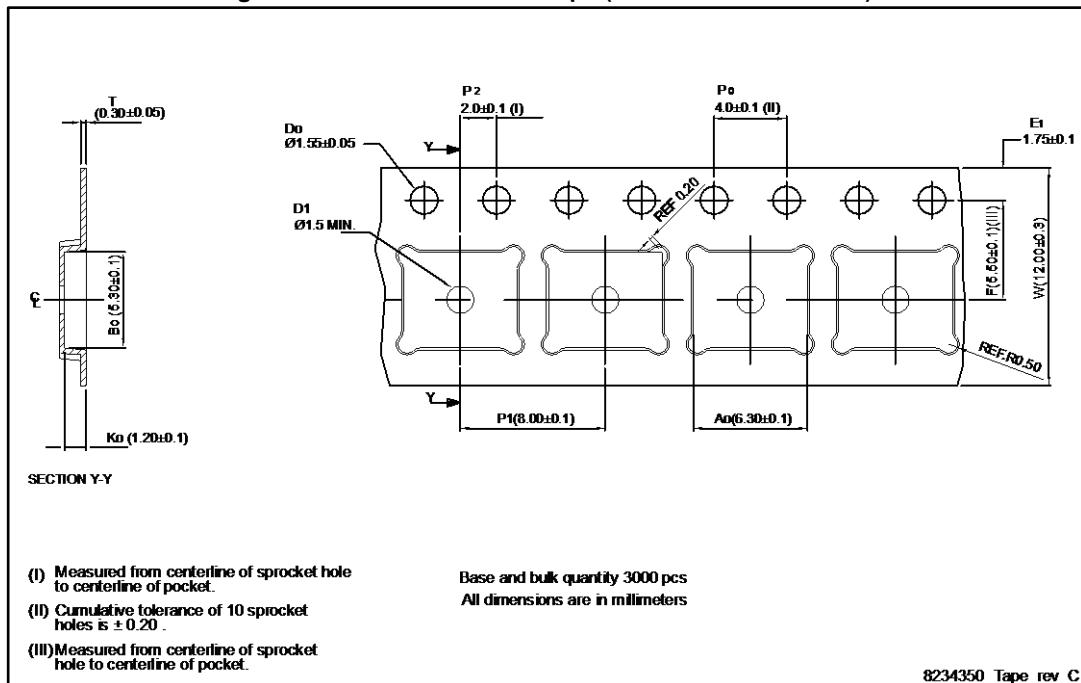


Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape

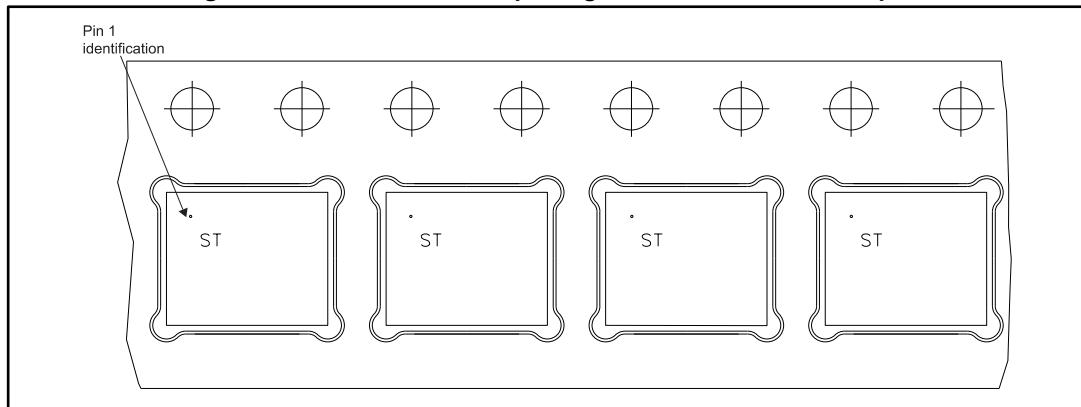
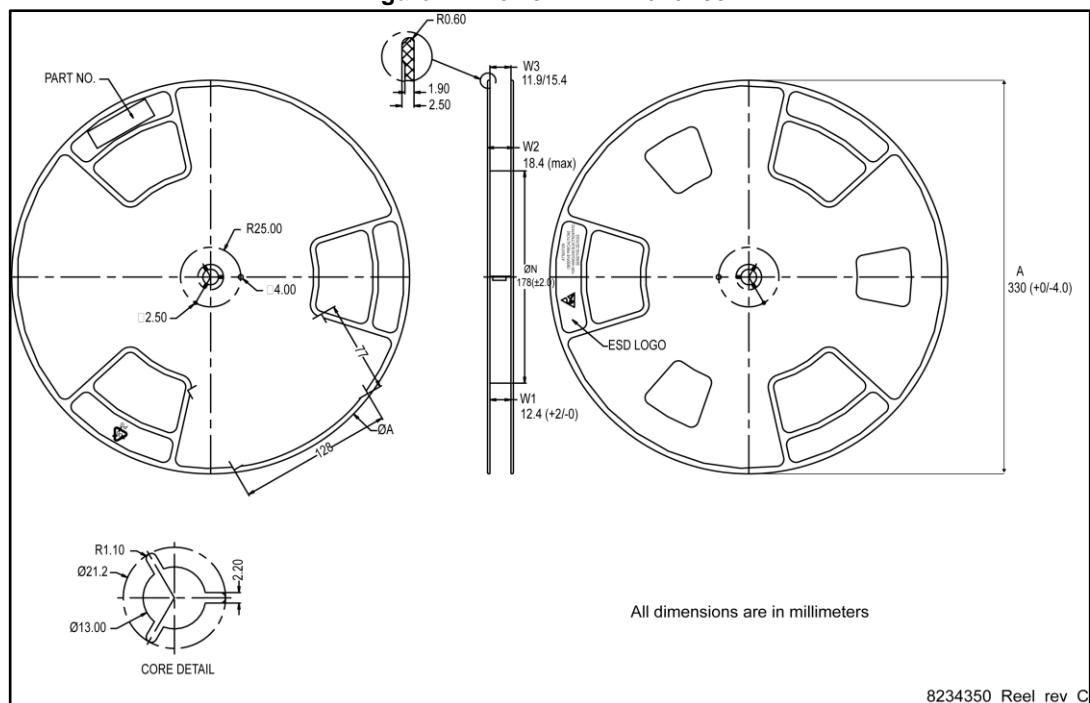


Figure 24: PowerFLAT™ 5x6 reel



5 Revision history

Table 11: Document revision history

Date	Revision	Changes
10-Apr-2017	1	First release.

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