FEMTOCLOCKS™ CRYSTAL-TO-LVPECL 100MHZ FREQUENCY MARGINING SYNTHESIZER

ICS843101I-100

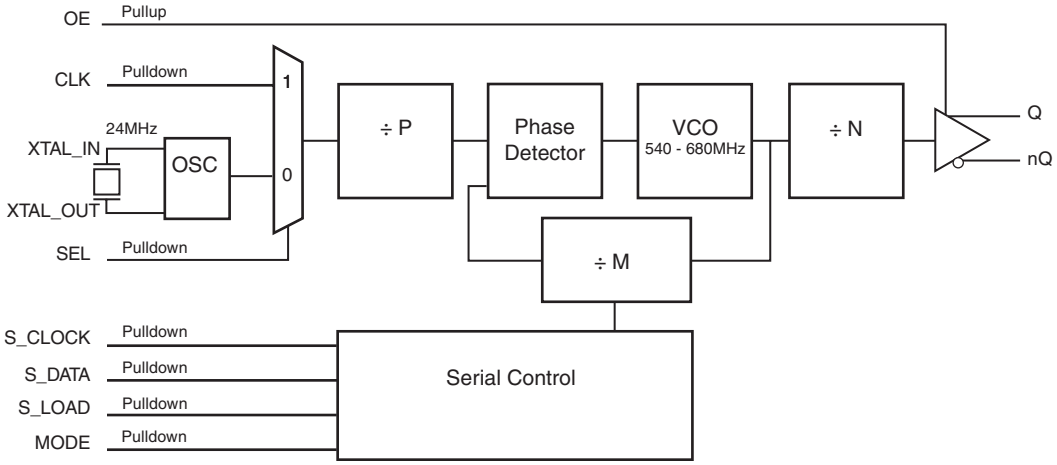
General Description

The ICS843101I-100 is a low phase-noise frequency margining synthesizer and is a member of the HiPerClockS™family of high performance clock solutions from IDT. In the default mode, the device nominally generates a 100MHz LVPECL output clock signal from a 24MHz crystal input. There is also a frequency margining mode available where the device can be programmed, using the serial interface, to vary the output frequency up or down from nominal in 2% steps. The ICS843101I-100 is provided in a 16-pin TSSOP.

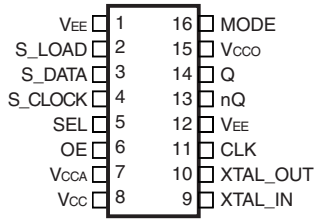
Features

- 100MHz nominal LVPECL output
- Selectable crystal oscillator interface designed for 24MHz, 18pF parallel resonant crystal or LVCMOS/LVTTL single-ended input
- Output frequency can be varied ±10% from nominal in 2% steps
- VCO range: 540MHz - 680MHz
- RMS phase jitter @ 100MHz, using a 24MHz crystal (1.875MHz - 20MHz): 0.55ps (typical)
- Output supply modes
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS-6) packages

Block Diagram



Pin Assignment



ICS843101I-100
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm
package body
G Package
Top View

Functional Description

The ICS843101I-100 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A 24MHz fundamental crystal is used as the input to the on chip oscillator. The output of the oscillator is fed into the pre-divider. In frequency margining mode, the 24MHz crystal frequency is divided by 2 and a 12MHz reference frequency is applied to the phase detector. The VCO of the PLL operates over a range of 540MHz to 680MHz. The output of the M divider is also applied to the phase detector.

The default mode for the ICS843101I-100 is 100MHz output frequency using a 24MHz crystal. The output frequency can be changed by placing the device into the margining mode using the mode pin and using the serial interface to program the M feedback divider. Frequency margining mode operation occurs when the MODE input is HIGH. The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by an output divider prior to being sent to the LVPECL output buffer. The divider provides a 50% output duty cycle. The relationship between the crystal input frequency, the M divider, the VCO frequency and the output frequency is provided in Table 1. When changing back from frequency margining mode to nominal mode, the device will return to the default nominal configuration that will provide 100MHz output frequency.

Serial operation occurs when S_LOAD is HIGH. Serial data can be loaded in either the default mode or the frequency margining mode. The 6-bit shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. After shifting in the 6-bit M divider value, S_LOAD is transitioned from HIGH to LOW which latches the contents of the shift-register into the M divider control register. When S_LOAD is LOW, any transitions of S_CLOCK or S_DATA are ignored.

Table 1. Frequency Margin Function Table

XTAL (MHz)	Pre-Divider (P)	Reference Frequency (MHz)	Feedback Divider (M)	M-Data (Binary)	VCO (MHz)	Output Divider (N)	Output Frequency (MHz)	% Change
24	2	12	45	101101	540	6	90	-10.0
24	2	12	46	101110	552	6	92	-8.0
24	2	12	47	101111	564	6	94	-6.0
24	2	12	48	110000	576	6	96	-4.0
24	2	12	49	110001	588	6	98	-2.0
24	2	12	50	110010	600	6	100	Nominal Mode
24	2	12	51	110011	612	6	102	2.0
24	2	12	52	110100	624	6	104	4.0
24	2	12	53	110101	636	6	106	6.0
24	2	12	54	110110	648	6	108	8.0
24	2	12	55	110111	660	6	110	10.0

Serial Loading

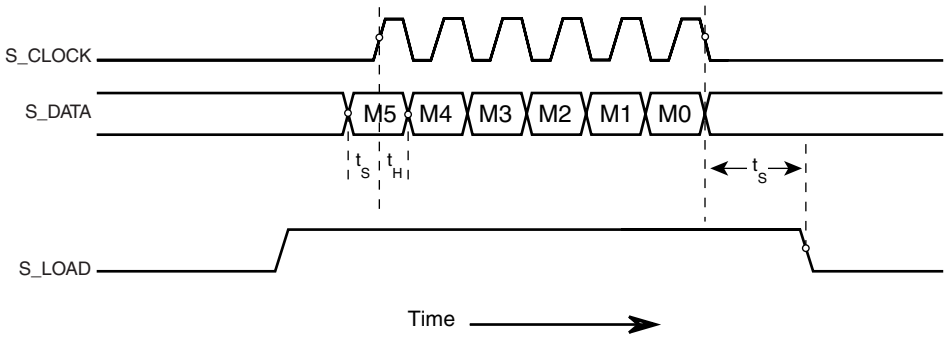


Figure 1. Serial Load Operations

TABLE 2. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 12	V_{EE}	Power		Negative supply pins.
2	S_LOAD	Input	Pulldown	Controls the operation of the Serial input. LVCMOS/LVTTL interface levels. See Table 4D.
3	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels. See Table 4D.
4	S_CLOCK	Input	Pulldown	Clock in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels. See Table 4D.
5	SEL	Input	Pulldown	Select pin. When HIGH, selects CLK input. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels. See Table 4B.
6	OE	Input	Pullup	Output enable pin. Controls enabling and disabling of Q/nQ outputs. LVCMOS/LVTTL interface levels. See Table 4A.
7	V_{CCA}	Power		Analog supply pin.
8	V_{CC}	Power		Core supply pin.
9, 10	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
11	CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
13, 14	nQ, Q	Ouput		Differential output pair. LVPECL interface levels.
15	V_{CCO}	Power		Output supply pin.
16	MODE	Input	Pulldown	MODE pin. LVCMOS/LVTTL interface levels. See Table 4C.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 3. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pulldown Resistor			51		kΩ

TABLE 4A. OE CONTROL INPUT FUNCTION TABLE

Input	Outputs
OE	**Q, nQ**
0	HiZ
1	Enabled

TABLE 4B. SEL CONTROL INPUT FUNCTION TABLE

Input	
SEL	**Selected Source**
0	XTAL_IN, XTAL_OUT
1	CLK

TABLE 4C. MODE CONTROL INPUT FUNCTION TABLE

Input	Condition
Mode	**Q, nQ**
0	Default Mode
1	Frequency Margining Mode

TABLE 4D. SERIAL MODE FUNCTION TABLE

Inputs			Conditions
S_LOAD	**S_CLOCK**	**S_DATA**	
L	X	X	Serial inputs are ignored.
H	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
↓	L	X	Contents of the shift register are latched.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	89°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 5A. Power Supply DC Characteristics, V_{CC} = V_{CCO} = 3.3V±5%, , V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.10	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				115	mA
I_{CC}	Core Supply Current				100	mA
I_{CCA}	Analog Supply Current				10	mA
I_{CCO}	Output Supply Current				8	mA

Table 5B. Power Supply DC Characteristics, V_{CC} = 3.3V±5%,V_{CCO} = 2.5V±5%, , V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.10	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				115	mA
I_{CC}	Core Supply Current				100	mA
I_{CCA}	Analog Supply Current				10	mA
I_{CCO}	Output Supply Current				8	mA

Table 5C. Power Supply DC Characteristics, V_{CC} = V_{CCO} = 2.5V±5%, , V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.10	2.5	V_{CC}	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				110	mA
I_{CC}	Core Supply Current				100	mA
I_{CCA}	Analog Supply Current				10	mA
I_{CCO}	Output Supply Current				8	mA

TABLE 5D. LVCMOS / LVTTL DC CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK	V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
		SEL, OE, MODE, S_LOAD, S_CLOCK, S_DATA	V_{CC} = 3.3V	2.2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	CLK	V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
		SEL, OE, MODE, S_LOAD, S_CLOCK, S_DATA	V_{CC} = 3.3V	-0.3		1.1	V
			V_{CC} = 2.5V	-0.3		0.8	V
I_{IH}	Input High Current	CLK, SEL, S_LOAD, S_CLOCK, S_DATA, MODE	V_{CC} = V_{IN} = 3.465 or 2.625V			150	µA
		OE	V_{CC} = V_{IN} = 3.465 or 2.625V			5	µA
I_{IL}	Input Low Current	CLK, SEL, S_LOAD, S_CLOCK, S_DATA, MODE	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		OE	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
Δt/Δv	Input Transistion Rise/Fall Rate	SEL, OE, MODE, S_LOAD, S_CLOCK, S_DATA				20	ns/V

TABLE 5E. LVPECL DC CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 6. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			24		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				300	µW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 7. INPUT FREQUENCY CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK			24		MHz
		XTAL_IN/XTAL_OUT			24		MHz
		S_CLOCK				50	MHz

TABLE 8A. AC CHARACTERISTICS, V_{CC} = V_{CCO} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				100		MHz
*t*jit(Ø)	RMS Phase Jitter; NOTE 1		Mode = LOW 100MHz, (1.875MHz - 20MHz)		0.55		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	300		700	ps
odc	Output Duty Cycle			48		52	%
t_S	Setup Time	S_DATA to S_CLOCK		10			ns
		S_CLOCK to S_LOAD		10			ns
t_H	Hold Time	S_DATA to S_CLOCK		10			ns

NOTE 1: Characterized using a 24MHz crystal.

TABLE 8B. AC CHARACTERISTICS, V_{CC} = 3.3V±5%,V_{CCO} = 2.5V±5%, , V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				100		MHz
*t*jit(Ø)	RMS Phase Jitter; NOTE 1		Mode = LOW 100MHz, (1.875MHz - 20MHz)		0.54		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	300		700	ps
odc	Output Duty Cycle			48		52	%
t_S	Setup Time	S_DATA to S_CLOCK		10			ns
		S_CLOCK to S_LOAD		10			ns
t_H	Hold Time	S_DATA to S_CLOCK		10			ns

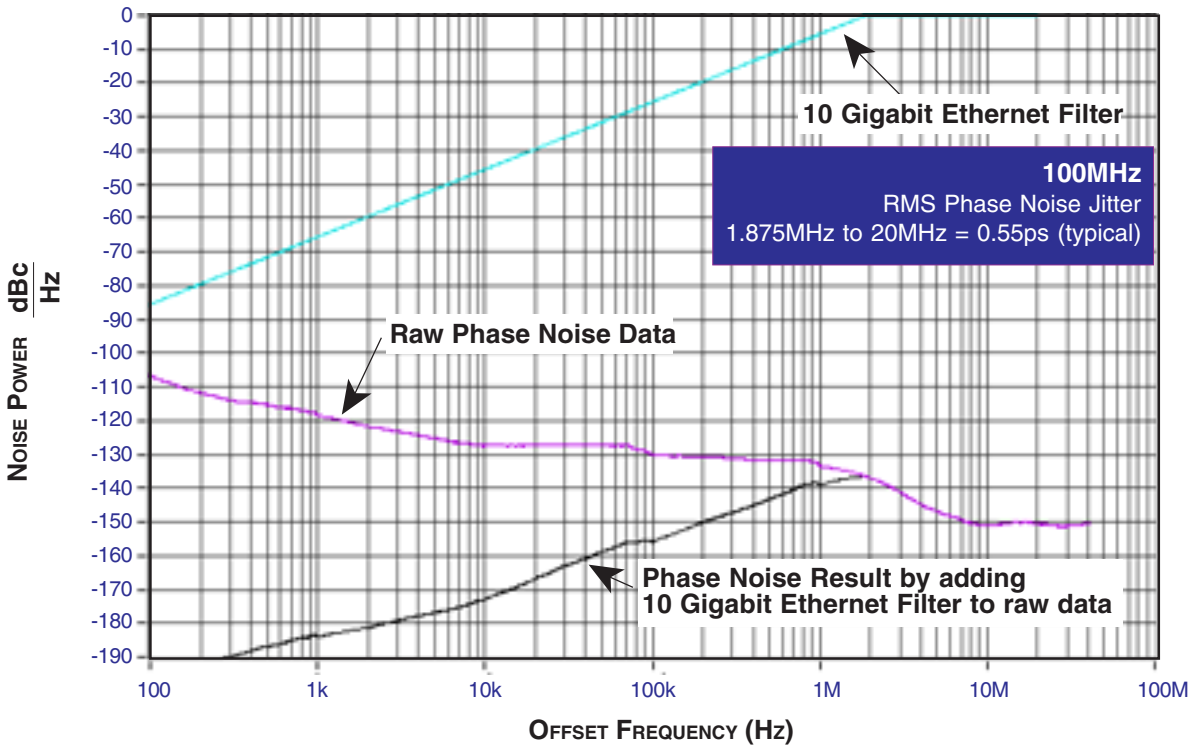
NOTE 1: Characterized using a 24MHz crystal.

TABLE 8C. AC CHARACTERISTICS, V_{CC} = V_{CCO} = 2.5V±5%, , V_{EE} = 0V, T_A = -40°C TO 85°C

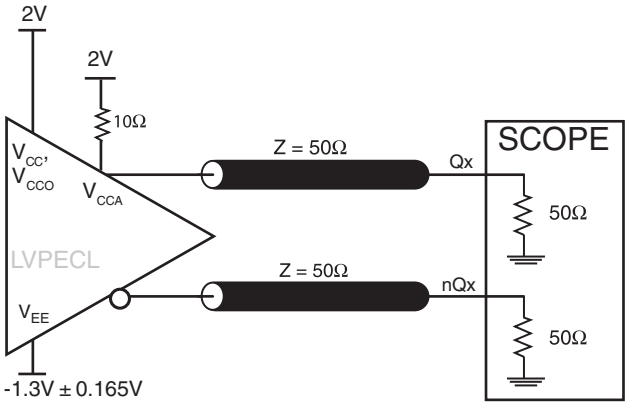
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				100		MHz
*t*jit(Ø)	RMS Phase Jitter; NOTE 1		Mode = LOW 100MHz, (1.875MHz - 20MHz)		0.54		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	300		700	ps
odc	Output Duty Cycle			48		52	%
t_S	Setup Time	S_DATA to S_CLOCK		10			ns
		S_CLOCK to S_LOAD		10			ns
t_H	Hold Time	S_DATA to S_CLOCK		10			ns

NOTE 1: Characterized using a 24MHz crystal.

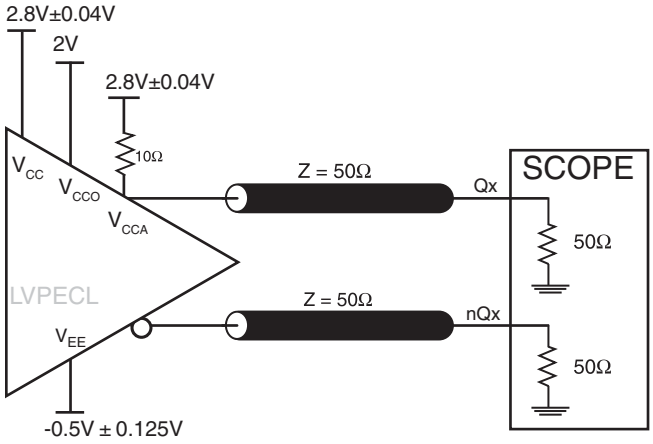
Typical Phase Noise at 100MHz (3.3V)



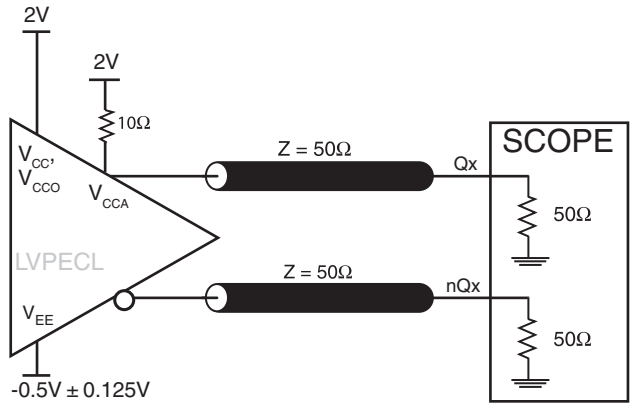
PARAMETER MEASUREMENT INFORMATION



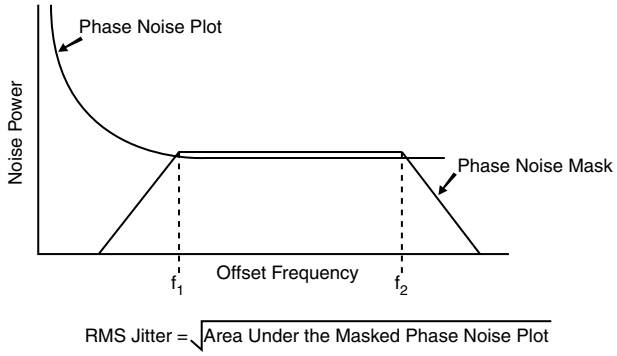
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



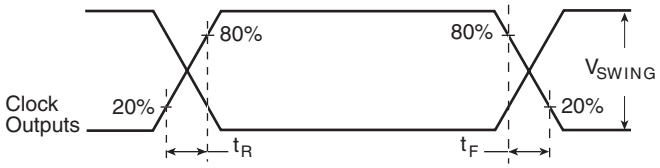
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



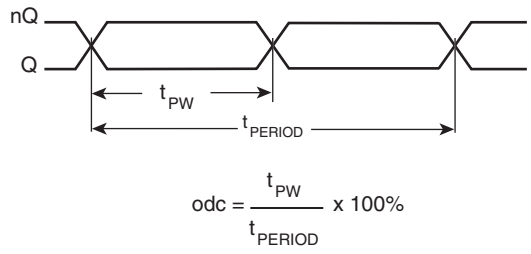
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



RMS PHASE JITTER



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843101I-100 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA}.

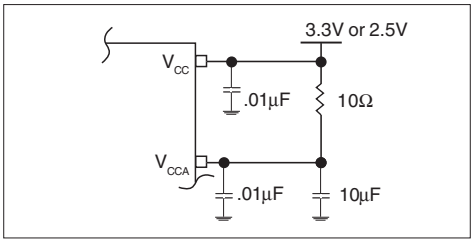


FIGURE 2. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843101I-100 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 3* below were determined using a 24MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

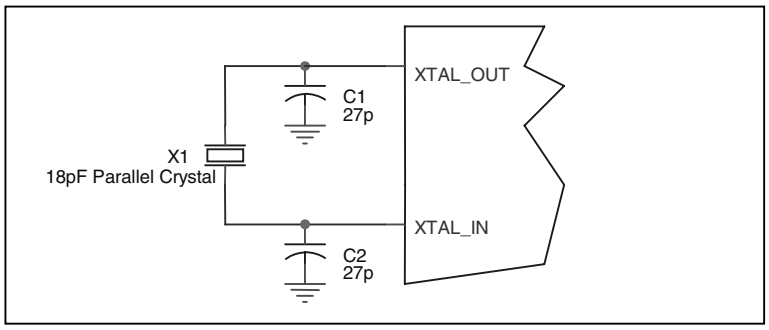


FIGURE 3. CRYSTAL INPUT INTERFACE

Recommendations for Unused Input Pins

Inputs:

Crystal Input:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK Input:
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Termination for 3.3V LVPECL Output

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

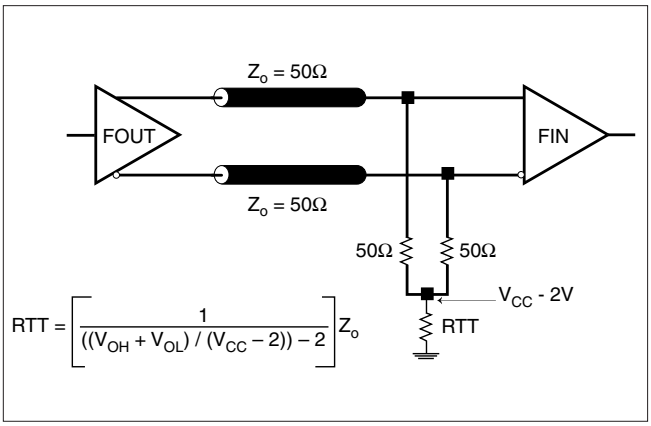


Figure 4A. LVPECL Output Termination

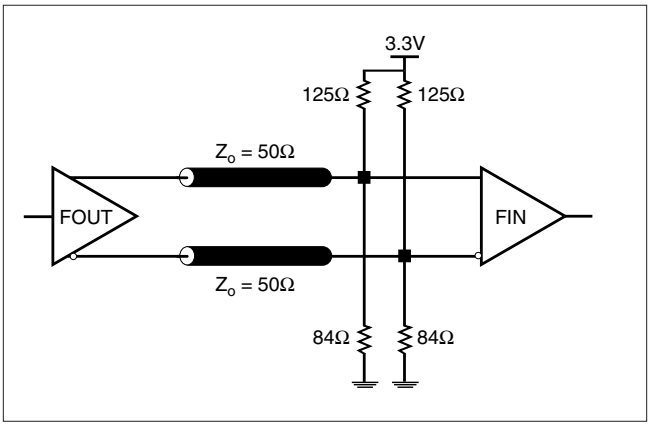


Figure 4B. LVPECL Output Termination

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

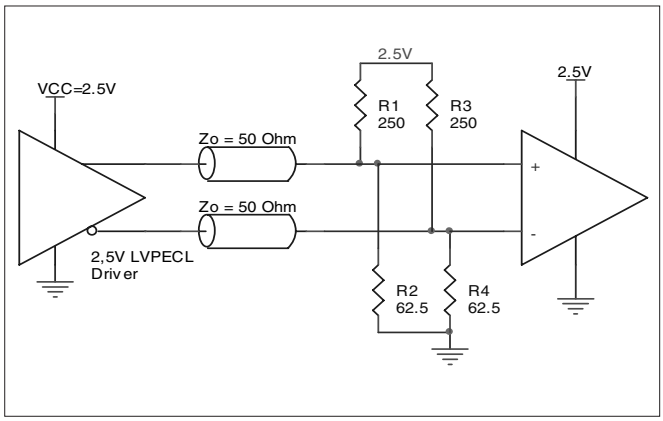


FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

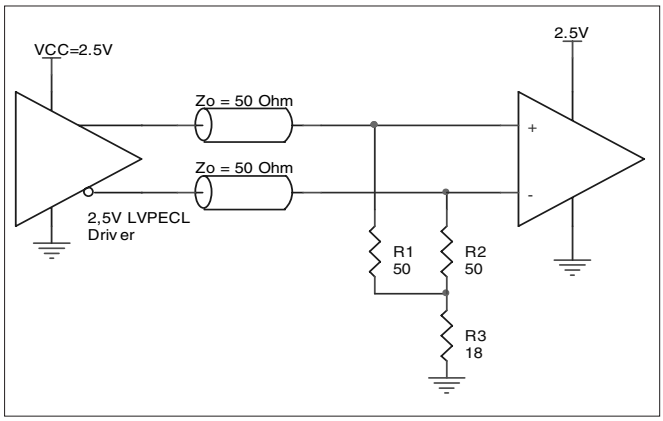


FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

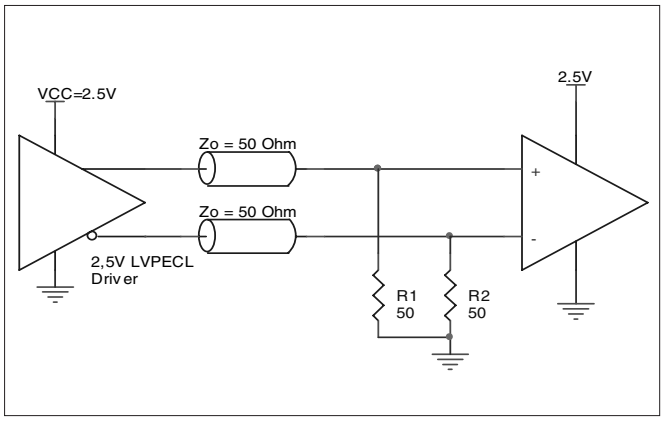


FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE

LAYOUT GUIDELINE

Figure 6 shows an example of ICS843101I-100 application schematic. In this example, the device is operated at V_{CC} = 3.3V. The 18pF parallel resonant 24MHz crystal is used. The C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVPECL terminations are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

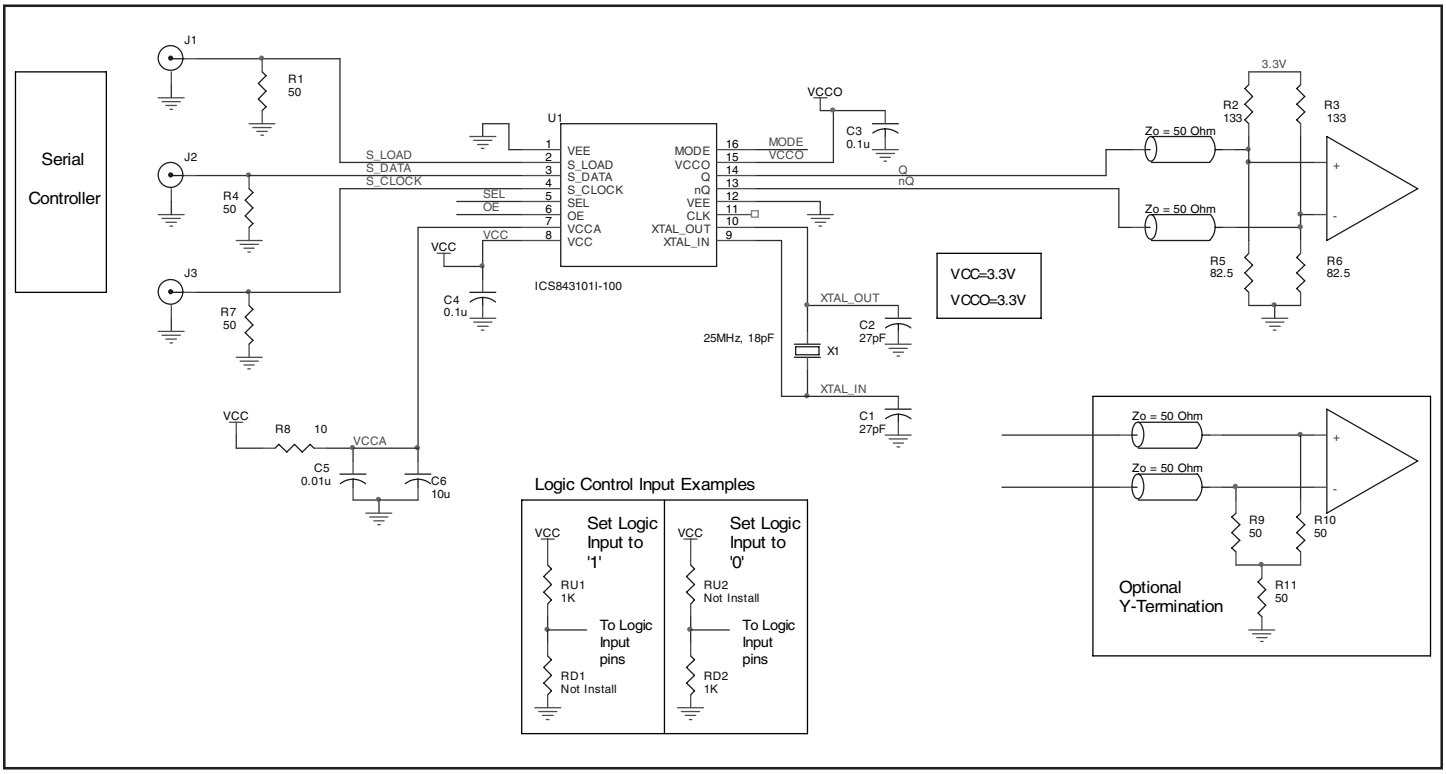


FIGURE 6. ICS843101I-100 SCHEMATIC EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843101I-100.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS843101I-100 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 115mA = **398.48mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

Total Power$_{_MAX}$ (3.63V, with all outputs switching) = 398.48mW + 30mW = **428.48mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 89°C/W per Table 9 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.429W *89°C/W = 123.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 9. THERMAL RESISTANCE θ_{JA} FOR 16-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

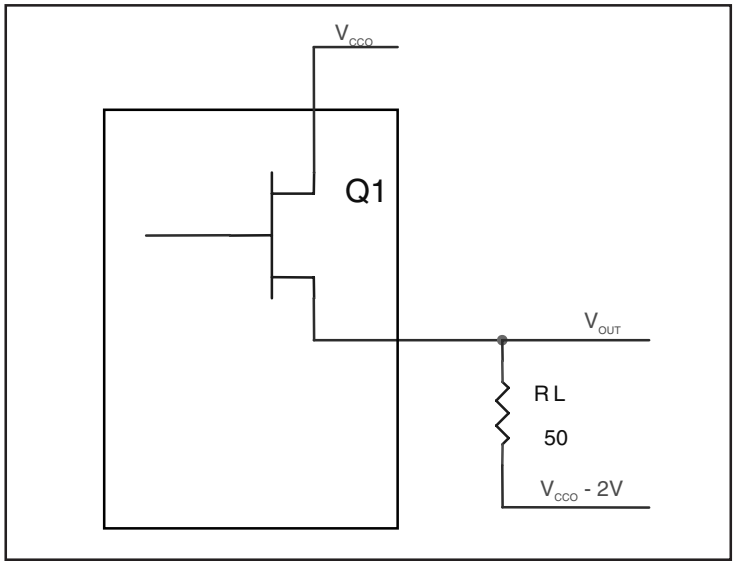


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 10. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

TRANSISTOR COUNT

The transistor count for ICS843101I-100 is: 4093

Package Outline - G Suffix for 16 Lead TSSOP

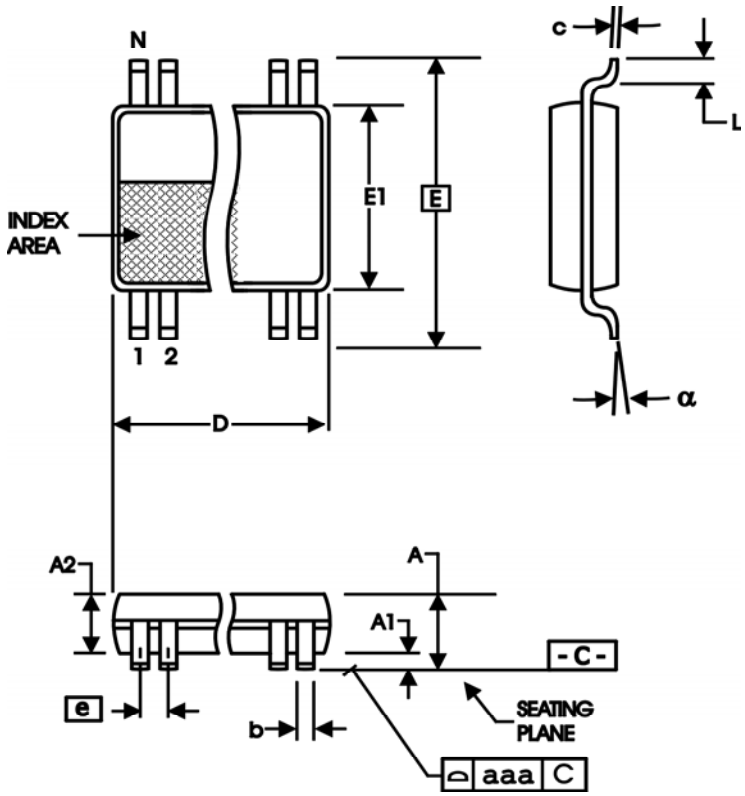


Table 11. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 12. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843101AGI-100	101AI100	16 Lead TSSOP	tube	-40°C to 85°C
ICS843101AGI100T	101AI100	16 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS843101AGI-100LF	01AI100L	16 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS843101AGI-100LFT	01AI100L	16 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS complaint.

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