

IXD611

600V, 600 mA High & Low-side Driver for N-Channel MOSFETs and IGBTs

Features

- Floating High Side Driver with boot-strap Power supply along with a Low Side Driver.
- Fully operational to 600V
- $\pm 50\text{V/ns}$ dV/dt immunity
- Gate drive power supply range: 10 - 35V
- Undervoltage lockout for both output drivers
- Outputs are in phase with inputs
- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up protected over entire operating range
- High peak output current: $\pm 600\text{ mA}$
- Matched propagation delay for both outputs
- Low output impedance
- Low power supply current
- Immune to negative voltage transients

Applications

- Driving MOSFETs and IGBTs in half-bridge circuits
- High voltage, high side and low side drivers
- Motor Controls
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Class D Switching Amplifiers

General Description

The IXD611, with its two inputs referenced to ground, has high speed low side and high side gate outputs to drive either a pair of N-channel MOSFETs or IGBTs in a half-bridge totem pole configuration. The High Side driver can control a MOSFET or IGBT connected to a positive high voltage up to 600V. The logic input stages are compatible with TTL or CMOS, have built-in hysteresis and are fully immune to latch up over the entire operating range. The IXD611 can withstand dV/dt on the output side up to $\pm 50\text{V/ns}$.

The IXD611 comes in either the 8-PIN PDIP (IXD611P1), 8-PIN SOIC (IXD611S1), 14-PIN PDIP (IXD611P7), or the 14-PIN SOIC (IXD611S7) packages.

Ordering Information

Part Number	Package Type
IXD611P1	8-PIN DIP
IXD611P7	14-PIN DIP
IXD611S1	8-PIN SOIC
IXD611S7	14-PIN SOIC

Warning: The IXD611 is ESD sensitive.

Figure 1A. Typical Circuit for IXD611P7/S7

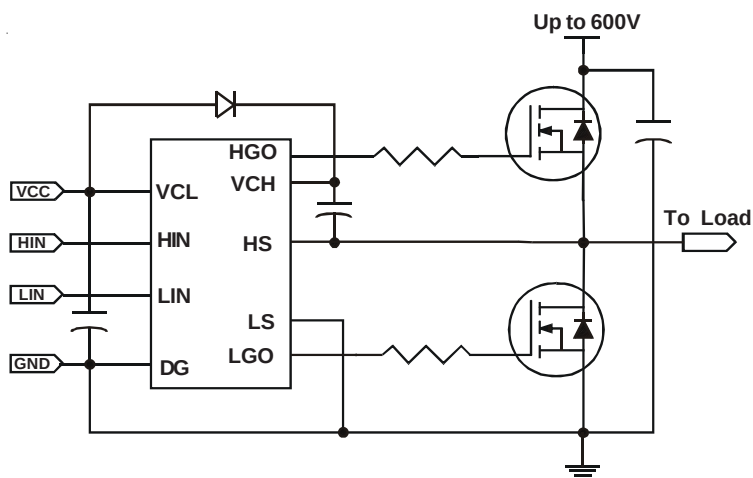


Figure 1B. Typical Circuit for IXD611P1/S1

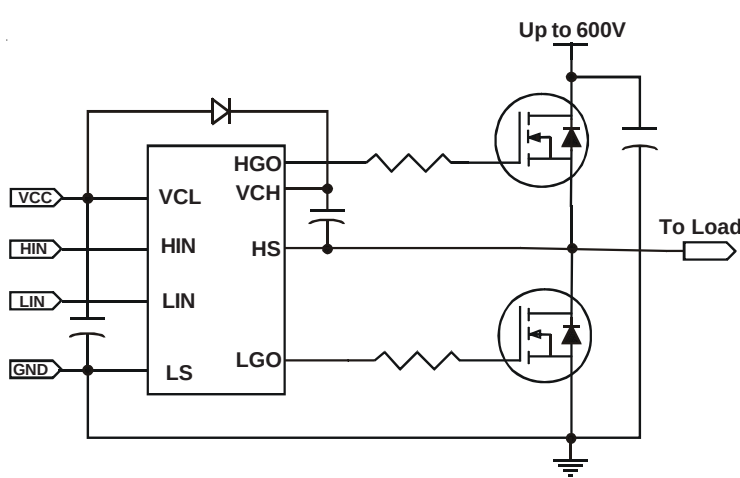
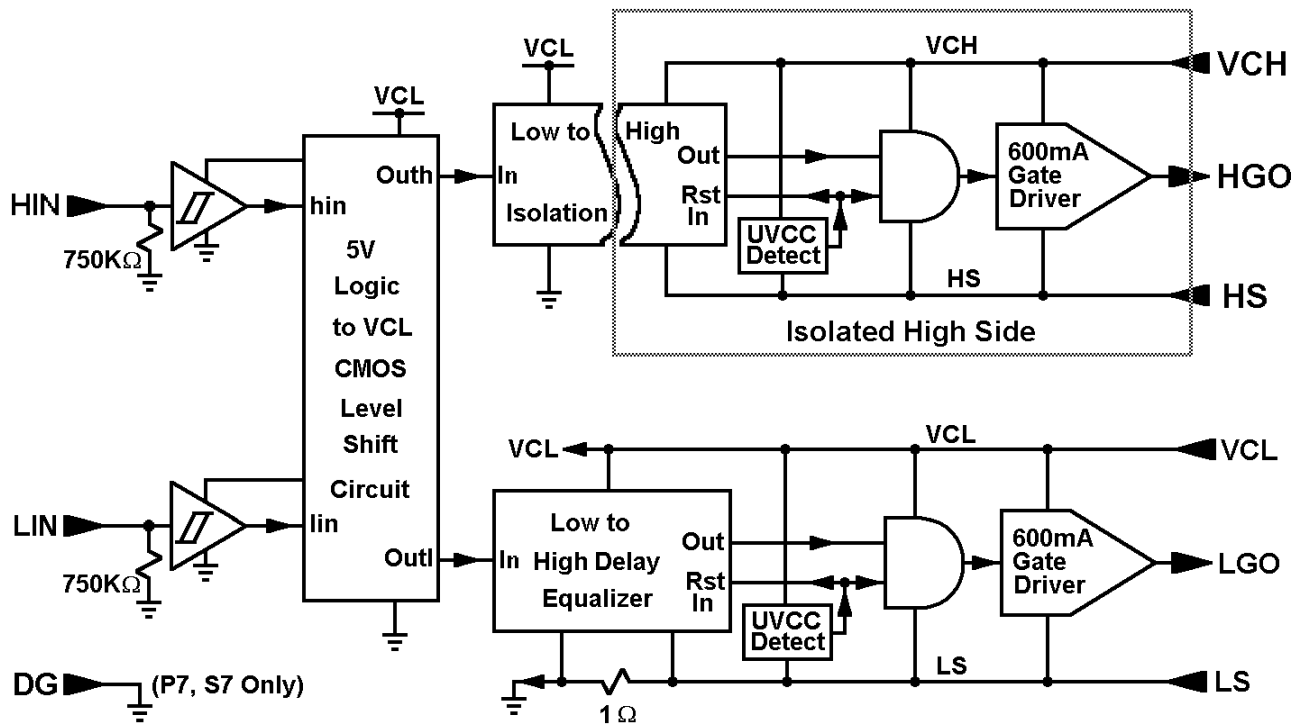


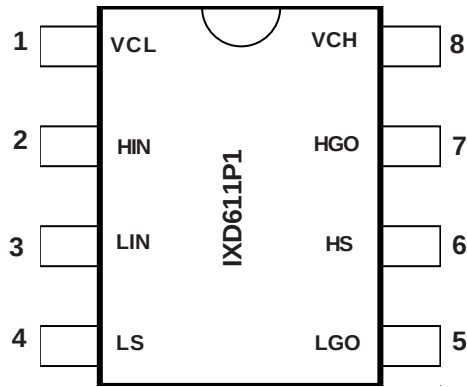
Figure 2. IXD611 Functional Block Diagram



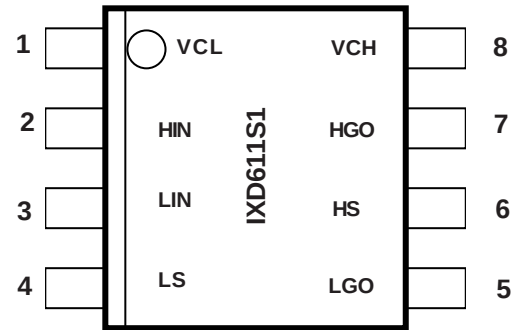
Pin Description And Configuration

SYMBOL	FUNCTION	DESCRIPTION
VCL	Supply Voltage	Low side power supply.
HIN	HS Input	High side Input signal, TTL or CMOS compatible; HGO in phase
LIN	LS Input	Low side Input signal, TTL or CMOS compatible; LGO in phase
DG	Ground	Logic reference ground (Not available for IXD611P1, IXD611S1)
VCH	Supply Voltage	High side floating power supply, referenced to HS
HGO	Output	High side driver output
HS	Return	High side floating ground
LGO	Output	Low side driver output
LS	Ground	Low side ground

Figure 3A. Pin configuration for IXD611P1 (8 pin DIP) and IXD611S1 (8 pin SOIC)

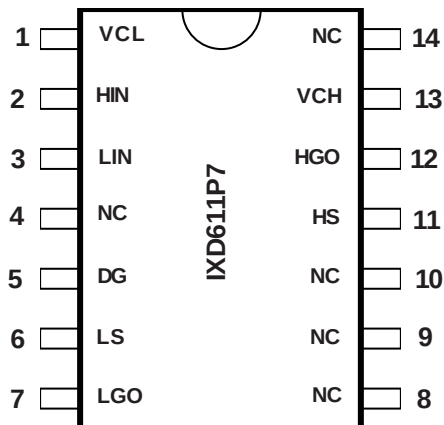


8 pin DIP

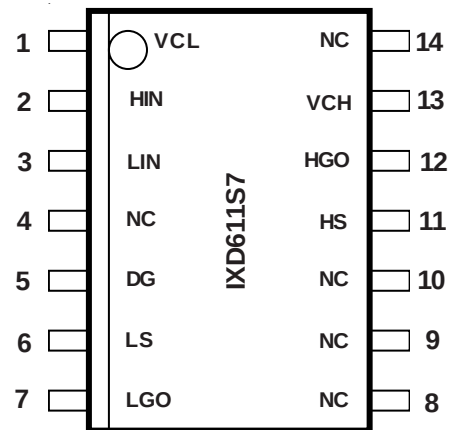


8 pin SOIC

Figure 3B. Pin configuration for IXD611P7 (14 pin DIP) and IXD611S7 (14 pin SOIC)



14 pin DIP



14 pin SOIC

Absolute Maximum Ratings

Symbol	Definition	Min	Max	Units
V_{HS}	High side floating supply offset voltage	-200	650	V
V_{CH}	High side floating absolute voltage	-0.3	35	V
V_{HGO}	High side floating output voltage	$V_{HS} - 0.3$	$V_{CH} + 0.3$	V
V_{CL}	Low side fixed supply voltage	-0.3	35	V
V_{LGO}	Low side output voltage	-0.3	$V_{CL} + 0.3$	V
V_{DG}	Logic supply offset voltage (P7, S7 only)	$V_{LS} - 0.7$	$V_{LS} + 0.7$	V
V_{IN}	Logic input voltage(HIN & LIN)	LS - 0.3	$V_{CL} + 0.3$	V
dV_{HS}/dt	Allowable offset supply voltage transient		50	V/ns
P_D	Package power dissipation@ $T_A \leq 25C$	8 pin PDIP	1.0	W
		8 pin SOIC	0.625	W
		14 pin PDIP	1.6	W
		14 pin SOIC	1.0	W
R_{THJA}	Thermal resistance, junction-to-ambient	8 pin PDIP	125	°C/W
		8 pin SOIC	200	°C/W
		14 pin PDIP	75	°C/W
		14 pin SOIC	120	°C/W
T_J	Junction Temperature		150	°C
T_S	Storage temperature	-55	150	°C
T_L	Lead temperature (soldering, 10 s)		300	°C

Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
V_{HS}	High side floating supply offset voltage	-200	600	V
V_{CH}	High side floating supply absolute voltage	10	30	V
V_{HGO}	High side floating output voltage	V_{HS}	V_{CH}	V
V_{CL}	Low side fixed supply voltage	10	30	V
V_{LGO}	Low side output voltage	0	V_{CL}	V
V_{DG}	Logic supply offset voltage (P7, S7 only)	$V_{LS} - 0.3$	$V_{LS} + 0.3$	V
V_{IN}	Logic input voltage(HIN, LIN)	V_{DG} or LS	V_{CL}	V
T_A	Ambient Temperature	-40	125	°C

Dynamic Electrical Characteristics

Symbol	Definition	Test Conditions	Min	Typ	Max	Units
t_{on}	Turn-on propagation delay	$V_{CL} = V_{CH} = 15V, C_{LOAD} = 1nF$		180	200	ns
t_{off}	Turn-off propagation delay	$V_{CL} = V_{CH} = 15V, C_{LOAD} = 1nF$		170	190	ns
t_r	Turn-on rise time	$V_{CL} = V_{CH} = 15V, C_{LOAD} = 1nF$		28	35	ns
t_f	Turn-off fall time	$V_{CL} = V_{CH} = 15V, C_{LOAD} = 1nF$		18	25	ns
t_{dm}	Delay matching, HS & LS turn-on/off	$C_{LOAD} = 1nF$		10	20	ns

Static Electrical Characteristics

Symbol	Definition	Test Conditions	Min	Typ	Max	Units
V_{INH}	Logic "1" input voltage	$V_{CL} = V_{CH} = 15V$	2.7			V
V_{INL}	Logic "0" input voltage	$V_{CL} = V_{CH} = 15V$			2.4	V
V_{HLGO}/V_{HHGO}	High level output voltage, $V_{CH}-V_{HGO}$ or $V_{CL}-V_{LGO}$	$I_O = 20mA$		0.22	0.3	V
V_{LLGO}/V_{LHGO}	Low level output voltage, V_{HGO} or V_{LGO}	$I_O = 20mA$		0.16	0.25	V
I_{HL}	HS to LS bias current.	$V_{HS} = 600V$		0.12	0.2	mA
I_{QHS}	Quiescent V_{CH} supply current	$V_{CH} = 15V, V_{IN} = 0V$ or $V_{IN} = 5V$		0.7	0.8	mA
I_{QLS}	Quiescent V_{CL} supply current	$V_{CL} = 15V, V_{IN} = 0V$ or $V_{IN} = 5V$		0.18	0.3	mA
I_{IN}^+	Logic "1" input bias current	$V_{IN} = V_{SUPPLY} = 15V$		11	20	uA
I_{IN}^-	Logic "0" input bias current	$V_{IN} = 0V$		1	2	uA
V_{CHUV}^+	V_{CH} supply undervoltage positive going threshold.		7.5	8	8.5	V
V_{CHUV}^-	V_{CH} supply undervoltage negative going threshold.		7	7.3	8	V
V_{CLUV}^+	V_{CL} supply undervoltage positive going threshold		7.5	8	8.5	V
V_{CLUV}^-	V_{CL} supply undervoltage negative going threshold.		7	7.5	8	V
V_{CHUVH}, V_{CLUVH}	Undervoltage Hysteresis		0.3	0.6		V
I_{GO}^+	HS or LS Output high short circuit current; $V_{GO} = 15V, V_{IN} = 5V, PW < 10\mu s$		0.5	0.6		A
I_{GO}^-	HS or LS Output low short circuit current; $V_{GO} = 15V, V_{IN} = 0V, PW < 10\mu s$		-0.6	-0.5		A

Precaution : When performing the high voltage tests, adequate safety precautions should be taken.

The diagram shows two digital signals over a 100ns period. The top signal, LIN/HIN, is a square wave that is high for 40ns and low for 60ns. The bottom signal, LGO/HGO, is also a square wave that is high for 40ns and low for 60ns. The signals are in phase.

The diagram illustrates the timing relationships for a 100 Gbps 2R optical receiver. It shows the Input Signal (HIN, LIN) and the Outgoing Signal (HGO, LGO) with various timing parameters. The input signal has a 50% duty cycle. The outgoing signal has a 10% duty cycle. The timing parameters include LGO (Low Gate Offset), HGO (High Gate Offset), and tdm (Time Delay Margin).

The graph shows the relationship between the PWM frequency (f_{PWM}) and the V++ Buss voltage (V_{HS}). The y-axis represents V_{HS} in Volts, with a break between 400V and 500V. The x-axis represents f_{PWM} in kHz, with a break between 300kHz and 1MHz. The voltage is constant at 600V for frequencies up to 100kHz. Between 100kHz and 300kHz, the voltage decreases linearly from 600V to 500V. This region is labeled "Sample Tested for Operation". For frequencies from 300kHz to 1MHz, the voltage remains constant at 500V.

f_{PWM} (kHz)	V_{HS} (V)
0 - 100	600
100 - 300	Linear decrease from 600V to 500V
300 - 1000	500

IXYS reserves the right to change limits, test conditions, and dimensions. 6



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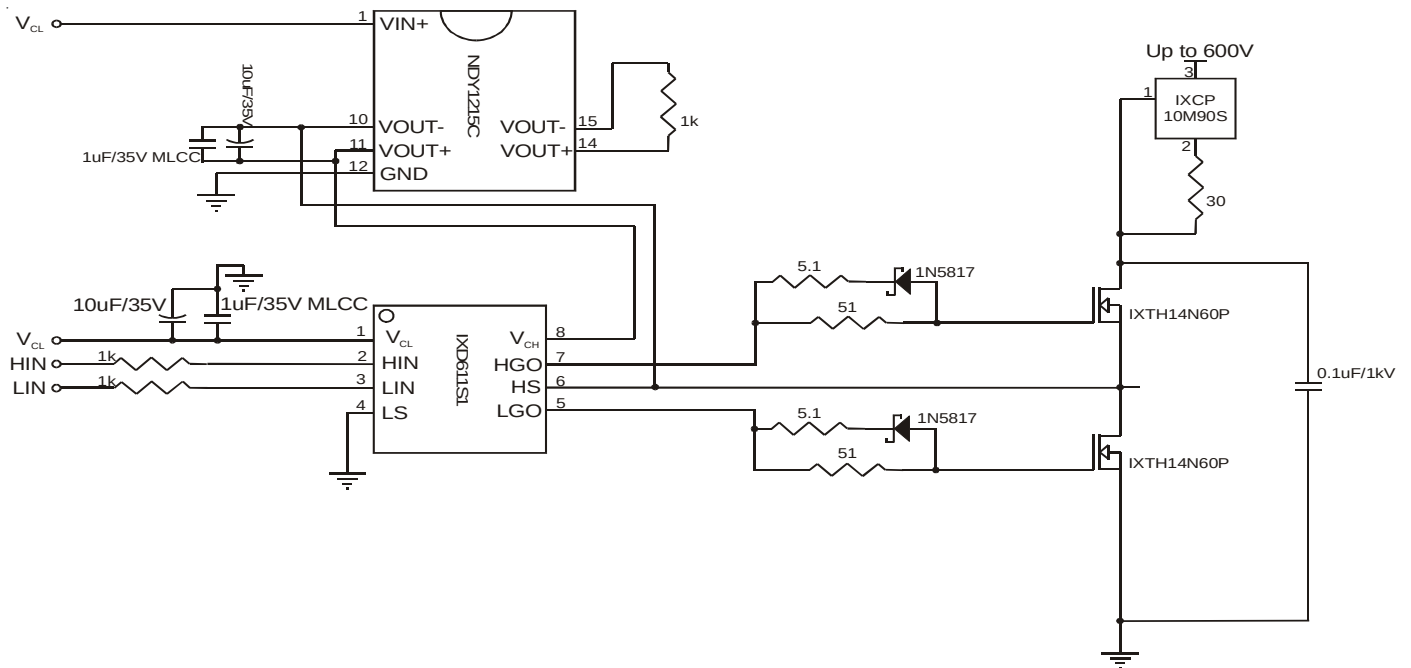


Figure 10. Test circuit for low frequency, 75kHz, operation.

$$V_{CH}, V_{CL} = 15V$$

Fig. 11 Rise Times vs. Supply Voltage

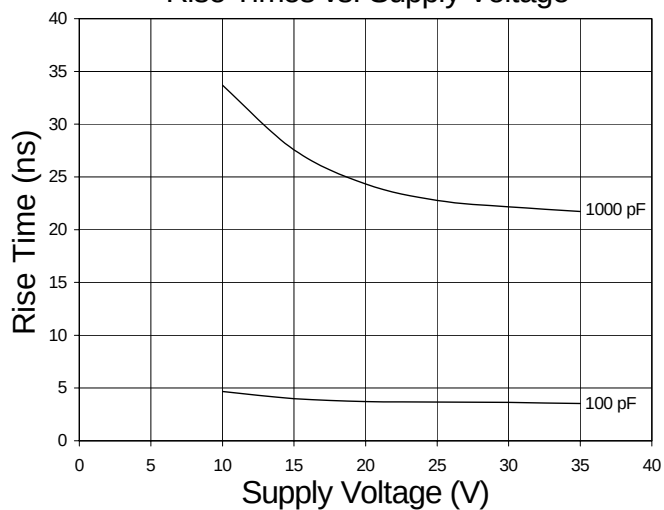


Fig.12 Fall Times vs. Supply Voltage

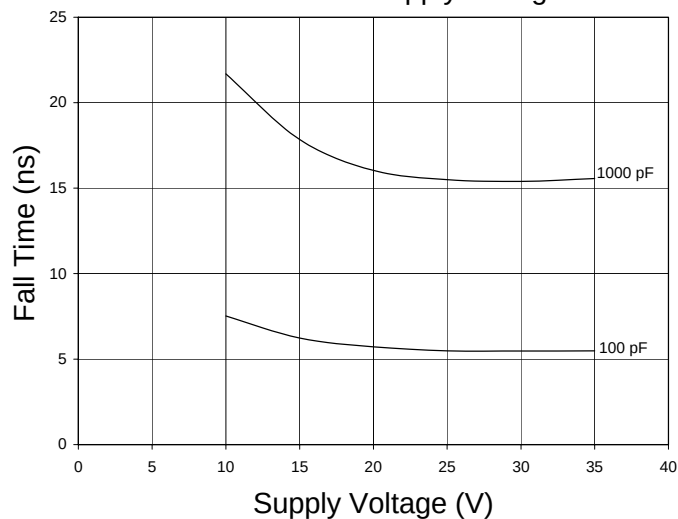


Fig. 13 Rise / Fall Times vs. Temperature
 $V_{IN} = V_{SUPPLY} = 15V$ $C_{LOAD} = 1000pF$

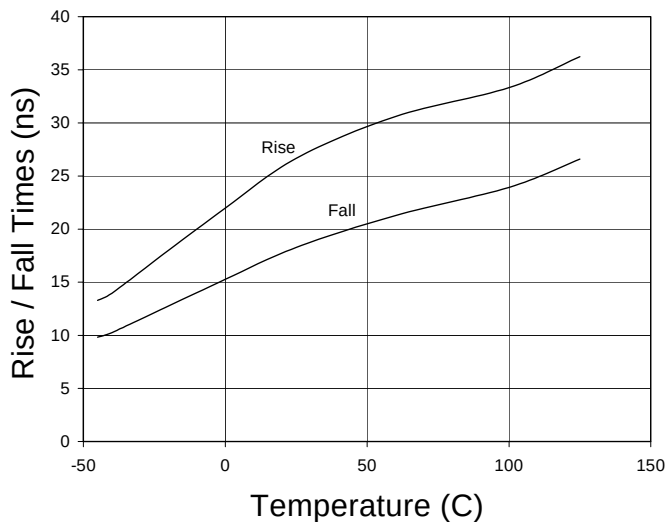


Fig. 14 Propagation Delay vs. Supply Voltage
 $C_L = 1000pF$ $V_{IN} = V_{SUPPLY}$

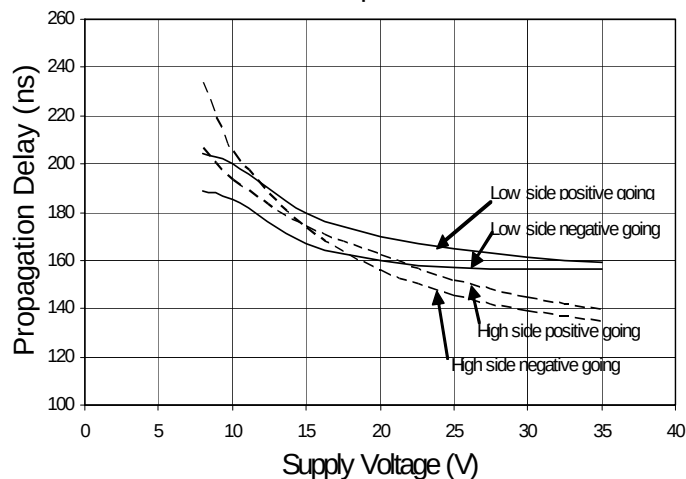


Fig.15 Propagation Delay vs. Temperature
 $V_{IN} = V_{SUPPLY} = 15V$ $C_{LOAD} = 1000pF$

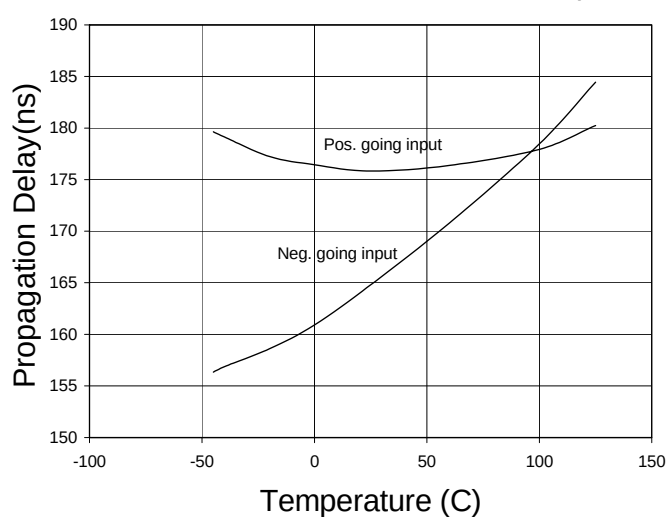


Fig. 16 Under Voltage Lock Out vs. Temperature

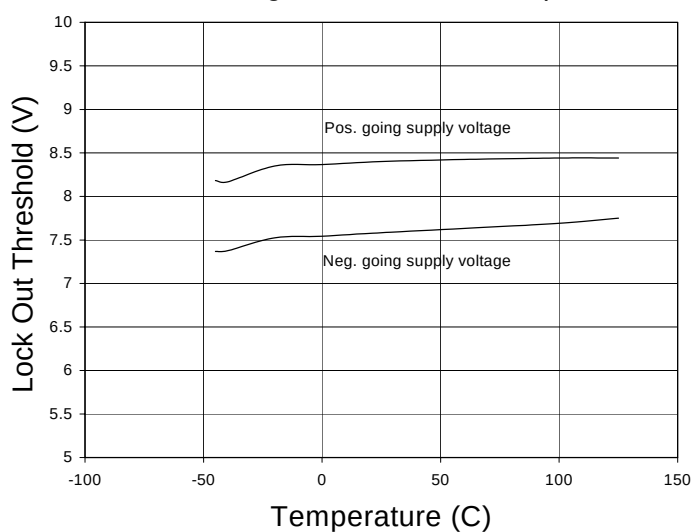


Fig. 17

Input Threshold Level vs. Supply Voltage

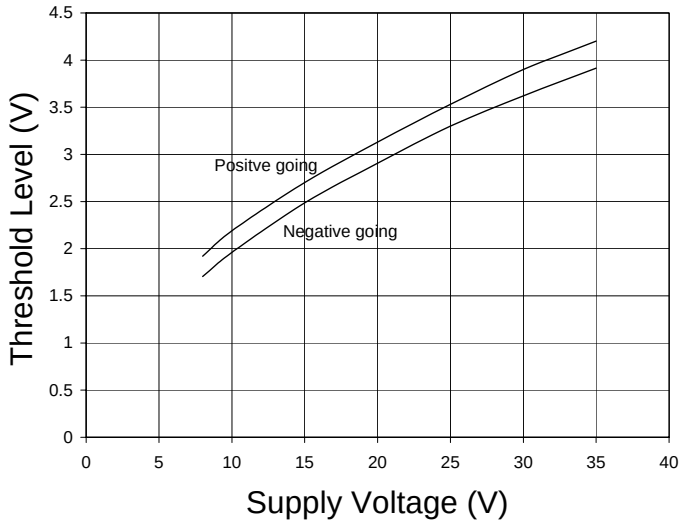


Fig. 18 Input Threshold Level vs. Temperature

$V_{SUPPLY} = 15V$

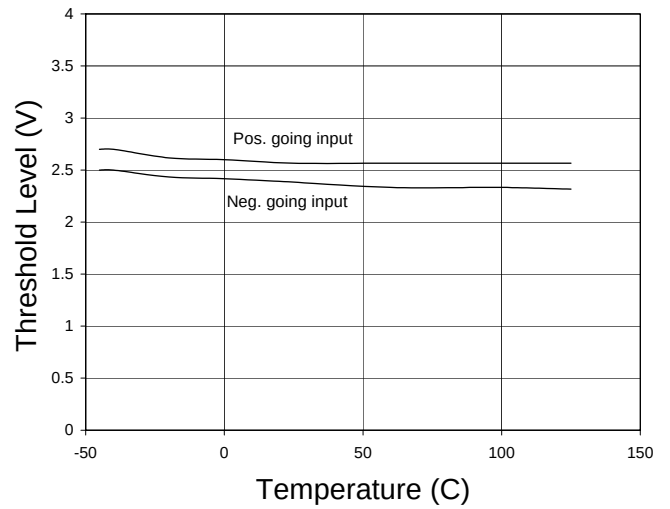


Fig.19

Quiescent Supply Current vs. Supply Voltage

$V_{IN} = "0"$

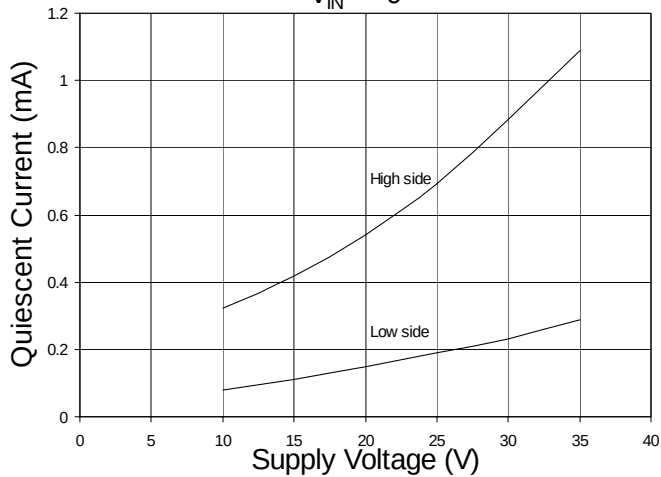


Fig. 20

Quiescent Current vs. Temperature

$V_{IN} = "0"$ $V_{SUPPLY} = 15V$ Both Drivers Combined

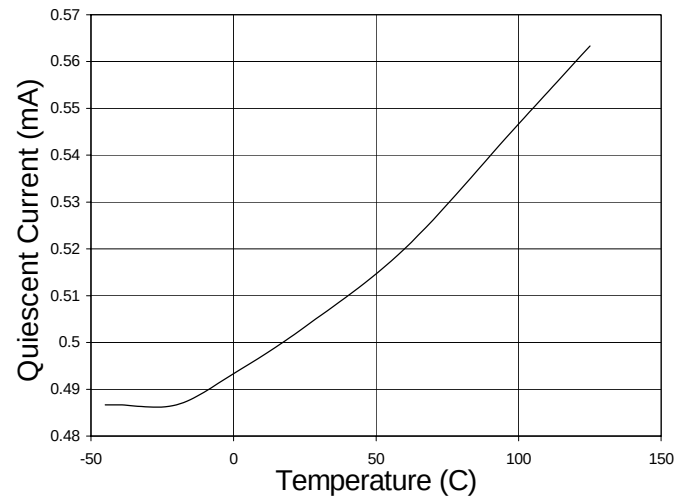


Fig.21

LIN / HIN Bias Current vs. Supply Voltage

$V_{IN} = \text{Supply Voltage}$

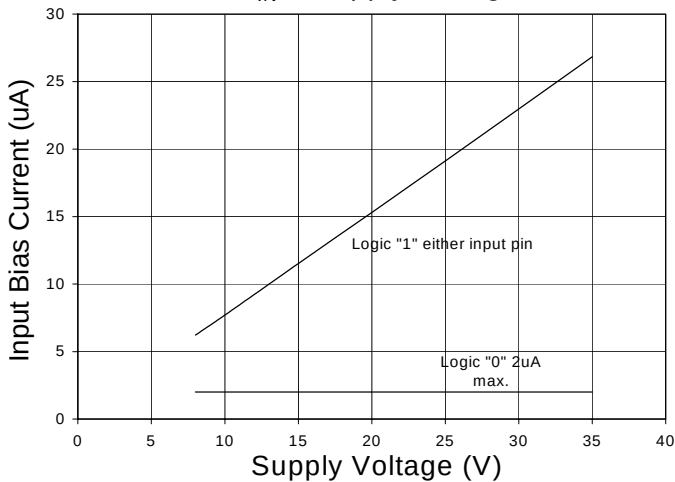


Fig.22

LIN / HIN Bias Current vs. Temperature

$V_{SUPPLY} = 15V$

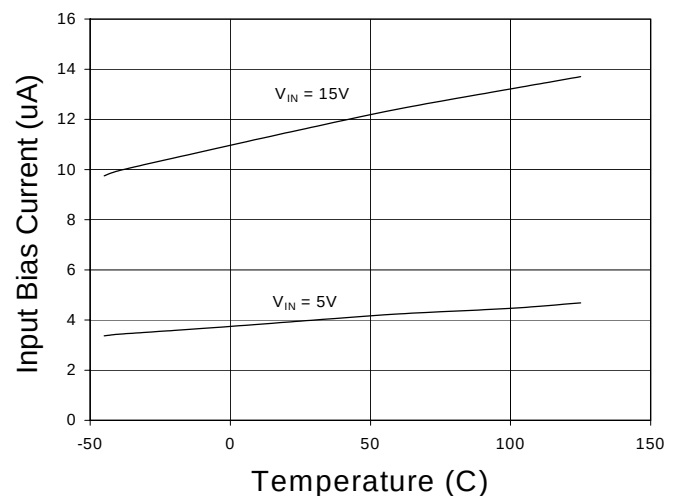


Fig. 23
Low Level Output Voltage vs. Supply Voltage
 $I_o = 20\text{mA}$

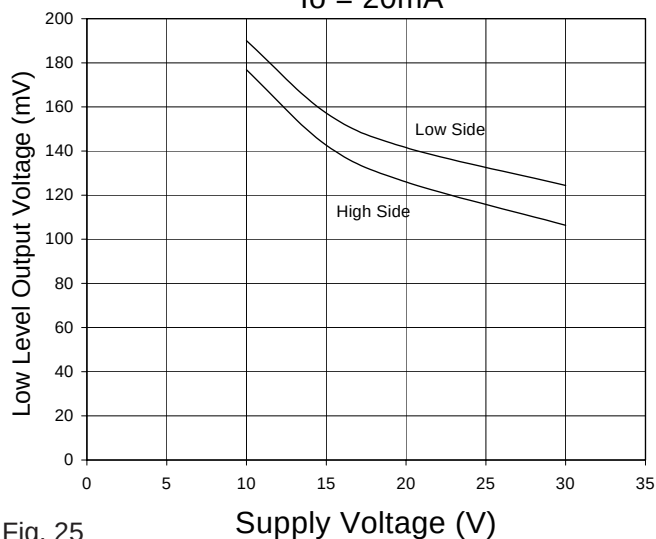


Fig. 24
High Level Output Voltage vs. Supply Voltage
 $I_o = 20\text{mA}$

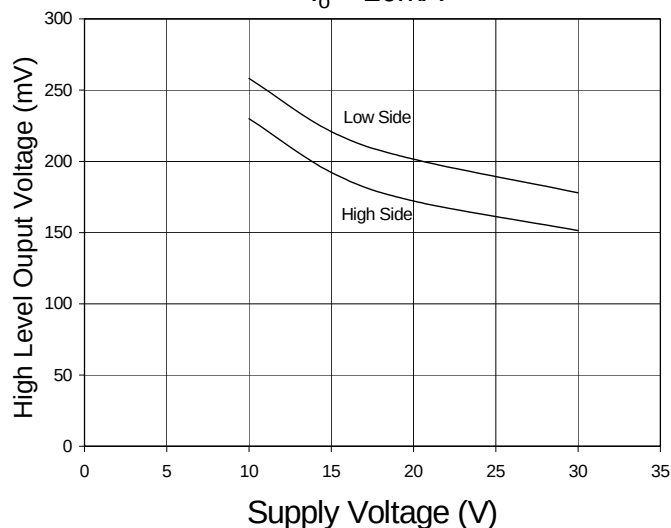


Fig. 25
Output Source Current vs. Supply Voltage

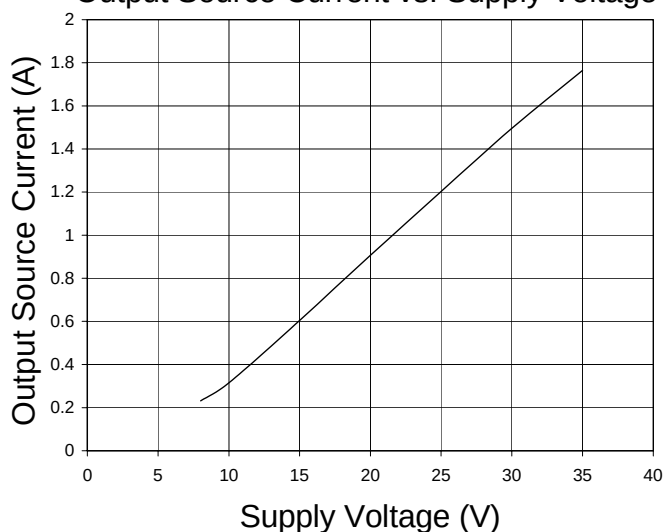


Fig. 26
Output Sink Current vs. Supply Voltage

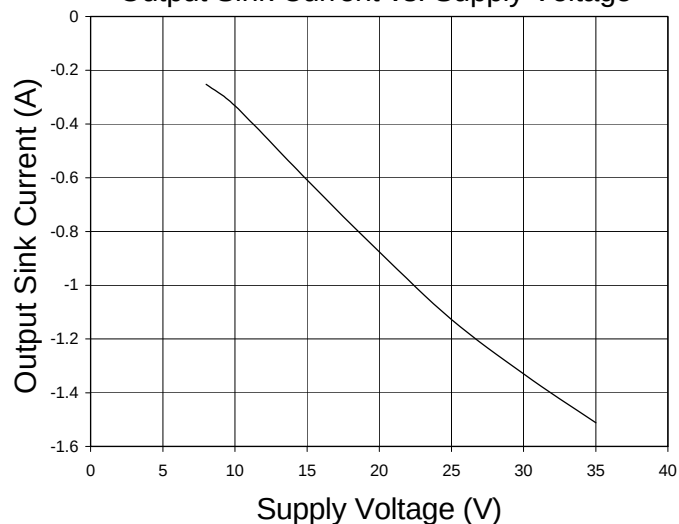


Fig. 27
Output Source Current vs. Temperature
 $V_{\text{SUPPLY}} = 15\text{V}$

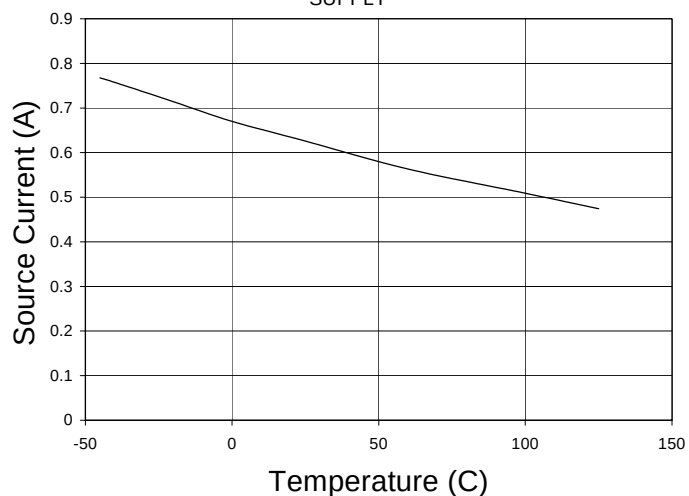


Fig. 28
Output Sink Current vs. Temperature
 $V_{\text{SUPPLY}} = 15\text{V}$

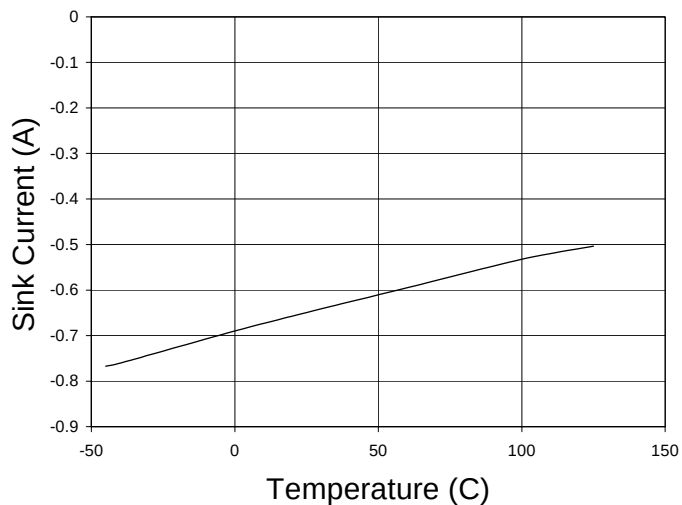


Fig. 29 Supply Current vs. Supply Voltage
 $C_{LOAD} = 100pF$ $V_{IN} = V_{SUPPLY}$ 50% Duty Cycle

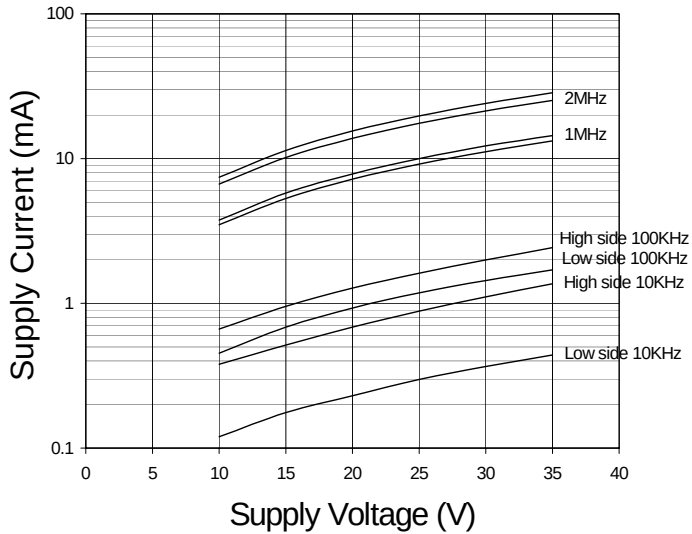


Fig. 30 Supply Current vs. Supply Voltage
 $C_{LOAD} = 1000pF$ $V_{IN} = V_{SUPPLY}$ 50% Duty Cycle

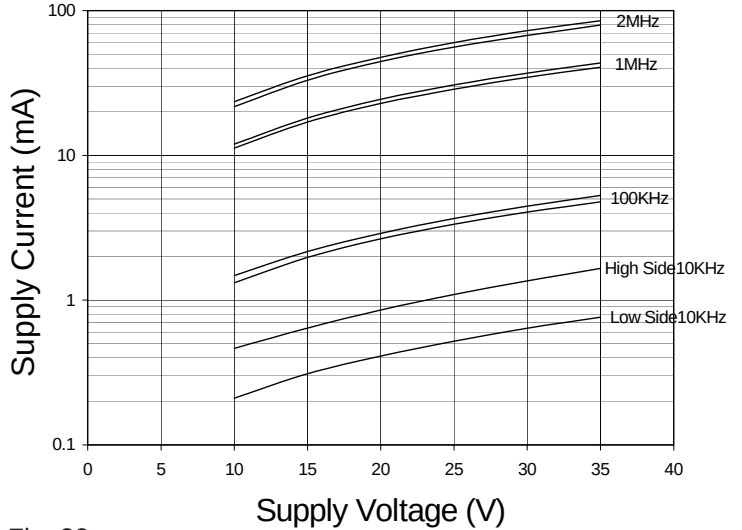


Fig. 31 High To Low Side Leakage Current vs. High Side V_{OFFSET}

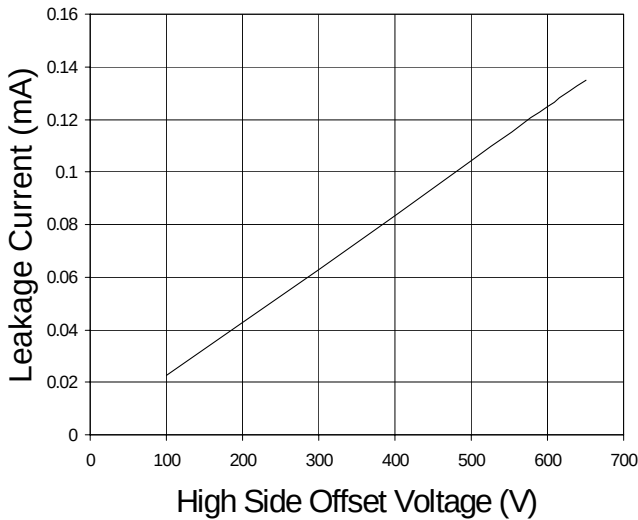


Fig. 32 High to Low Side Leakage Current vs. Temperature
 $V_{OFFSET} = 600V$ $V_{CL} = V_{CH} = 15V$

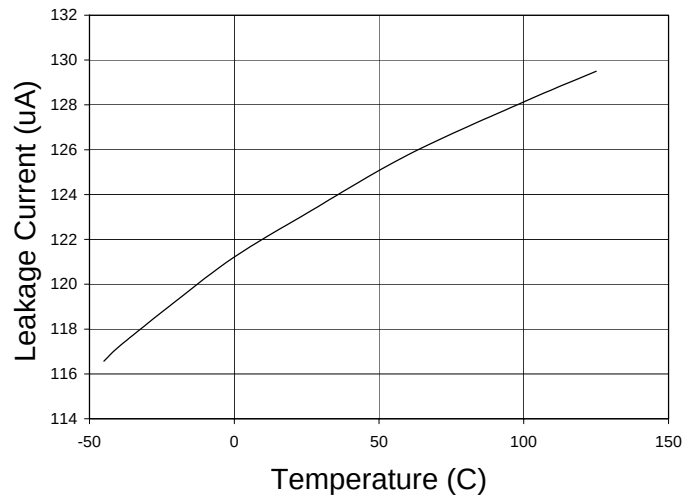


Fig. 33 Output Resistance vs. Supply Voltage

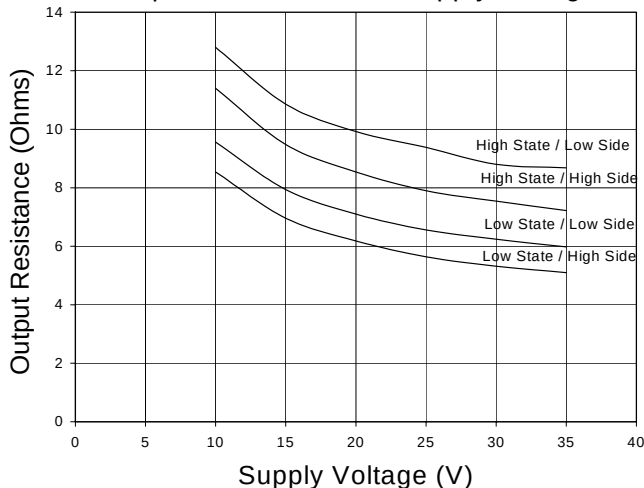


Fig. 34 Pulse Width Stability vs. Temperature
 $V_{CL} = V_{CH} = 15V$ Input PW = 300ns

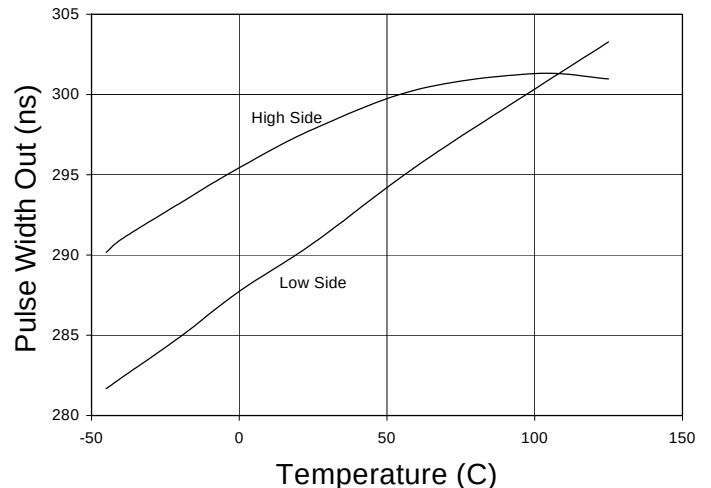


Fig. 35

Normalized PW Out vs. PW In (Low Side)

$V_{IN} = V_{SUPPLY} = 10V, 20V, 30V$ $C_{LOAD} = 1000pF$

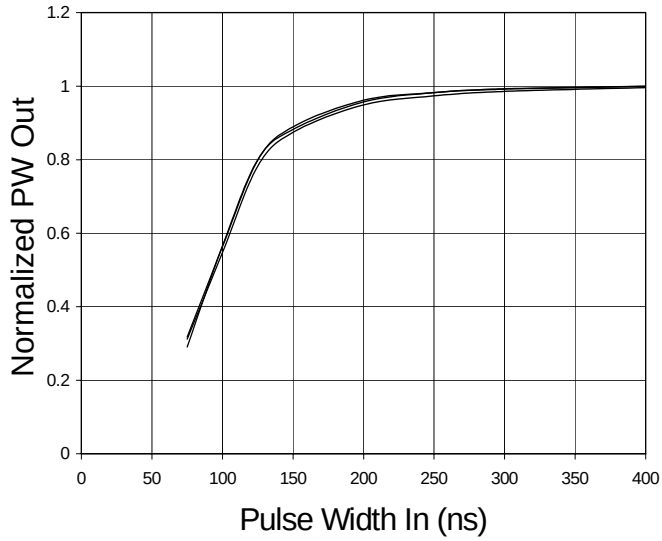
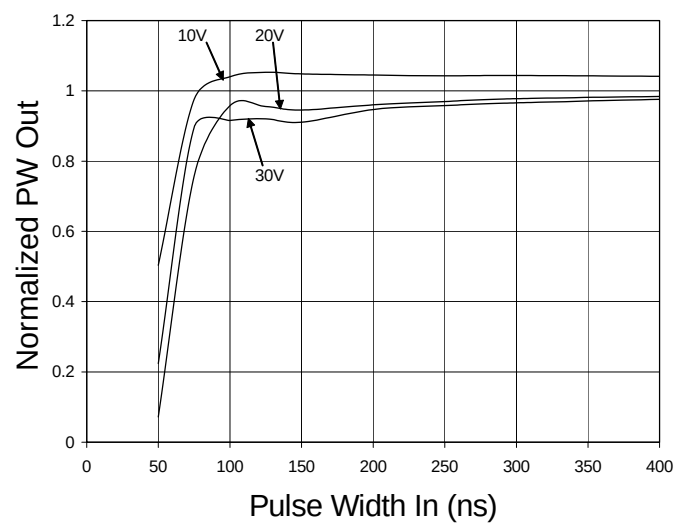
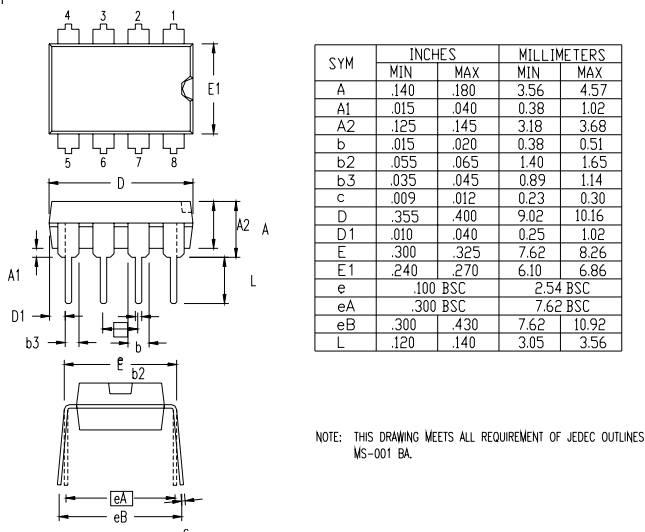
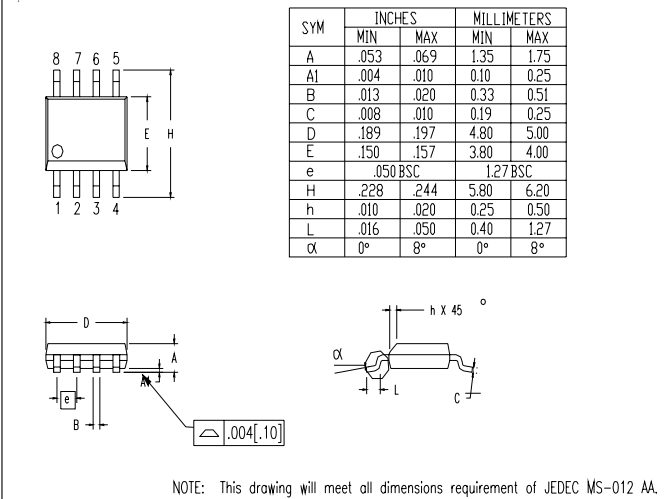
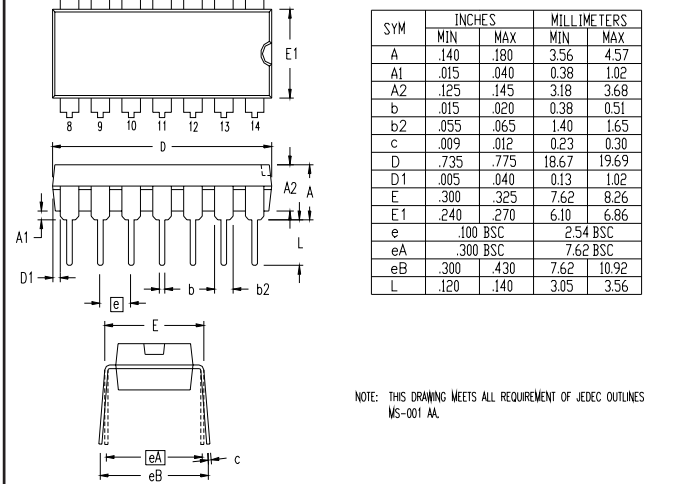
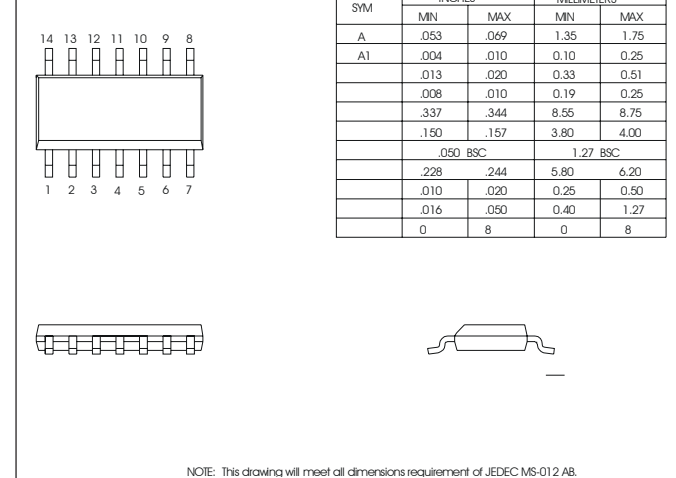


Fig. 36

Normalized PW Out vs. PW In (High Side)

$V_{IN} = V_{SUPPLY} = 10V, 20V, 30V$ $C_{LOAD} = 1000pF$



IXD611P1 Package

IXD611S1 Package

IXD611P7 Package

IXD611S7 Package


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